DesignCon 2009
PCB Power Delivery Optimizations for the Cost Driven Era

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The Power Deliver Problem

- Support DC current requirements of each IC

- Support AC current requirements of each IC

- Sufficiently suppress AC noise between separate IC power nodes and ICs

- Support I/O return path impedance requirements

- Meet emissions and susceptibility requirements

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Divide and Conquer

- Divide the problem between what is on the PCB and the requirements and parasitics of each IC

- Results in impedance budget for each IC at the PCB attach

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What We Can Control On the PCB

- PCB stack-up
- PCB laminate selection
- Bypass capacitor selection
- Bypass network design
- Choices interact
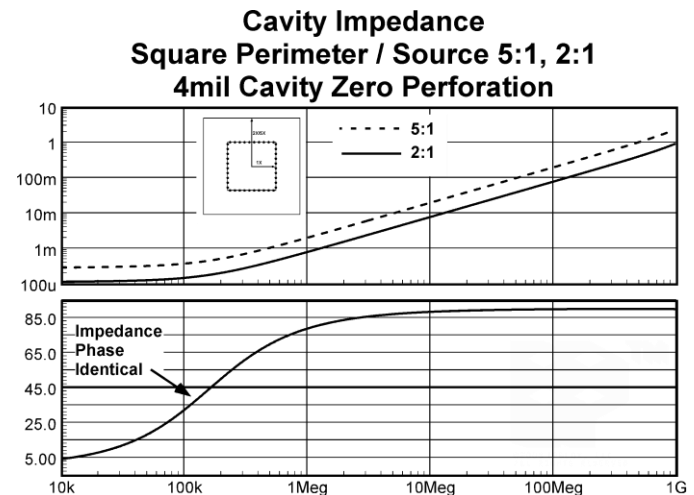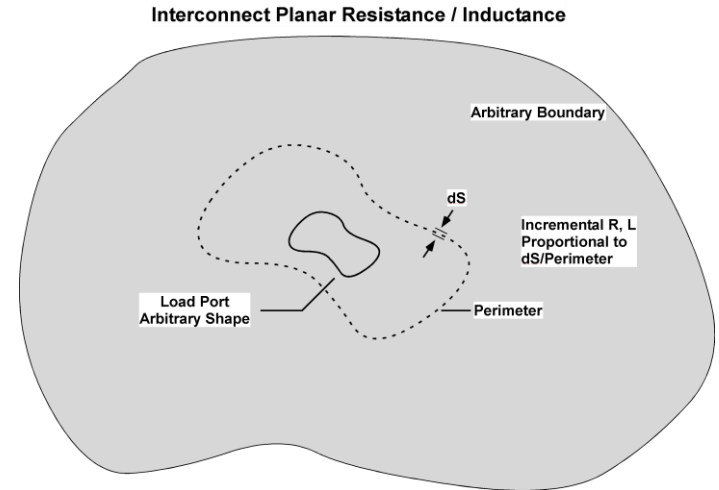
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Power Plane Behavior

- Power plane cavities exhibit two distinct behaviors:
  - Distributed impedance
    - How the cavity appears to many loads distributed over the cavity X-Y extents
    - Very low inductance, modest value capacitor
    - Thin cavities increase capacitance
  - Local impedance
    - How the cavity appears to any given load
    - Series R-L out to bypass caps & VRM
    - Thin cavities decrease inductance

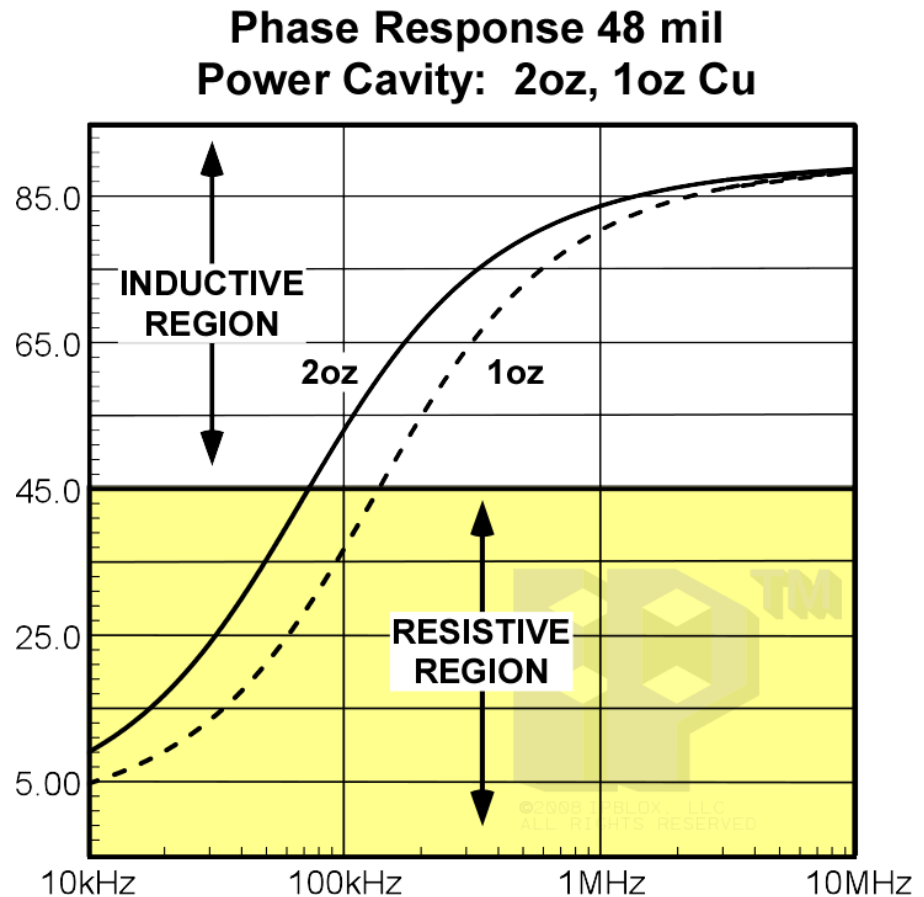TERASPEED CONSULTING GROUP

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Plane Cavity R / L

- In the X-Y plane, spreading resistance and inductance both scale identically
  - Simulation computations can be greatly reduced by solving first as just an R-mesh, and then reducing the result to a matrix or RLCs between IC and capacitor attachment nodes and then solving complex Z vs Freq

- Changing the size / shape of a polygon changes |Z| but not phase

Interconnect Planar Resistance / Inductance

Arbitrary Boundary

dS

Incremental R, L Proportional to dS/Perimeter

Load Port Arbitrary Shape

Perimeter

Cavity Impedance
Square Perimeter / Source 5:1, 2:1
4mil Cavity Zero Perforation

- - - - 5:1
——— 2:1

Impedance Phase Identical

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Cavity Height and Complex Z

- R/L behavior depends on:
  - Conductor bulk resistance,
  - Skin effect,
  - Conductor relative permeability, 1.0 for copper
  - Cavity dielectric height
- Reflected as phase response of interconnect alone

Phase Response 48 mil Power Cavity: 2oz, 1oz Cu

INDUCTIVE REGION

2oz   1oz

85.0

65.0

45.0

RESISTIVE REGION

25.0

5.00

10kHz   100kHz   1MHz   10MHz

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# Cavity Height and Complex Z

- Thick cavities exhibit almost no local skin effect

- Local power connections inductive from 73kHz 2oz, 138kHz 1oz

- Z phase 2oz crosses 45 deg 0.53F of 1oz
  - W/o skin effect w/b 0.50F

Phase Response 48 mil
Power Cavity: 2oz, 1oz Cu

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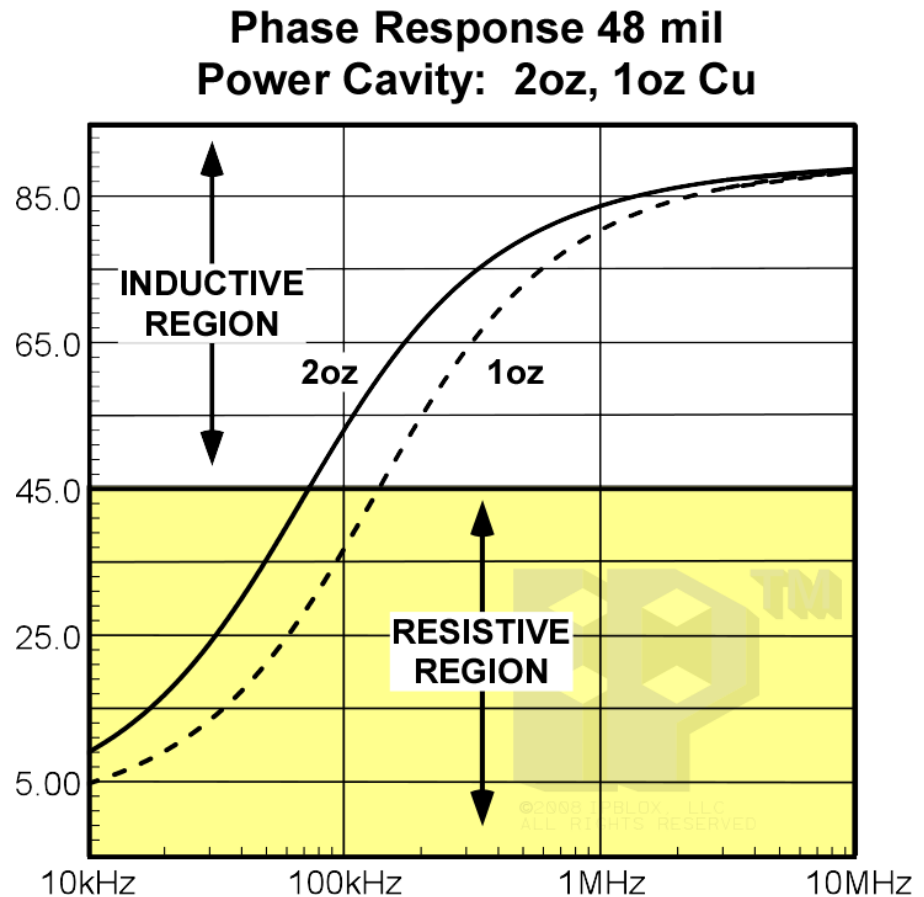
Cavity Height and Complex Z

- Cavity transition to inductive response occurs:
  - <150kHz for 48mil 1oz
  - <3MHz   for 4mil 1oz
  - <15MHz for 1mil 1oz
    - Skin effect apparent

- Three key parameters are:
 - **INDUCTANCE**, and **INDUCTANCE**, and **INDUCTANCE**

Cavity Impedance
Square Perimeter / Source 2:1
Zero Perforation, 1oz / 2oz Cu

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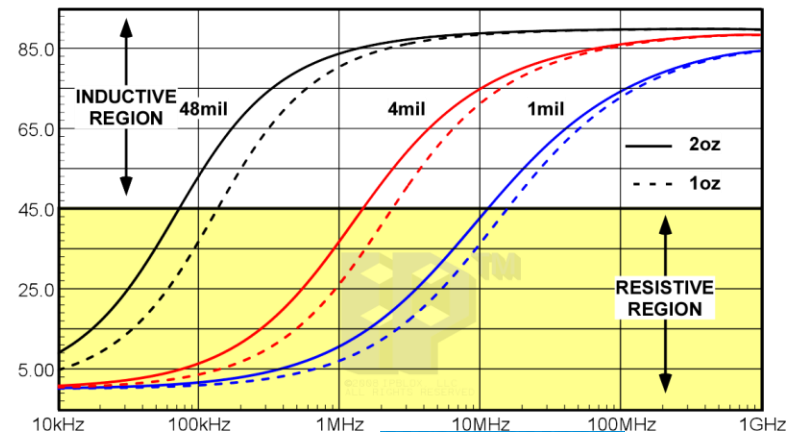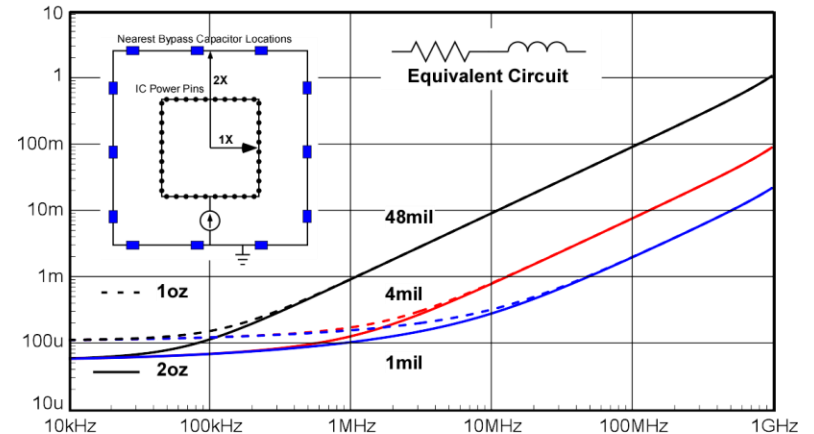
PDN as Collection of Local PDNs

- Good approximation that handles worst case-
  - All ICs draw I_{AC_MAX} in phase
- Approximation becomes increasingly accurate for thick cavities
  - Spreading |Z| isolates non-local bypass
- Effective divide and conquer
  - Second pass optimization *may* reduce final requirements

PDN as Collection of Local Loads

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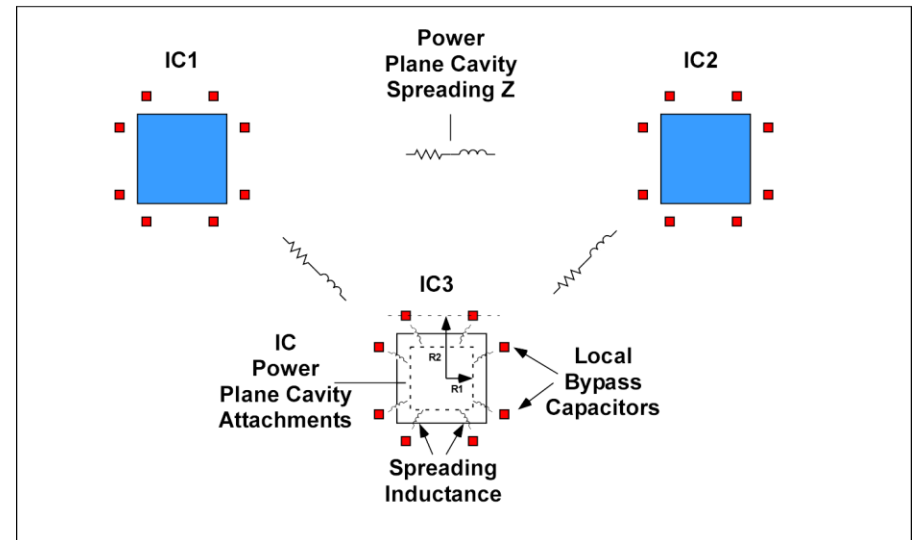
PDN as Collection of Local PDNs

- Solve PDN for each IC first

- Adjust for full optimization second
  - Useful tools: Optimize PI™, Hyperlinx™, SI-Wave™

- Adjust for resonances and EMI hot-spots third

PDN as Collection of Local Loads

IC1   Power Plane Cavity Spreading Z   IC2

IC3

IC Power Plane Cavity Attachments   Local Bypass Capacitors

Spreading Inductance

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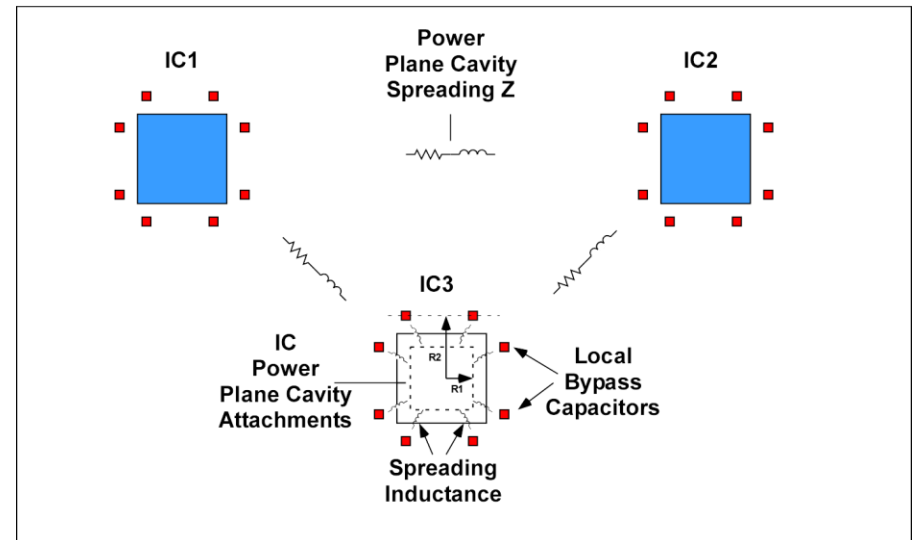
2 Routing Layer Constructions

- 4 layer, thick power cavity traditional
  - Very high impedance cavity
    - Typical 300pH L_{SPREAD} to IC power
  - Peripheral bypass caps below 300pH little effect
  - < 300pH Relies on enough power / gnd pairs directly under IC to bottom of PCB and caps to match

2 Signal Layer Constructions

| 4 Layer | 6 Layer | 6 Layer | 6 Layer | 6 Layer |
| One FR406 Power Cavity | One FR06 Power Cavity | One HK04 Power Cavity | Two FR406 Cavities | Two HK04 Cavities |

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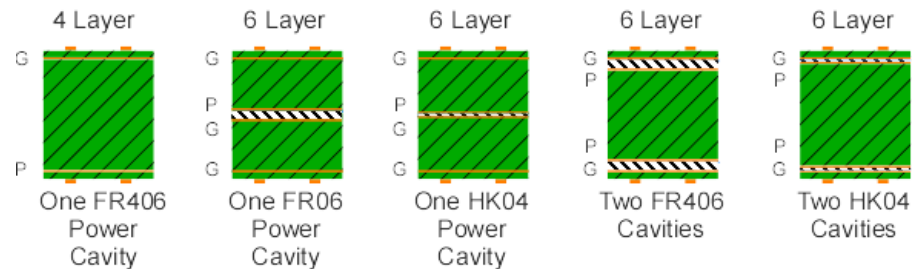
2 Routing Layer Constructions

- Add thin power cavity to center?
  - IC Z axis L improves 2:1
  - Caps can go top or bottom
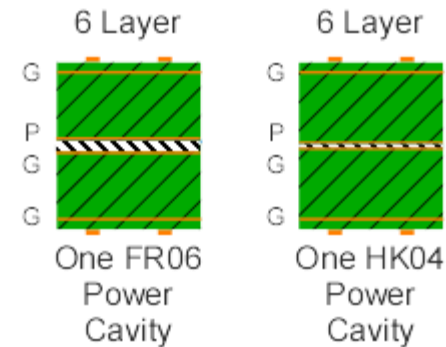- Total Z axis still very high for caps and IC

2 Signal Layer Constructions

6 Layer

6 Layer

One FR06 Power Cavity

One HK04 Power Cavity

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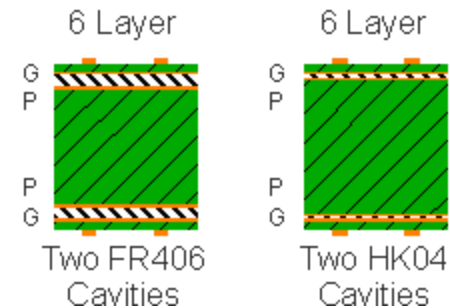# 2 Routing Layer Constructions

- Add thin power cavities to outside
  - IC Z axis very low
  - Cap attach very low
  - L/R spreading very low
- Bottom cavity natural puddle, or add'l route (4mil), or combination

2 Signal Layer Constructions

6 Layer	6 Layer
G P	G P
P G	P G
Two FR406 Cavities	Two HK04 Cavities

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4 Routing Layer Constructions

- Traditional 6 layer same as 4 layer
  - For Tx line return purposes 2 PCBs, top and bottom
- 8 layer constructions very different than 6 layer
  - IC Z axis drops
  - 2 power cavities
    - Can puddle bottom

4 Signal Layer Constructions

6 Layer	8 Layer	8 Layer
One FR406 Power Cavity	Two FR406 Power Cavities	Two HK04 Cavities

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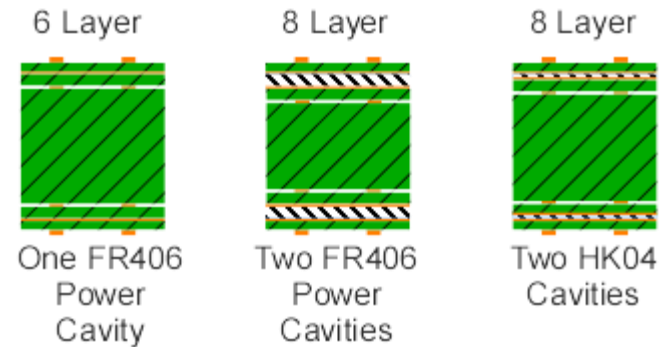
Caps Req'd Versus L

- ## Caps peripheral to IC using thick cavities:
  - Poor effectiveness

- ## Caps under IC
  - Works adequately if IC mfg provides enough pwr/gnd via pairs
  - If not 4 layer design won't work

Inductance Bypass Network to IC Power Cavity Attach

1. 50 mil cavity
   Caps around IC

2. 4 mil center cavity
   Caps around IC

3. 4 mil cavities, top used
   Caps around IC

4. Bottom caps only

5. 1 mil cavities, top used
   Caps around IC only

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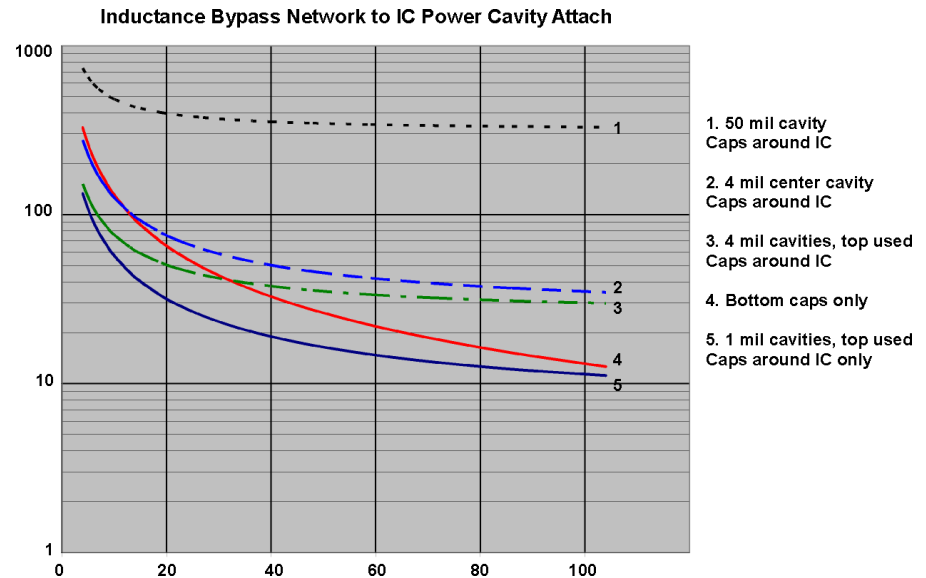
Caps Req'd Versus L

- Caps peripheral to IC using thin cavities:
  - Can eliminate many caps
  - How many depends on target L, cavity thickness
  - Only works down to L_{SAT}

Inductance Bypass Network to IC Power Cavity Attach

1. 50 mil cavity Caps around IC

2. 4 mil center cavity Caps around IC

3. 4 mil cavities, top used Caps around IC

4. Bottom caps only

5. 1 mil cavities, top used Caps around IC only
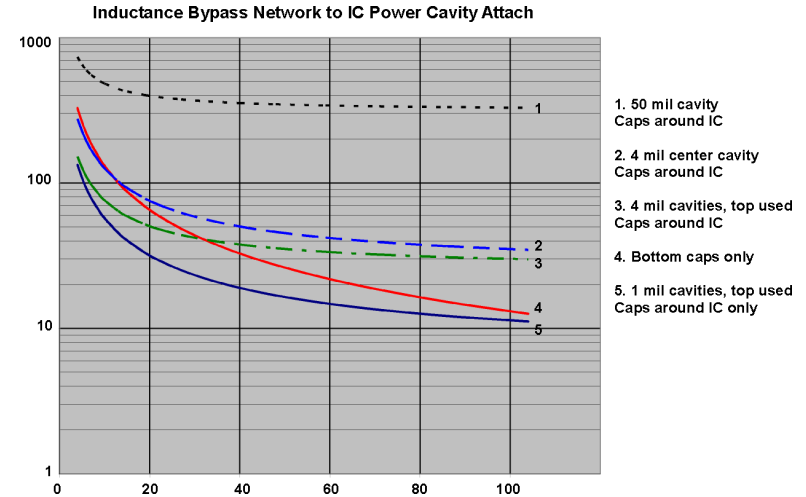
	0402	X2Y	L_{SAT}
4 layer, 50 mil center	6	2	625pH
6 layer, 4 mil center	41	11	50pH
6 layer, 4 mil top	21	6	50pH
6 layer, 1 mil top	81	24	13pH

Figure 1, Inductance Saturation Capacitor Counts, Typical

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Caps Req'd vs L$_{TGT}$
2 / 4 Routing Layer PCBs

Target Inductance	0402			X2Y™	
	4/6 Layer	6/8 Layer		6/8 Layer	
	Bottom Caps	4mil	1mil	4mil	1mil
5pH	363	No Solution	No Solution	No Solution	No Solution
10pH	182	No Solution	136	No Solution	37
20pH	91	No Solution	37	No Solution	10
30pH	61	102	21	28	6
40pH	46	34	15	9	4
50pH	37	20	12	6	3
60pH	31	15	9	4	3
70pH	26	11	8	3	2
80pH	23	9	7	3	2
90pH	21	8	6	2	2
100pH	19	7	5	2	1
120pH	16	5	4	1	1
140pH	13	4	4	1	1
160pH	12	4	3	1	1
180pH	11	3	3	1	1
200pH	10	3	3	1	1
220pH	9	3	2	1	1

Capacitor Counts vs. Inductance to IC Attach 0.062" PCB

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Caps Req'd vs L_{TGT}
2 / 4 Routing Layer PCBs

- At modest L_{TGT}:
  - 90pH < L_{TGT} < 300pH

  4mil, 1mil drops caps ≈ 3:1, 4:1 versus 50/42mil

- More demanding L_{TGT} more advantage to 1mil versus 4mil cavities

- Combination of 1mil and X2Y® 10:1 cap reduction from 200pH down to 20pH L_{TGT}
  - 200pH 63mOhms @ 50MHz
  - 20pH   6.3mOhms @ 50MHz

| Target Inductance | 0402 | | | X2Y™ | |
| | 4/6 Layer | 6/8 Layer | | 6/8 Layer | |
	Bottom Caps	4mil	1mil	4mil	1mil
5pH	363	No Solution	No Solution	No Solution	No Solution
10pH	182	No Solution	136	No Solution	37
20pH	91	No Solution	37	No Solution	10
30pH	61	102	21	28	6
40pH	46	34	15	9	4
50pH	37	20	12	6	3
60pH	31	15	9	4	3
70pH	26	11	8	3	2
80pH	23	9	7	3	2
90pH	21	8	6	2	2
100pH	19	7	5	2	1
120pH	16	5	4	1	1
140pH	13	4	4	1	1
160pH	12	4	3	1	1
180pH	11	3	3	1	1
200pH	10	3	3	1	1
220pH	9	3	2	1	1

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Evaluating Costs

- Evaluation comes down to the big three:
  - PCB material cost
  - Bypass caps, BOM cost
  - Bypass caps, placement cost
- Conventional bypass caps are almost free
  - $0.001 typical in high volume
- Assembly placement cost is the critical parameter for both more and/or better PCB materials and/or better caps

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Evaluating Costs

- At current prices, break-even on 4/6 layer alternatives occurs near $0.01 / comp placement
  - Why?
    - Adding 1 layer of FR406 adds $2.00/sq ft / $0.014 / sq"
      - Save 1.3 caps / sq" pays back - $2.00 / (144 * $0.011)
    - Changing 2 layers of FR406 to HK04 adds $6.00/sq ft
      - Save 3.8 caps / sq" pays back - $6.00 / (144 * $0.011)
    - X2Y™ replaces caps ≈ 4:1
      - $0.03 comp + $0.01 place ≈ $0.004 comp + $0.04 place
- Key drivers:
  - Performance targets and
  - Assembly cost

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Example Cases

- 4" x 8" PCB
- Ten IC's 70pH L_{TGT}
  - 22mOhms @ 50MHz
- 2 routing layers
- $2.00/sq ft FR406 / layer pair
- $5.00/sq ft HK04™ / layer pair
- $0.001 / cap 0402
- $0.03 / cap X2Y™
- $0.015 / cap assy

Costs	0402			X2Y	
	4 lyr	6 lyr		6 lyr	
	Bottom	4 mil top	1 mil top	4 mil top	1 mil top
PCB	$0.89	$1.33	$2.66	$1.33	$2.66
Capacitors req'd	260	110	80	30	20
Cap. mat'l	$0.26	$1.10	$0.08	$0.90	$0.60
Cap. assy	$3.45	$1.65	$1.20	$0.45	$0.30
Total	$4.57	$4.07	$3.94	$2.68	$3.56

Table 1, Example Two Signal Routing Layer Costs

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Example Cases

- 4" x 8" PCB
- 4 routing layers
- 12 ICs 50pH L_{TGT}
  - 15mOhms @ 50MHz
- $2.00/sq ft FR406 / layer pair
- $5.00/sq ft HK04™ / layer pair
- $0.001 / cap 0402
- $0.03 / cap X2Y™
- $0.015 / cap assy

Costs	0402			X2Y	
	6 lyr	8 lyr		8 lyr	
	Bottom	4 mil top	1 mil top	4 mil top	1 mil top
PCB	$1.33	$1.78	$3.11	$1.78	$3.11
Capacitors req'd	444	240	144	72	36
Cap. mat'l	$0.45	$0.24	$0.15	$2.16	$1.08
Cap. assy	$6.66	$3.60	$2.16	$1.08	$0.54
Total	$8.44	$5.62	$5.42	$5.02	$4.73

Table 1, Example Four Signal Routing Layer Costs

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Conclusions

- Power distribution focus is managing inductance
- PCBs are locally inductive from low frequencies
  - Transition frequency independent of plane shape
  - Inductance proportional to thickness
- Thinner dielectric allows more inductance in bypass cap network, IE fewer caps
- In many low-cost constructions, total manufactured cost can be minimized through use of:
  - More material – take 4 to 6 layer, or 6 to 8 layer w/ glass / resin cavities
  - More expensive raw materials – using 1 mil polyimide (DuPont Interra HK04®), or epoxy (Oak/Mitsui BC24®) dielectric in place of 4 mil glass / resin
  - Lower inductance capacitors such as X2Y™
- Thinner cavities offer other performance benefits, but here we are concerned only with cost and presume function can be realized w/thick cavities
- Actual results depend on IC L_{TGT} and assembly cost per capacitor
  - Know your requirements!
  - Know your costs!

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