Measurement and Comparative S21 Performance of Raw and Mounted Decoupling Capacitors

Summary

All IC power systems require some level of passive decoupling. The ability to accurately predict in-system capacitor performance is critical to reliable power system design. We present methods to readily obtain both raw device, and practical in-system performance for any capacitor of interest.

Introduction

Decoupling capacitors perform a lowly, but critical system function. An accurate understanding of capacitor performance is necessary to realize any quality power distribution system. We demonstrate reliable methods to obtain both raw capacitor performance and in-system performance through straightforward test fixtures.

Capacitors

A decoupling capacitor acts as a noise shunt, placing impedance across the power distribution network. Noise currents drawn from active circuitry impress across the overall PDS impedance, deflecting the supply voltage. Decoupling capacitors have typically served two purposes:

- Stabilization of DC power rails against active circuitry load transients
- Coupling of DC power rails to ground as digital logic signal returns

At high frequency, decoupling capacitor impedance is inductive. The number of capacitors needed to realize a given impedance is directly proportional to the mounted inductance. Performance and cost both benefit from optimization capacitor mounting inductance.

DC Power IC Cut-Off Frequency

For modern circuits, DC power stabilization requires holding power system impedance up to frequencies of 20-100MHz, depending on the active devices used. Looking into an IC power pins, package inductance, in-package and on-die capacitance together create a low-pass power filter. For practical reasons, this filter has a cut-off that is rarely lower than 20MHz and rarely higher than 100MHz. Lower frequency cut-offs demand greater and expensive in-package and on-chip capacitance. Higher frequency cut-offs require massive increase to the number of power and ground pins that are a necessity, but by themselves provide no direct application value.

Similarly, were an IC manufacturer to significantly raise the PDS cut-off frequency, they would drastically raise the cost of their packaging, and also place a very expensive demand on the PCB power system. Beware the ASIC or ASSP supplier who knows little, and/or is willing to disclose little about the impedance versus frequency requirements of their parts. This is a recipe for disaster. A power system is very difficult to substantively modify once boards have been built. Find out what your devices need early in the design process.

Return Signal Coupling

High-speed logic signals contain frequency spectra according to both the signal repetition rate and signal rise / fall time. Common practice for many years has been to use DC power rails as signal returns. When rise times were slow, this was a good reuse of valuable copper consumed by power planes. In an era of 10-100ps rise times, it is an invitation to EMC headaches that have very expensive solutions such as a lot of Buried Capacitance (BC)[1], or no solution at all.

There are methods to extend the frequency response of boards, including distributed edge termination, among others[2].

The upshot is that successful decoupling design begins with an architecture for both power and signaling at the start. From that architecture, the power distribution impedance versus frequency requirements can be found. Against those requirements we map the mounted capabilities of our chosen decoupling capacitors. The focus of this article is determining capacitor capabilities before schematic capture.

Raw Capacitor Performance

All capacitors include a certain amount of intrinsic inductance. The mounted inductance limits performance at high frequency. The mounted inductance consists of two parts:

- Raw component inductance
- Attachment inductance

Our first task is to extract the raw parameters for any prospective capacitor. Once we know what the capacitor can do in an ideal environment, then we will be able to evaluate trade-offs in mounting and grouping.

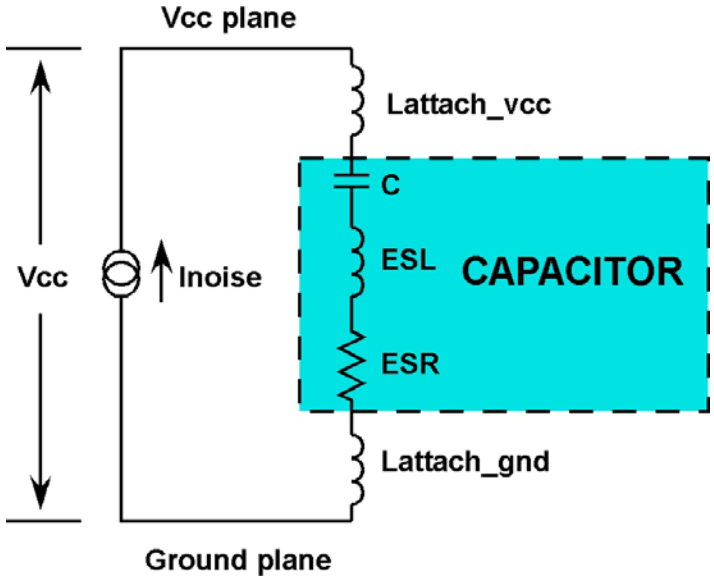

Figure 1. SPICE Model, mounted decoupling capacitor

We can effect accurate raw device measurement with a simple microstrip fixture for each capacitor type we are interested in. The fixture for each capacitor consists of two SMA connectors with a 50 ohm microstrip connection to the DUT. Near the DUT the 50 ohm microstrip impedance is discontinuous. The smaller the fixture, the smaller the discontinuity and more accurately the fixture reports high frequency performance. With little effort, capacitor performance to 300MHz and beyond is easily attainable. S21 insertion loss may be measured with almost any VNA such as an Agilent 8712.

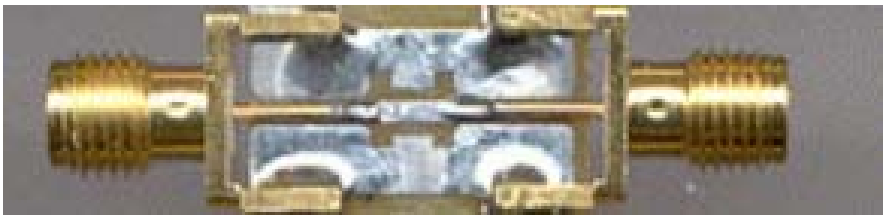

Figure 2. Example microstrip test fixture

Here, we show an example fixture for X2Y 1206 capacitors. The fixture is just large enough to provide the SMA connections and the capacitor attachment.

Extracting the Capacitor Parameters

The idealized model of the test set-up is as shown in Figure 2.

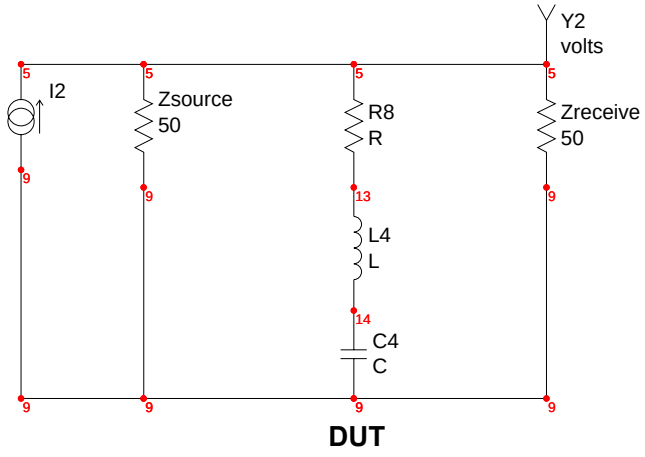

Figure 3. SPICE Model, Microstrip Fixture

First calibrate the VNA using the test fixture with no capacitor soldered in. Then solder the capacitor and collect S21 parameters.

The voltage amplitude in dB is:

$$S21dB = 20*Log_{10} * Z_{DUT} / (Z_{DUT} + 25)$$

Solving for Z_{DUT}:

$$Z_{DUT} = 25 * 10^{(S21dB / 20)} / (1 - 10^{(S21dB / 20)})$$

Insertion loss for a capacitor follows a 'V' curve. MLCC capacitors have high Q's and consequently steep inflections near the SRF.

For a simple series R-L-C:

$$Z = \sqrt{(ESR^2 + (Z_C - Z_{ESL})^2)}$$

At the SRF the inductive and capacitive reactances cancel, leaving only the ESR.

$$ESR = 25 * 10^{(S21dB\_MAX\_LOSS / 20)} / (1 - 10^{(S21Db\_MAX\_LOSS / 20)})$$

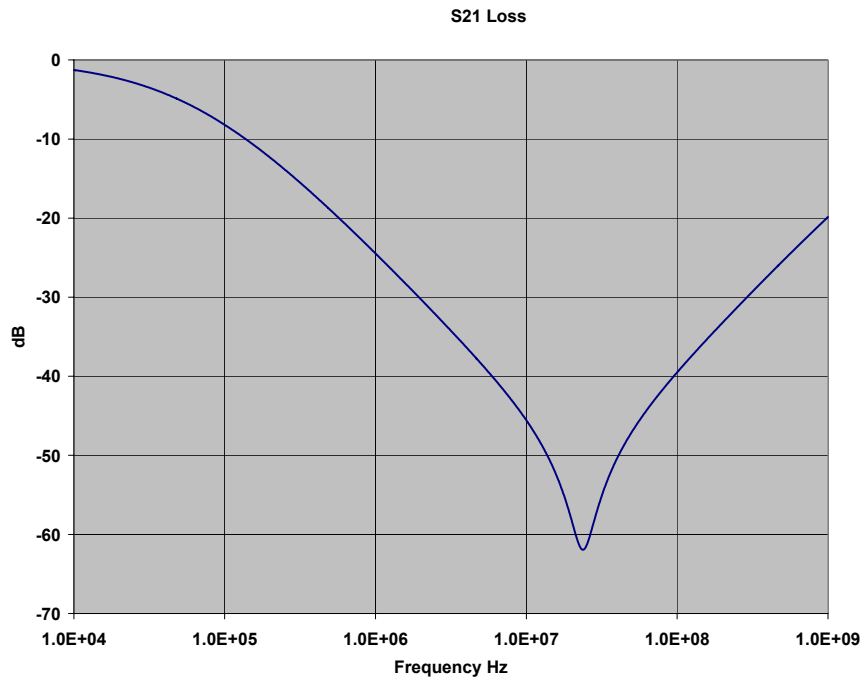

Figure 4. Insertion Loss, Typical 100nF MLCC

Once we have the ESR, then we can find the capacitance. The capacitance may be accurately obtained by solving the impedance equation at a frequency F1 well below the SRF, and noting that at the SRF, the capacitive and inductive reactances are equal, allowing us to substitute:

$$Z_{F1} = 25 * 10^{(S21dBF1 / 20)} / (1 - 10^{(S21dBF1 / 20)})$$

$$C = (F_{SRF}/F_1 - F_1/F_{SRF})/(2\prod * F_{SRF} * \sqrt{(Z_{F1}^2 - ESR^2)})$$

Once we have the capacitance, we can solve for the inductance based on the SRF as simply:

$$L = 1/((2\pi * F_{SRF})^2 * C)$$

The advantage of this extraction method is that it minimizes errors due to stray inductance in the test fixture, and provides a repeatable and accurate measurement.

Additional details on this extraction methodology may be found on the X2Y website: www.x2y.com application note: "#3004 - Accurate Capacitor Inductance Extraction from s21 Measurements"

Raw Device Results

Typical results for several popular devices are shown.

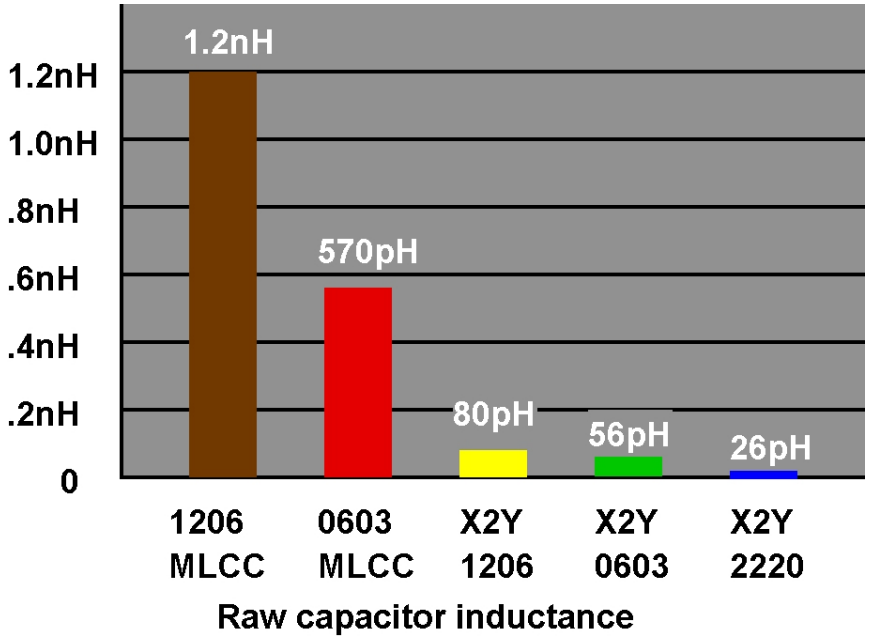

Figure 5. Example Extracted Inductance

Here we see that an X2Y capacitor exhibits 1/10th or less the inductance of its MLCC counterpart. In PCB applications that use microstrip layout configurations, this would allow us to get away with only 1/10th the number of decoupling capacitors. In configurations that use vias, the attachment inductance[3] and PCB layer stack up[4] used reduces the gain.

Mounted Inductance Measurement

Our end objective is to predict performance in real systems. The capacitor attachment, and power distribution plane arrangement has as much effect on the decoupling performance as the capacitors themselves. The evaluation process is similar as with the microstrip test boards, except that now a multilayer board representative of the board construction of interest is used.

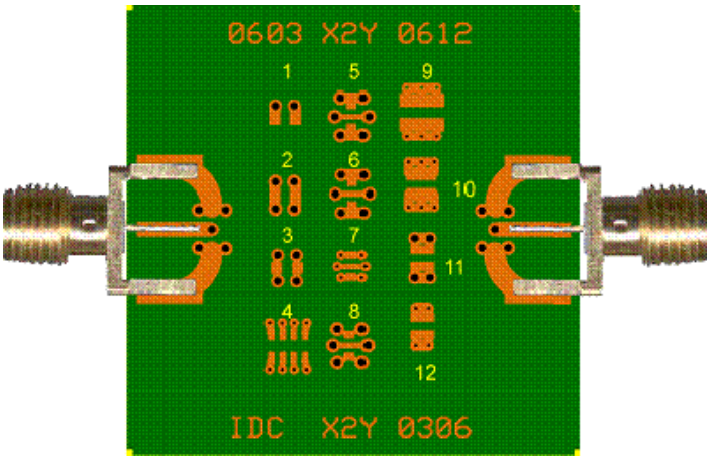

Figure 6. Example Test Fixture

For accurate measurements:

- Keep overall board area to a minimum, this sets the highest board SRF and minimizes result coloring due to plane capacitance.
- A good size is a square section that separates the SMA connectors by about the size of the largest BGA that will be used in designs with comparable board construction.
- Mount capacitors near the middle of the test board. Spreading inductance has little effect, especially on thin planes for capacitors mounted somewhat off-axis. This facilitates using one board to evaluate 9-12 different types of capacitors with minimal error.

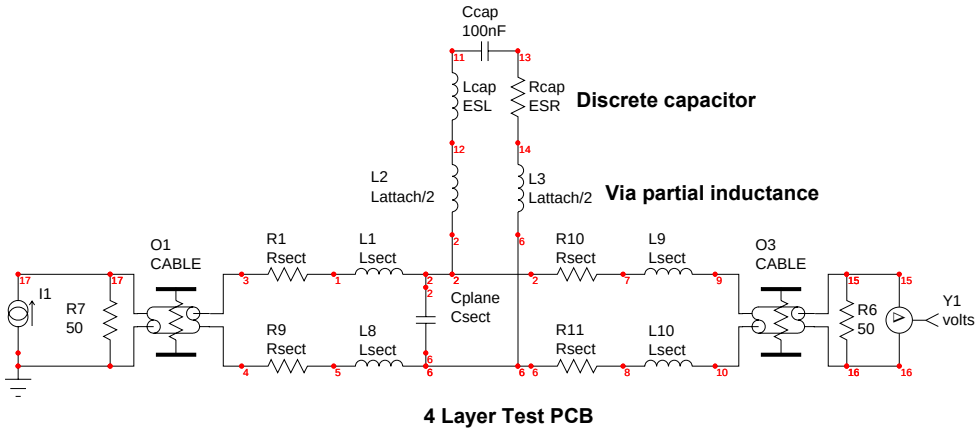

Figure 7. SPICE Model 4 Layer Test Board

The measurement and extraction procedure is similar to that for raw parts on a microstrip board:

$$ESR = 25 * 10^{(S21dB\_MAX\_LOSS / 20)} / (1 - 10^{(S21Db\_MAX\_LOSS / 20)})$$

$$Z_{F1} = 25 * 10^{(S21dBF1 / 20)} / (1 - 10^{(S21dBF1 / 20)})$$

$$C = (F_{SRF}/F_1 - F_1/F_{SRF})/(2\pi * F_{SRF} * \sqrt{(Z_{F1}^2 - ESR^2)})$$

$$L = 1/((2\pi * F_{SRF})^2 * C)$$

Where F1 is a frequency significantly below the SRF. Typically, select F1 near SRF / 10.

Boards with multiple patterns provide easy means to experiment with several different mounting strategies to maximize the efficiency of the mount. Attachment inductance increases with any:

- Lateral distance from the capacitor pad to the attachment via.
- Length of the via tube to the respective plane.
- Plane separation.
- Proximity of like polarity vias / traces

Attachment inductance decreases wth:

- Increased via tube diameter
- Proximity of opposing polarity vias / traces.
- Additional vias

Some example measurements:

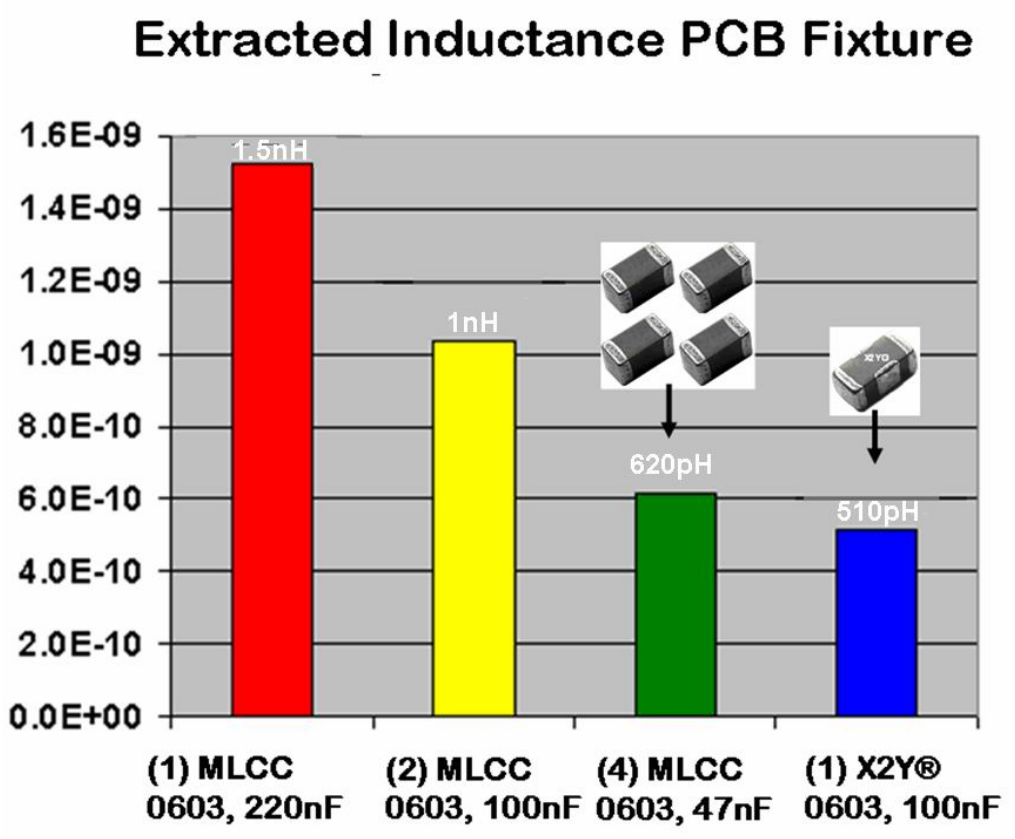

Figure 8. Extracted inductances of PCB mounted DUTs with like capacitance values.

Measurements using equivalent capacitances on a 0.062" thick 4 layer board demonstrate that a single mounted X2Y capacitor has 1/3 the inductance of an ordinary MLCC, and outperforms four MLCC s mounted in a cluster designed to minimize mutual inductance.

Plane spacing on these test boards is 0.038. Boards with thinner plane spacing increase the advantage of low inductance capacitors over conventional devices, resulting in even better gains using X2Y.

Practical application of these measurement techniques and results with FPGA PCB layouts bear-out superior results, replacing over one hundred conventional MLCC capacitors with fewer than one third as many X2Y capacitors. Test results and decoupling design methodology are covered in *High Performance FPGA Bypass Filter Networks*[5].

Conclusion

Capacitor high frequency performance is limited by the mounted capacitor inductance. Simple microstrip and four layer fixtures enable straightforward extraction of both raw device characteristics, as well as mounted device system performance. Using these methods comparison and assessment of the advantages of modern low inductance capacitors versus traditional decoupling methods can be accurately assessed. Complete board designs correlate well with test board measurements.

Note: Performance results reported in this and other application notes can only be achieved with patented X2Y® components sourced from X2Y® licensed manufacturers or their authorized distribution channels.

References

[1] Buried Capacitance™ Q&A

[2] Istvan Novak of SUN Microsystems , additional resources may be found in the SI-LIST archives: http://www.si-list.org/

[3] Understanding Capacitor Inductance and Measurement in Power Bypass Applications

[4] Impact of PCB Stack-up and Capacitor Via Design In Power Distribution Design, IEEE EMC Society SCV Meeting

[5] High Performance FPGA Bypass Filter Networks, DesignCon 2005, DesignCon 2005, Jan 31 Feb 3, Santa Clara, CA

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