Bypass Capacitor Inductance, Data Sheet Simplicity to Practical Reality

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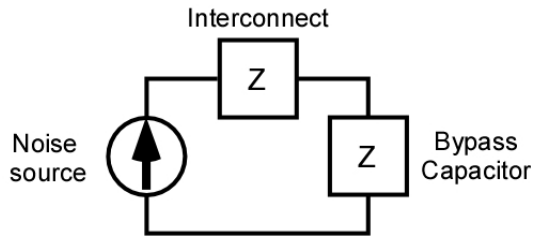
Bypass Capacitors in Power Delivery Systems

- Bypass capacitors provides a shunt path for noise currents.
- Capacitors become inductive beyond the SRF.
- Effectiveness falls off ideally by 20db / decade above the SRF.
- Interconnect between the noise source, and the capacitor affects capacitor performance.
- Single RLC capacitor model is a primitive device approximation



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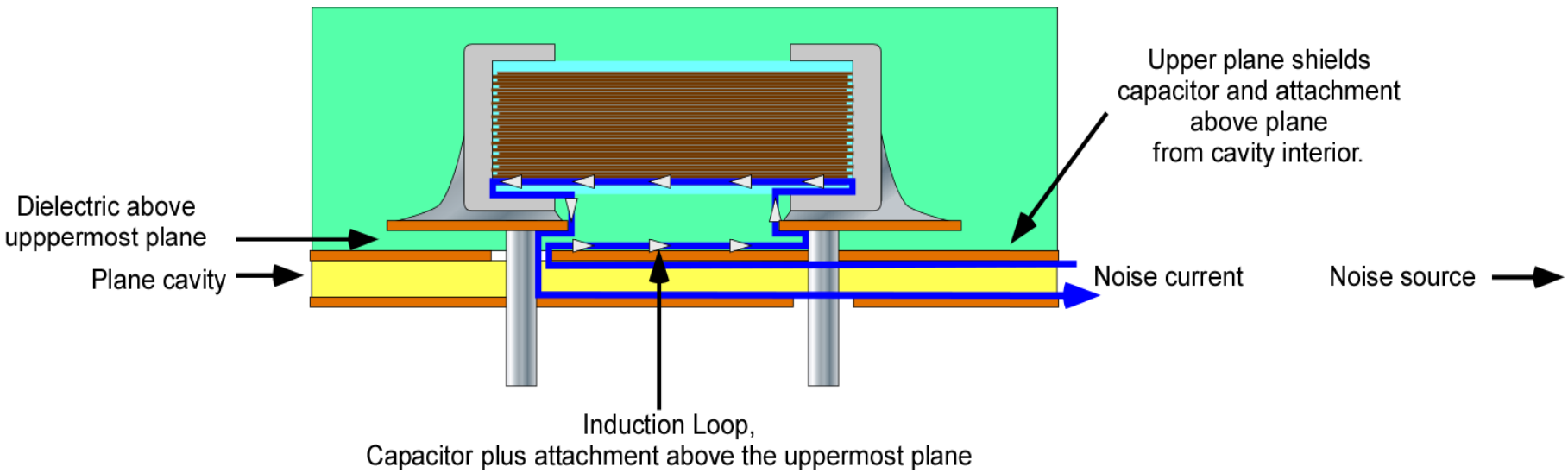
Partial Inductances???

- Inductance is the measure of the work function around a loop. The capacitor itself is only part of this loop.



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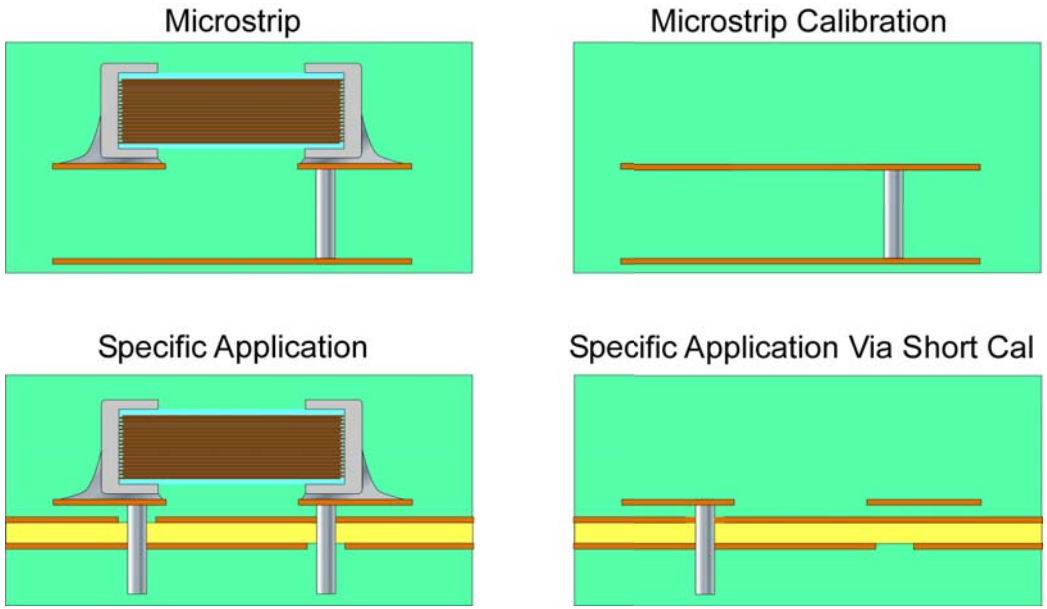
Which Inductance Is "Correct"?

- Difference of device versus a pad short in a microstrip?
- Device absolute in a microstrip?
- Difference between device and via short in a specific mounted configuration?
- Device absolute in a specific configuration?



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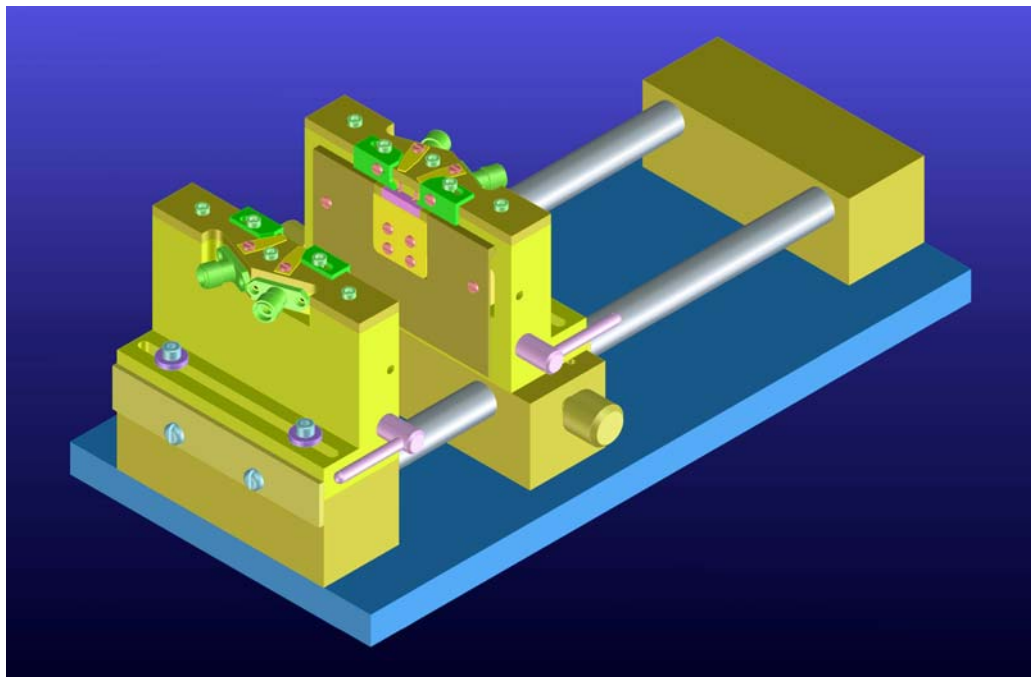
"Device Only" Measurements

- An oxymoron, but potentially useful if approached with care
- Really means **consistent and repeatable** measurements, typically in a CPW, or microstrip fixture.
- Intercontinental Microwave fixture is a good example.



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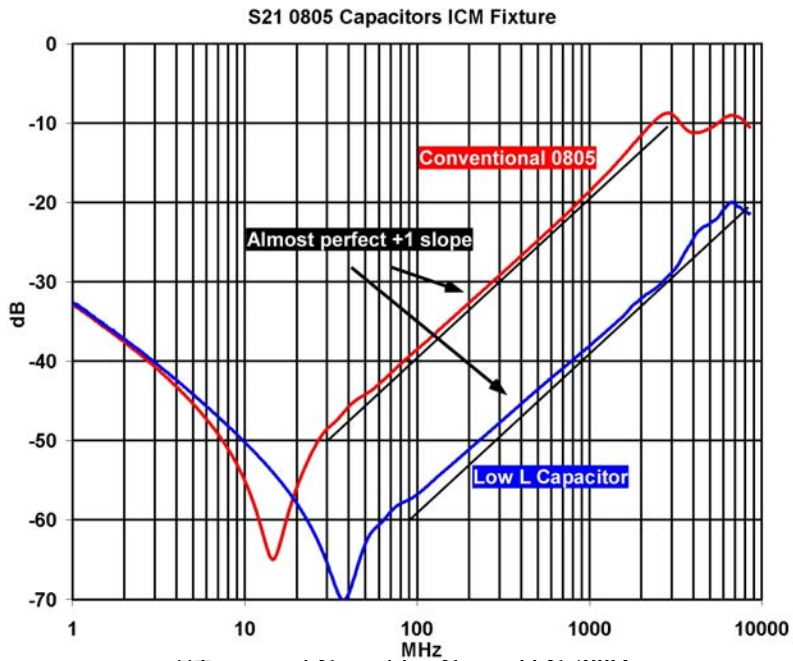
"Device Only" Measurements, Cont'd

- Tells us about loss, series and parallel combined, in a series filter configuration.
- The fixture only compares microstrip or CPW insertion loss.
- A quality fixture affords a view of relative, but not absolute performance that the capacitors will exhibit in a PDS application.



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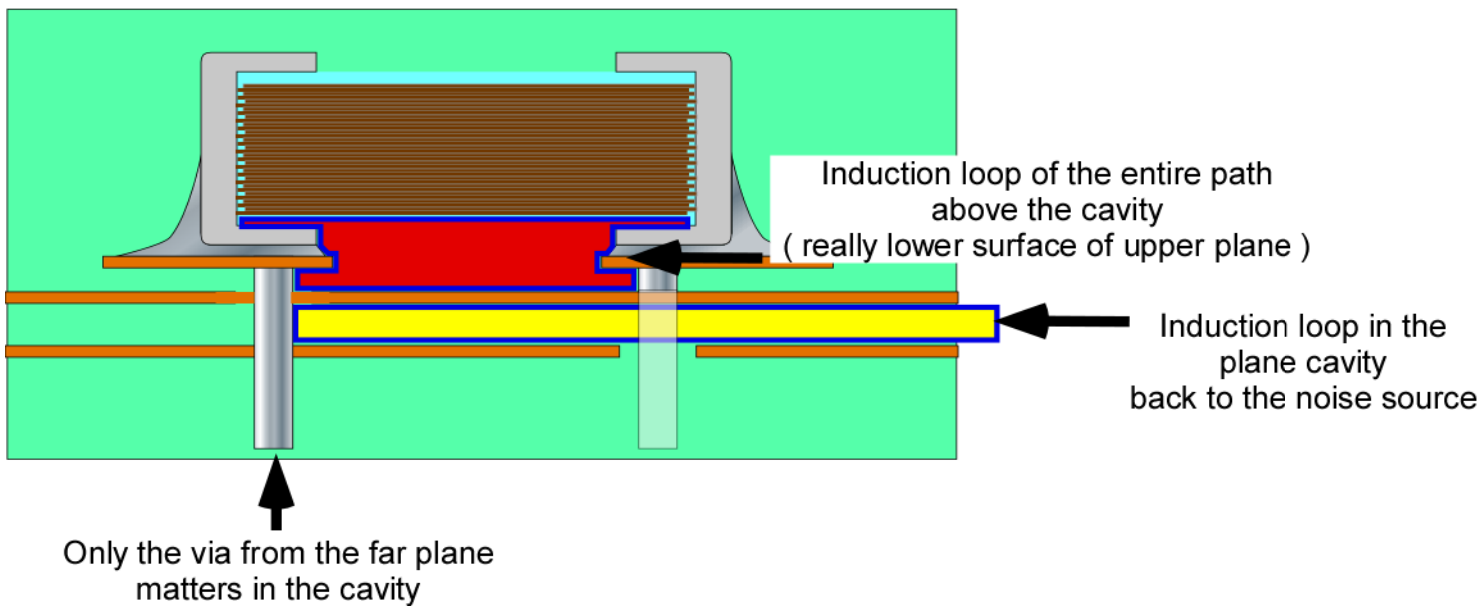
Plane Cavities and the Mounted Capacitor

- Planes make great RF shields above a few MHz.
- Above the cut-off there are two distinct induction loops:
  - From the noise source looking out to the via connecting to the bottom plane and its anti-pad.
  - Everything in the path above the lower surface of the upper plane.

Two Induction Paths in Series



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The Upper Induction Path

- The capacitor design AND the application define the upper induction path.
- Of nine variables three fall under direct vendor control:
  - Capacitor size,
  - Terminal configuration,
  - Bottom cover layer thickness,
- The remaining six are at least partially application defined:
  - Upper dielectric height,
  - Via count,
  - Via diameter,
  - Via separation,
  - Via offset from the capacitor pad and
  - Surface etch configuration

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The Upper Induction Path

- Far too many variables out of their control for a vendor to define
- Users can explore design space full 3D models
- Otherwise limitations on measurement space must be imposed.

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Analog Models

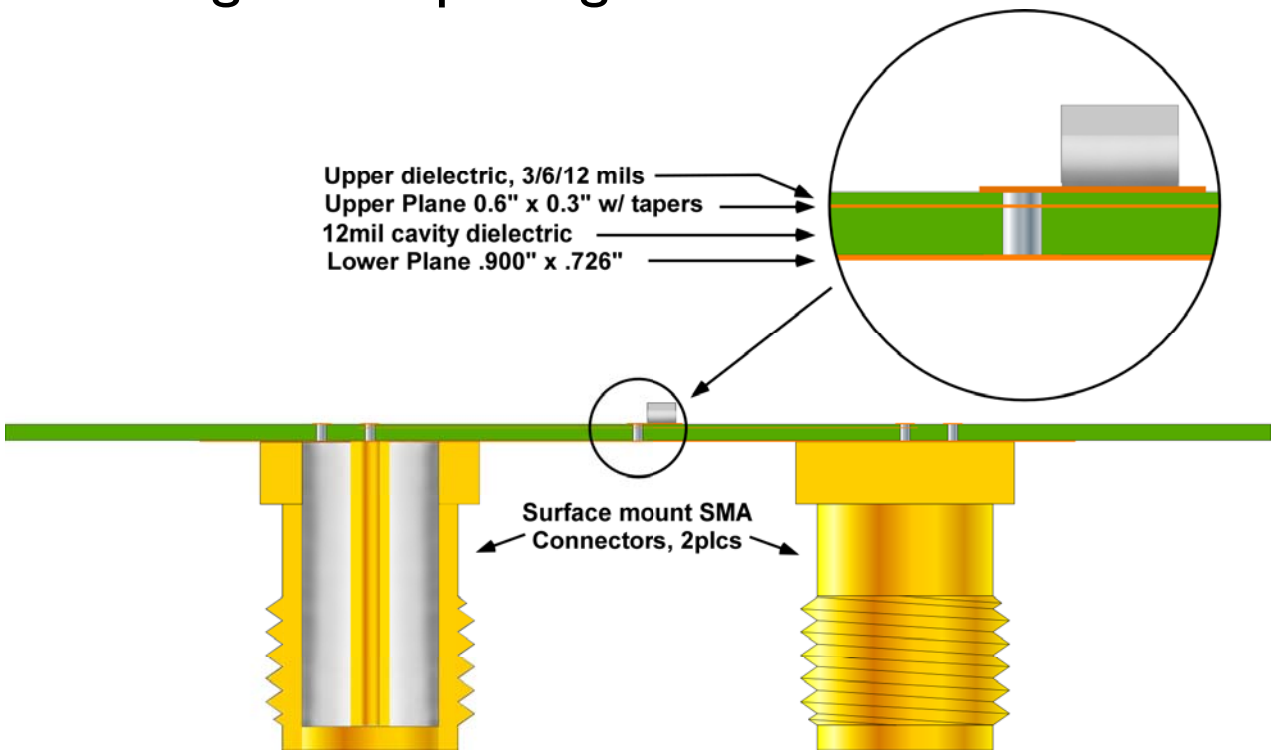
- Analog models seek to characterize behavior of one or more capacitors in a specific configuration.
- A well-designed analog can within a LIMITED range
  - Compare relative performance of two or more devices
  - Predict in-system performance for similar configurations as the vehicle.
- Examples: Intel Universal Capacitor Test Vehicle (DesignCon 2005)
- Good analogs require considerable care in design, data collection and interpretation

Good Analog Models

- Optimize device placement and orientation to the noise source for each DUT
- Optimize surface etch features for each DUT
- Optimize via: drill, pad and antipads for each DUT
- **EXACTLY** reproduce PCB stack-up above the uppermost plane in the cavity(s) bypassed by the DUT.
- Provide instrument / fixture deembedding.
- Ensure fringing does not introduce distortion.

SigCon / Teraspeed Fixture

- Joint fixture development between Dr. Howard Johnson, Signal Consulting, Inc, and Teraspeed, LLC.
- Suitable to evaluate bypass capacitors 1nF and larger from 0201 through 1812 packages.



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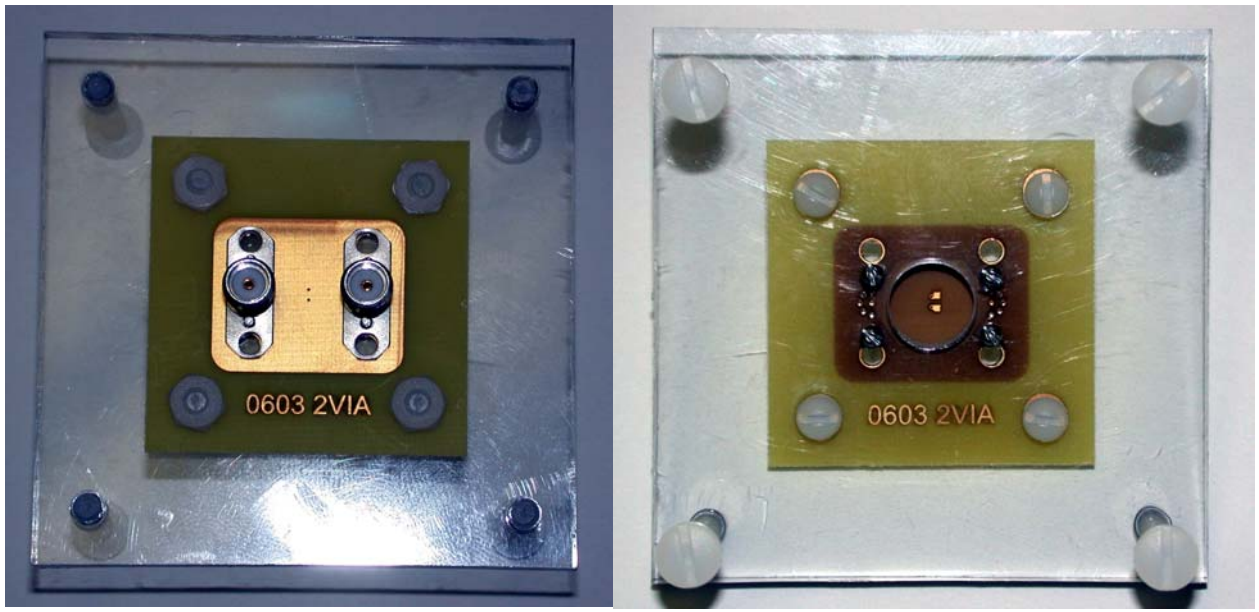
SigCon / Teraspeed Fixture



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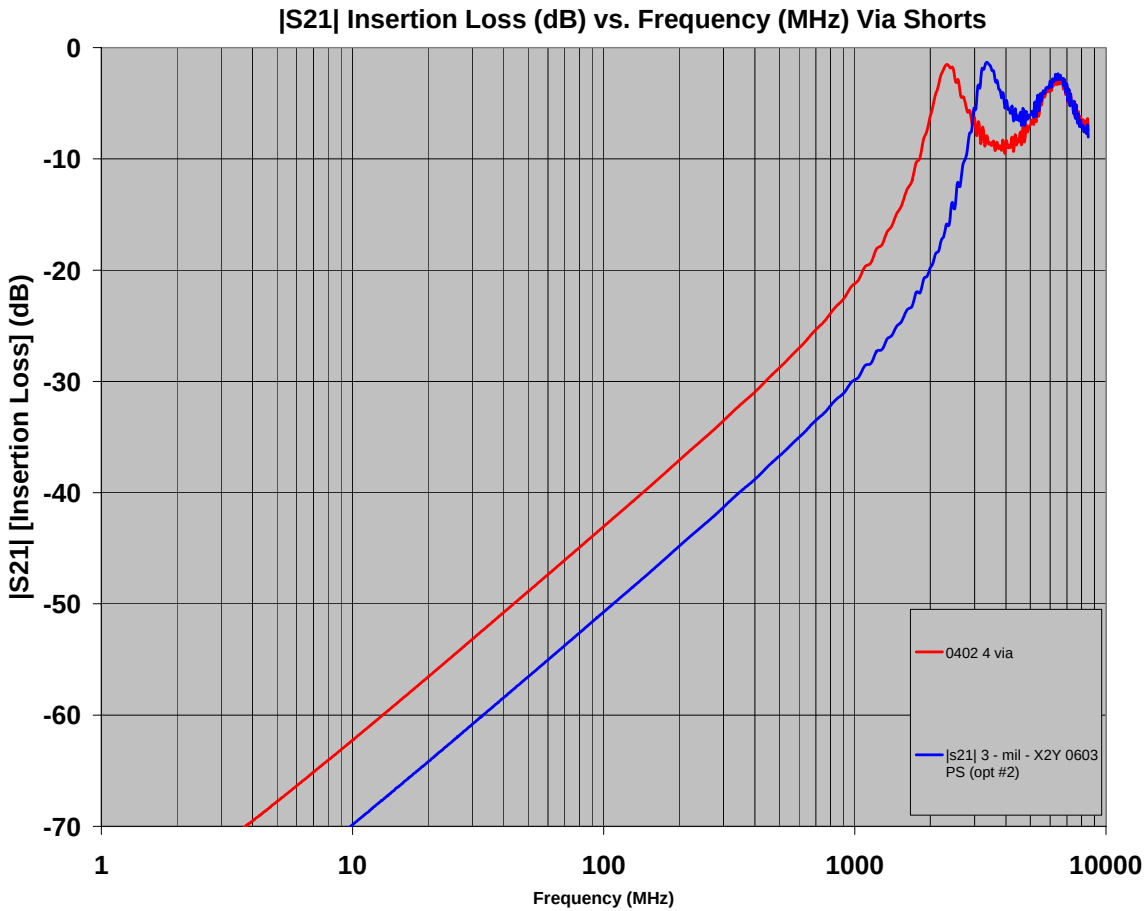
SigCon / Teraspeed Fixture

- The Good:
  - Low parasitic capacitance < 15pF
    - High plane / cap PRF >> 1GHz for 0402 caps
    - Little distortion up to 1GHz, and can be largely deembedded
  - Lower plane 1.5oz Cu effective shield from 2MHz up.
  - Includes via short and pad short sites to deembed instruments and cabling
  - Diamond test coupon limits modal resonances.
- The Bad:
  - SMA probe placement on either side of DUT doesn't fully match cantilever relationship of many noise sources.
- The Ugly:
  - Costly assembly. Separate fab for each upper dielectric height.

Example Results: 4Via 0402, 6 via X2Y 0603 Calibration Via Shorts



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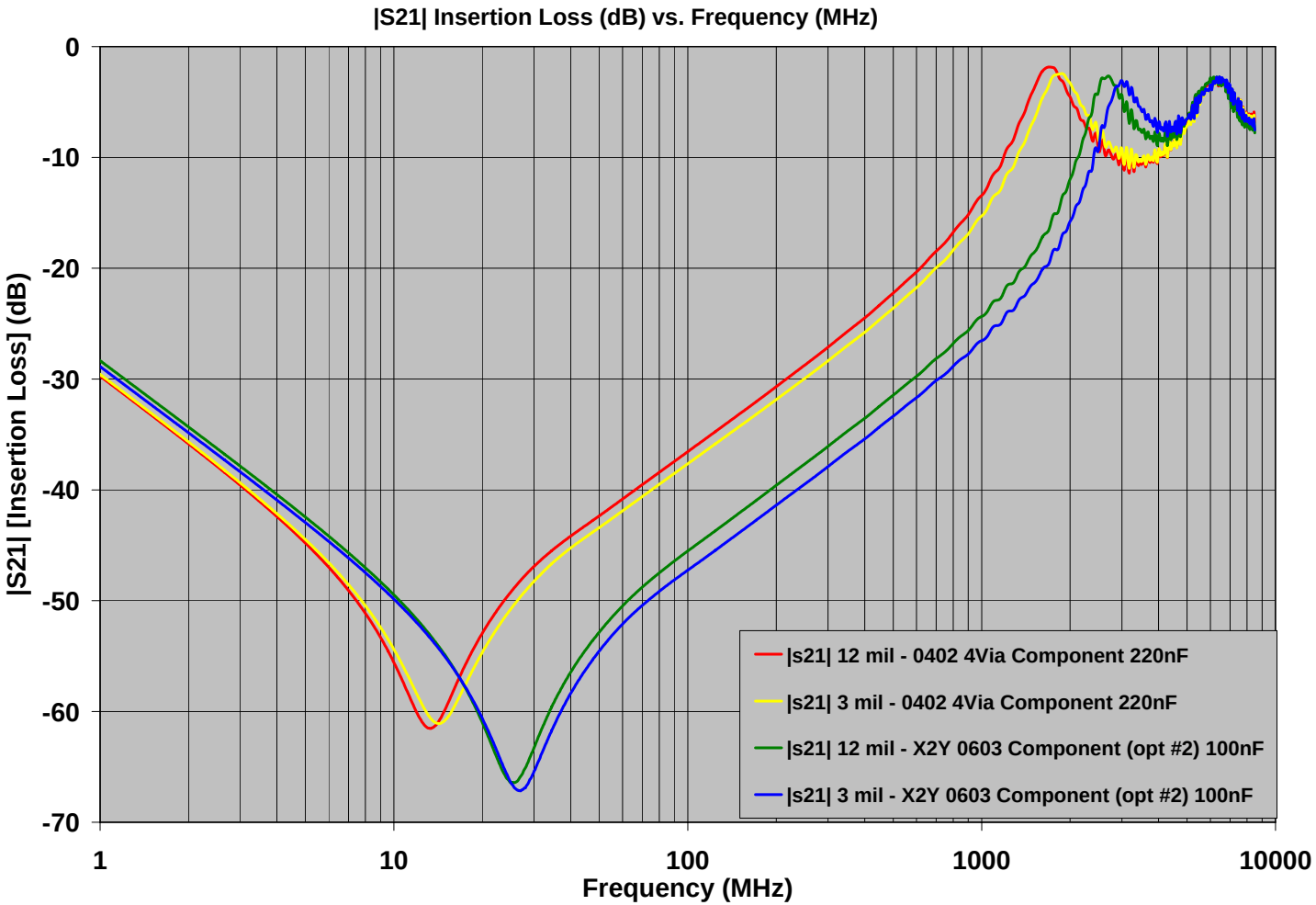
Example Results:
4Via 0402, 6 via X2Y 0603
3mil and 12 mil Upper Dielectric



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Conclusions

- Capacitor inductance is a misnomer:
  - Mounted capacitor loop inductance is what we want to know
  - Depends on both the capacitor design, and the application design: Where, what and how we mount.
- "Device Only" Measurements are valid for relative comparisons between devices
- Well-designed analog models or full 3D simulations can provide accurate numbers useable for bypass design