Accurate Capacitor Inductance Extraction from S21 Measurements

Summary

This application note details accurate extraction of ESR, capacitance and mounted inductance of decoupling capacitors.

Introduction

Decoupling capacitors operate as shunts to noise currents in power distribution networks. At high frequencies the impedance and therefore performance is limited by the mounted capacitor inductance. That inductance includes the partial inductance of the surface trace if any, vias, and plane separation.

We need to be particularly mindful of the attachment inductance if we wish to use low inductance capacitors such as X2Y's to full advantage. To this end, it is important to extract accurate models for each of the capacitor R-L-C values as well as the inductance of the capacitor attached in any particular board configuration we may wish to use. Here, we present a method to repeatably obtain reliable extractions, regardless of the capacitor type or attachment.

Decoupling Model

When comparing decoupling capacitors we ultimately deal with both the capacitor impedance and the attachment impedance to the power distribution system.

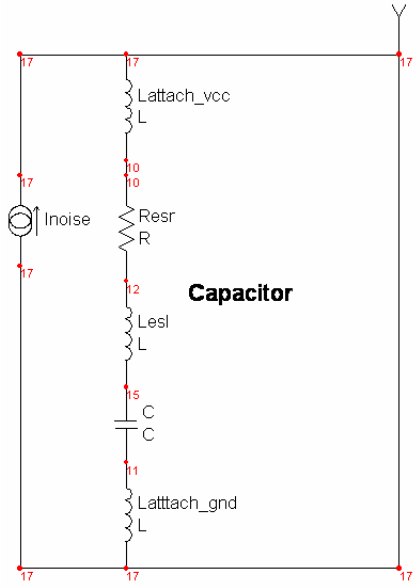

Figure 1. Attached Decoupling Capacitor Model

To find the device only parameters we start with a microstrip fixture. The fixture employs 50 ohm traces connecting the signal output port of a VNA at one end and the signal input port at the other as shown in this example:

Figure 2. Example Capacitor Test Fixture, X2Y 1206 Capacitor

Boards should be designed to maintain 50 ohms as closely as possible leading up to and away from the device under test. Make the board no larger than necessary to reduce the introduction of unwanted parasitics. Figure 2 illustrates a fixture used for X2Y 1206 evaluation.

Shunt Loss to Impedance Conversion

Whether measuring the device by itself, or in a representative board, the device appears as a shunt that loads the parallel VNA source and receiver as shown in this idealized model:

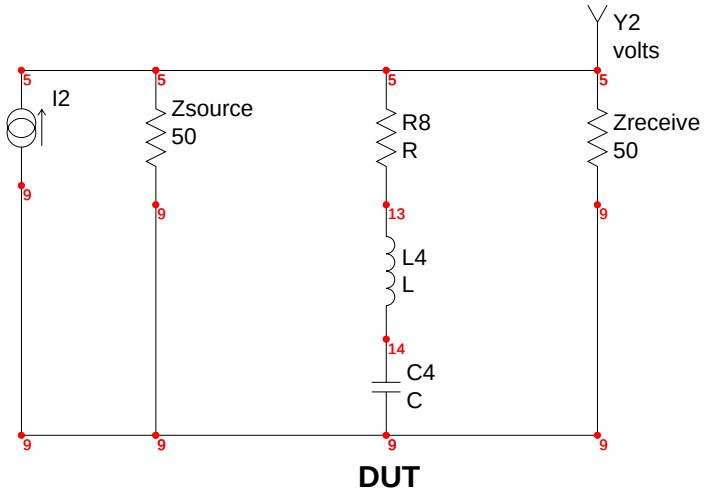

Figure 3. Shunt measurement model

The Norton equivalent of the VNA generator and receiver connected together is a 50 ohm source in parallel with a 50 ohm load, i.e. 25 ohms in parallel with the DUT shunt.

The voltage amplitude in dB is:

$$S21dB = 20*Log_{10} * Z_{DUT} / (Z_{DUT} + 25)$$

Solving for Z_{DUT}:

$$Z_{DUT} = 25 * 10^{(S21dB / 20)} / (1 - 10^{(S21dB / 20)})$$

For S21dB << 0, this is often approximated as in Pozar by:

$$Z_{DUT} = 25 * 10^{(S21dB / 20)}$$

For losses of 26dB or more, the approximation introduces less than 5% error and is useful for quick estimates. At low insertion losses, the approximation over reports capacitance, and under-reports inductance, leading to optimistic performance estimates. There is no particular need to use the approximation. For the sake of accuracy, we do not. We note it primarily to correlate with popular literature.

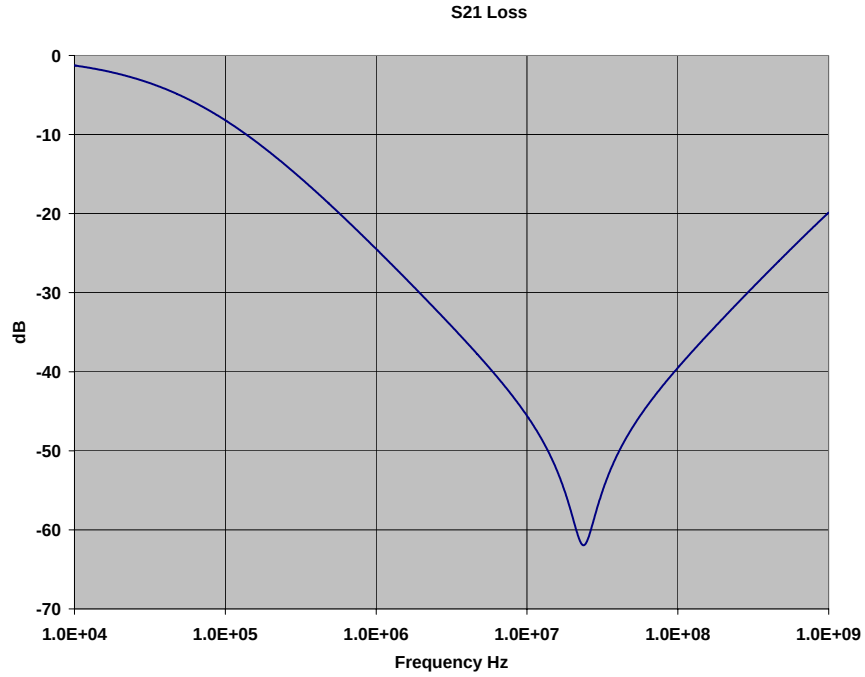

Figure 4. Example S21 Loss, 100nF 0603 Capacitor

ESR Extraction

For a simple series R-L-C:

$$Z = \sqrt{(ESR^2 + (Z_C - Z_{ESL})^2)}$$

At the capacitor SRF, $Z_C = Z_{ESL}$, leaving only the ESR:

$$Z = \sqrt{(ESR^2 + (Z_{C\_SRF} - Z_{C\_SRF})^2)} = \sqrt{(ESR^2)} = ESR$$

This results in the minimum impedance value, and maximum insertion loss. Consequently, we obtain the ESR from the impedance conversion at the point of maximum insertion loss:

$$ESR = 25 * 10^{(S21dB\_MAX\_LOSS / 20)} / (1 - 10^{(S21Db\_MAX\_LOSS / 20)})$$

Capacitance Extraction

At any frequency other than the SRF, the impedance results from all three components, ESR, C, and ESL. Since:

$$Z_C = 1/j\omega C$$

$$Z_{ESL} = j\omega ESL$$

Then for two frequencies F_{SRF}, and F_1:

$$Z_{C\_F1} = Z_{C\_SRF} * F_{SRF}/F_{1,}$$

$$Z_{ESL\_F1} = Z_{ESL\_SRF} * F_1/F_{SRF,}$$

Consequently, at some frequency F_1 significantly below the SRF:

$$Z_{F1} = \sqrt{(ESR^2 + (F_{SRF}/F_1 * Z_{C\_SRF} - F_1/F_{SRF} * Z_{ESL\_SRF})^2)}$$

And again since at the SRF

$$Z_{C\_SRF} = Z_{ESL\_SRF}$$

So:

$$Z_{F1} = \sqrt{(ESR^2 + (F_{SRF}/F_1 * Z_{C\_SRF} - F_1/F_{SRF} * Z_{c\_SRF})^2)}$$

Further substituting:

$$Z_{F1} = \sqrt{(ESR^2 + ((F_{SRF}/F_1 - F_1/F_{SRF}) * Z_{C\_SRF})^2)}$$

And solving for Z_C at the SRF:

$$Z_{C\_SRF} = \sqrt{(Z_{F1}^2 - ESR^2)}/(F_{SRF}/F_1 - F_1/F_{SRF})$$

And finally solving for C:

$$C = (F_{SRF}/F_1 - F_1/F_{SRF})/(2\pi * F_{SRF} * \sqrt{(Z_{F1}^2 - ESR^2)})$$

Inductance Extraction

Following the same logical substitutions for ESL:

$$Z_{F1} = \sqrt{(ESR^2 + ((F_{SRF}/F_1 - F_1/F_{SRF}) * Z_{ESL\_SRF})^2)}$$

And solving for Z_{ESL} at the SRF:

$$Z_{ESL\_SRF} = \sqrt{(Z_{F1}^2 - ESR^2)} / (F_{SRF}/F_1 - F_1/F_{SRF})$$

And solving for ESL:

$$ESL = \sqrt{(Z_{F1}^2 - ESR^2)}/((F_{SRF}/F_1 - F_1/F_{SRF}) * (2\pi * F_{SRF}))$$

This yields the same result as solving for L from F_{SRF} and C:

$$ESL = 1/(C * (2\pi * F_{SRF})2)$$

Effects of Fixture Parasitics

Any real fixture will have some parasitics, most notably a small amount of series resistance and inductance. The effect of these parasitics is to increase the insertion loss, particularly at high frequency. If we apply only the shunt formula:

$$Z_{DUT} = 25 * 10^{(S21dB / 20)} / (1 - 10^{(S21dB / 20)})$$

Increasing series impedance gives rise to artificially depressed Z_{DUT} values that overestimate the filtering capabilities of the DUT.

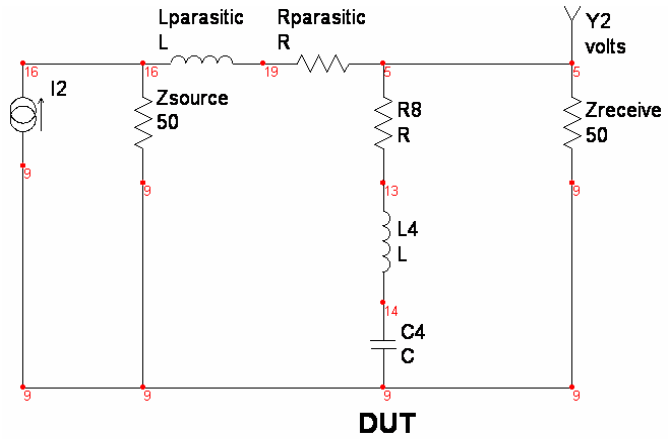

Figure 5. Fixture with parasitics

Fortunately, extraction based on the SRF is almost completely insensitive to fixture parasitics, particularly with high Q ceramic capacitors.

$L_{PARASITIC}$ and $R_{PARASITIC}$ both only slightly increase the parallel equivalent of Z_{SOURCE} and $Z_{RECEIVE}$. At the SRF, this introduces an insignificant error in the extracted value of R_{ESR}.

At the frequency, typically F_{SRF} / 10 where we extract both the capacitance and inductance, the magnitude of $L_{PARASITIC}$ is similarly much lower than even at $F_{SRF,}$ and the measurement is similarly unaffected.

Multilayer Board Measurements

At the end of the day we need to know the performance of decoupling capacitors on real-world boards. Via attachments add considerable inductance, and for low inductance capacitors, dominate the total inductance.

The procedure for multilayer boards is similar to microstrip. For these purposes, we can either construct a test board representative of the stack-up, or we can embed test access in a full-size board. Small test boards do not exhibit cavity resonance until several hundred MHz.

When dealing with decoupling measurements using common capacitor values resonances for even high K dielectrics on large boards are generally not a problem. This is because capacitor SRF for common values occurs well below quarter wave resonance of at least 30MHz, and this method only requires measured values up to and just beyond the mounted capacitor SRF.

Conclusion

This application note presents a straightforward and reliable method for extracting R-L-C parameters of decoupling capacitors for both raw parts, and parts mounted in real application conditions. Accurate capacitor characterization is particularly important to realize the full performance and economic benefits of low inductance decoupling capacitors. Accurate measurement data is only required up to and just past the device mounted SRF.

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