IC Decoupling and EMI Suppression using X2Y® Technology

Summary

Decoupling and EMI suppression of ICs is a complex system level engineering problem complicated by the desire for faster switching gates, size reduction, and the increasing requirements for more power at lower operating voltages. Generally in a power distribution system (PDS), decoupling is used to suppress transients across a broad frequency. EMI suppression is filtering of conducted and/or radiated noise emissions. Capacitors are the natural choice to perform this dual function. They are able to provide energy and the low impedance required for decoupling and EMI suppression.

Capacitors are used in a PDS to provide energy from kHz to MHz frequencies. Typically, there is less concern for low inductance in the kHz region, so larger electrolytic or tantalum capacitors are used to provide bulk energy. Developments in the last several years have yielded high-value ceramic capacitors that can provide the bulk energy more reliably than electrolytic capacitors and ceramics don't suffer the scarcity and high cost of tantalums dielectric components. However, these large body ceramics are sufficient mainly at kHz frequencies due to the parasitic inductance associated with their design and package size.

To improve the effectiveness over a larger frequency range the parasitic inductance for ceramic capacitors needs to be minimized. This is typically accomplished in three ways:

1. By making the package smaller, parasitic inductance is also reduced. On the other hand this also limits the number of electrode layers and therefore the capacitance value. The trade off is a part more useful at higher frequencies. For example, a capacitor with a 1206 package size is 0.12" x 0.10" whereas a 0603 package is half the size at 0.06" x 0.03", reducing inductance by half.

2. A reverse-aspect-ratio capacitor uses the longer dimensions of the package as terminations to reduce inductance. For example, a 0603 package capacitor has the terminations on the 03" side whereas a 0306 (reverse-aspect-ratio capacitor) is terminated on the 06" sides, again halving the inductance.

3. In order to provide the total amount of capacitance (energy) and still utilize smaller, lower inductive packaged capacitors, multiple capacitors in parallel can be used. The capacitors in parallel reduce the parasitic inductance and resistance while the capacitance is additive. For example, suppose the total needed capacitance needed for an IC is 1uf. Instead of using (1) 1uf capacitor, (10) 0.1uf capacitors in parallel would supply the

same 1uf of capacitance while reducing the parasitic inductance and resistance by 1/10th, at the sacrifice of board space.

As with anything in life, a solution to one problem may generate new ones. With the downward trend in the physical size of ICs along with greater power requirements at lower voltages (thus more decoupling is needed) placement of large number capacitors close to an IC (while maintaining proper spacing between capacitors) becomes impractical, if not impossible. (Several studies have shown that capacitors spaced too closely together degrade performance[1,2]).

The net result is the printed circuit board (PCB) is decoupled/EMI suppressed instead of the IC. The reality is the PCB is the path of power, not the source or receiver. By decoupling/EMI suppressing the path (PCB) several new parameters are introduced into the equation. Considerations such as trace and via inductance, large current loops, and the physical geometry of the PCB itself play a dominant role. These complex factors become the limiting factors in the PDS design, not the capacitors themselves.

Consider for a moment the following scenario, which places more emphasis on the capacitor as the limiting factor in the PDS:

- The IC power and return/ground pins are located next to each other. This helps to keep the current loop size to a minimum.

- Land pads for decoupling/EMI suppression capacitors are large enough for multiple vias to be used. By putting the vias in parallel, the parasitic resistance and inductance are minimized between the power planes and the capacitor.

In order for this scenario to work a physically large, low-inductance, large value capacitor is needed. This goes against the current design methodology that smaller is better (less inductive), so the question that arises is “Does a physically large, low-inductance, large value capacitor exist?”

This application note looks to illustrate through insertion loss (s-parameters) and impedance plots what X2Y® Technology has to offer in a large package, high capacitive value component for IC decoupling/EMI suppression.

Understanding the benefits of X2Y® Technology

X2Y® components should not be considered a discrete capacitive element, but rather a capacitive circuit capable of several connection configurations. The two main configurations are called Circuit 1 and Circuit 2, shown in Figure 1.

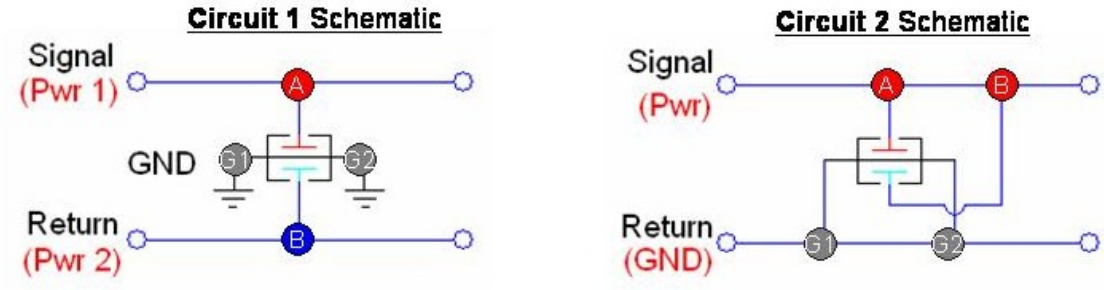


Figure 1. *Schematic of Circuit 1 and Circuit 2 configurations for an X2Y® component. (For more information on configurations see Application Note #1002.)*

Figure 2 and Figure 3 is an insertion loss and impedance plot respectively of a standard 0603 220nf capacitor, 0306 220nf reverse-aspect-ratio capacitor, and a 0603 100nf X2Y® component in the Circuit 2 configuration. (Note: 100nf X2Y® component is equivalent to 200nf total capacitance. For more information explaining the capacitive rating for X2Y® components see Application Note #3001.)

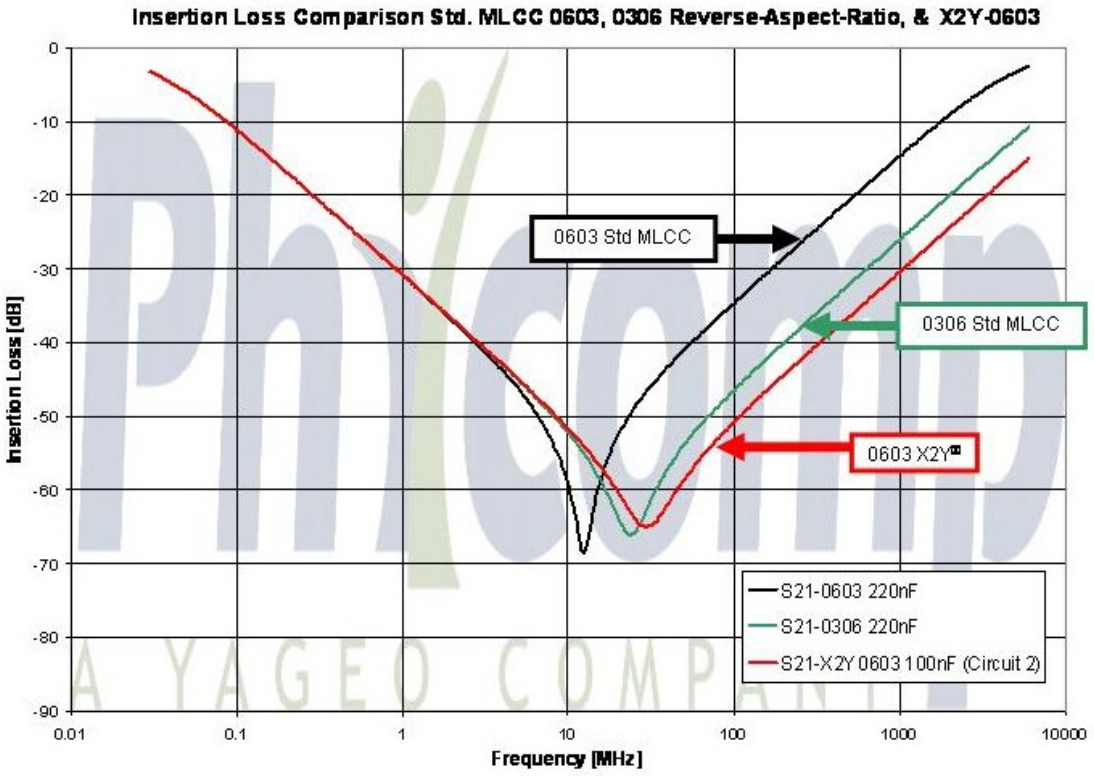


Figure 2. *S21 insertion loss plot of 0603/0306 components taken in a Wiltron Test Fixture. All component plots have 443 data points. Data courtesy of Yageo-Phycomp.*

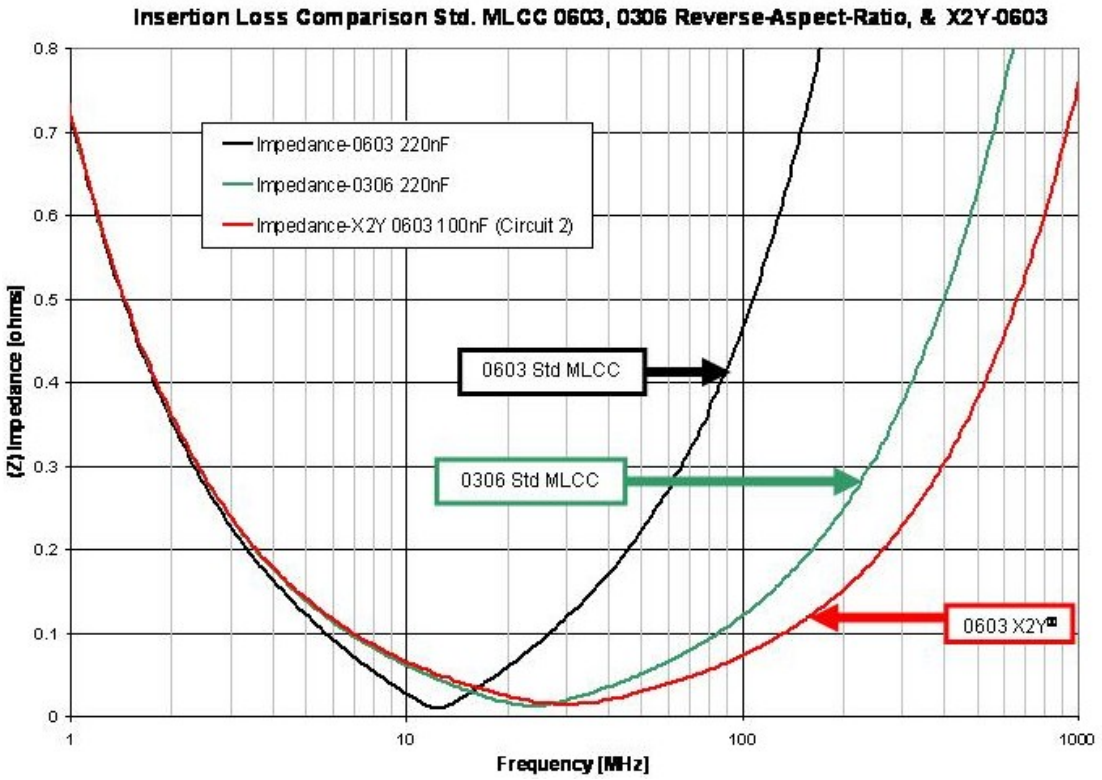


Figure 3. *Impedance conversion plot of 0603/0306 components (Figure 2).*

Both Figure 2 and Figure 3 show that the 0603 X2Y® component provides a substantial reduction in inductance/impedance. However, a 0603/0306 component cannot be manufactured in large bulk capacitive values. Several components would still be required and therefore would not offer a complete solution to the scenario. Yet, as stated earlier, the larger the component's package, the more inductive it is. Does this hold true?

Figure 4 and Figure 5 use the results in Figure 2 and Figure 3 to investigate the performance of an 1812 470nf (940nF of total capacitance) and 1uF (2uF of total capacitance) X2Y® component in a Circuit 2 configuration. One would expect both 1812 components to have more inductance/impedance than any of the 0603/0306 components.

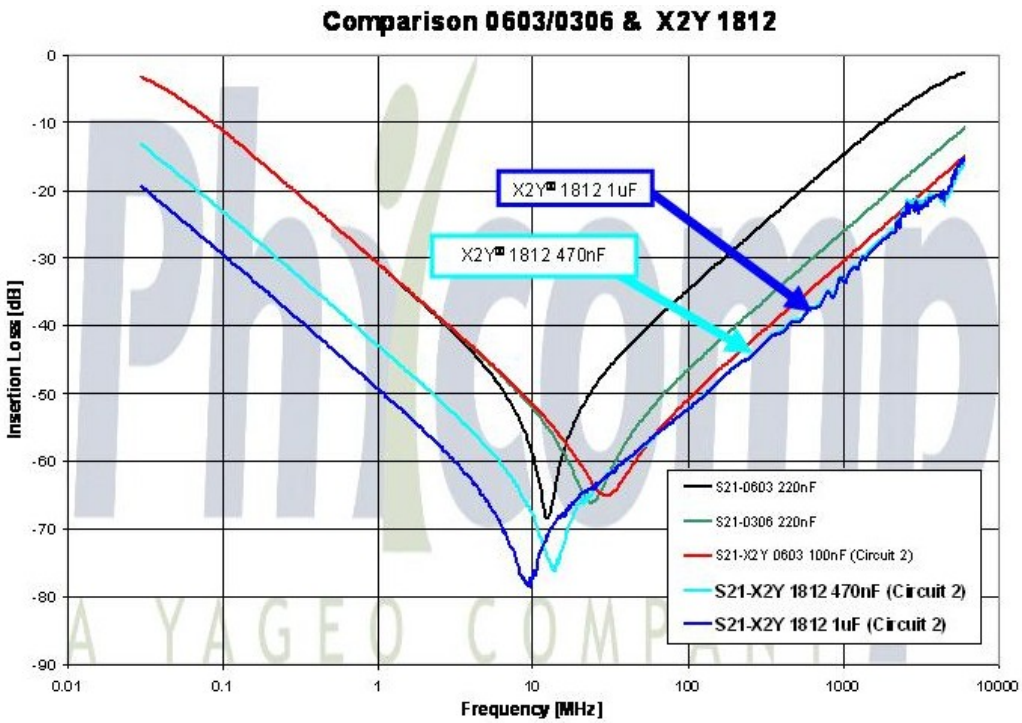


Figure 4. *S21 insertion loss plot of 0603/0306 components & 1812 X2Y® components taken in a Wiltron Test Fixture. The 0603/0306 component plots have 443 data points and the 1812 component plots have 801 data points. Data courtesy of Yageo-Phycomp.*

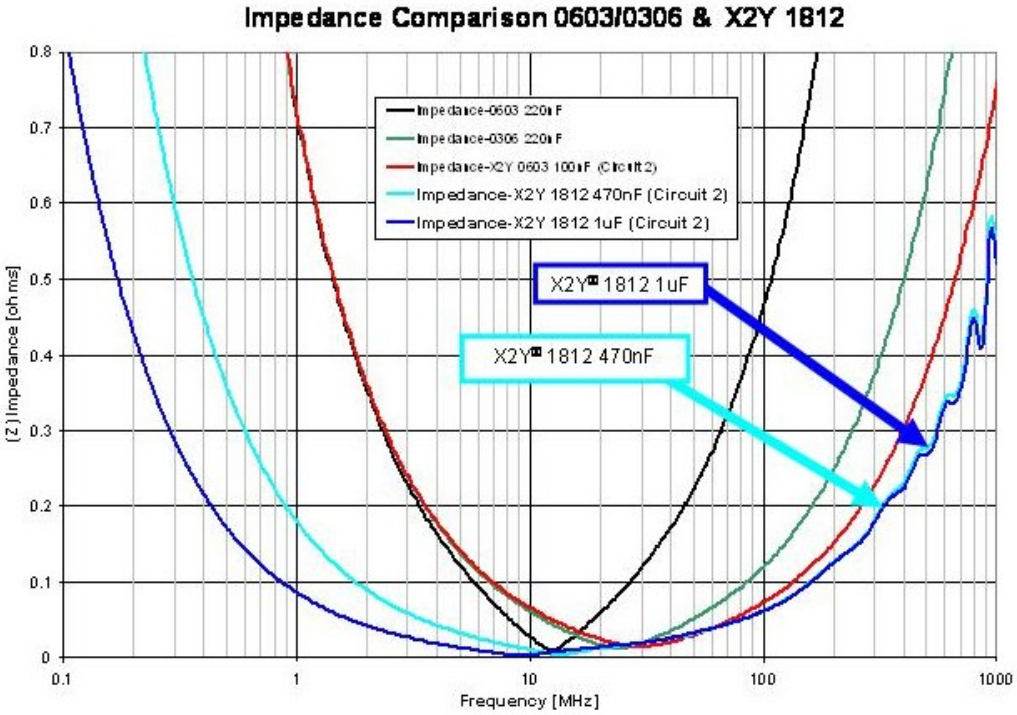


Figure 5. *Impedance conversion plot of 0603/0306 & 1812 components (Figure 4).*

Both the X2Y® 1812 components showed lower impedance than the even the best 0603/0306 (0603 100nF X2Y®) component, which contradicts expectations. The key to understanding the performance of the X2Y® Technology is the internal parallel structure. **For X2Y® components the more layers in the structure the lower the impedance, thus a larger package size is preferred.**

Up until this point, only Circuit 2 has been shown and discussed. Circuit 2 uses the X2Y® component more as a capacitive element than a circuit. As a result, the full advantage of the structure cannot be realized. (H-field cancellation is the predominant mode of cancellation for Circuit 2). Circuit 1, on the other hand, utilizes the structure for E- and H-field cancellation making it not only a capacitive element, but an effective passive cancellation circuit. The result is the reduction of the internal mutual inductance of the component. This not only improves the performance beyond resonance (high frequency), but the efficiency of the transfer of energy at low frequency.

(For more information on E- and H-field cancellation and the internal structure see Application Note #1002 & 1003).

Figure 6 is an insertion loss plot of the 1812 1uF X2Y® component in a Circuit 1 and Circuit 2 configuration.

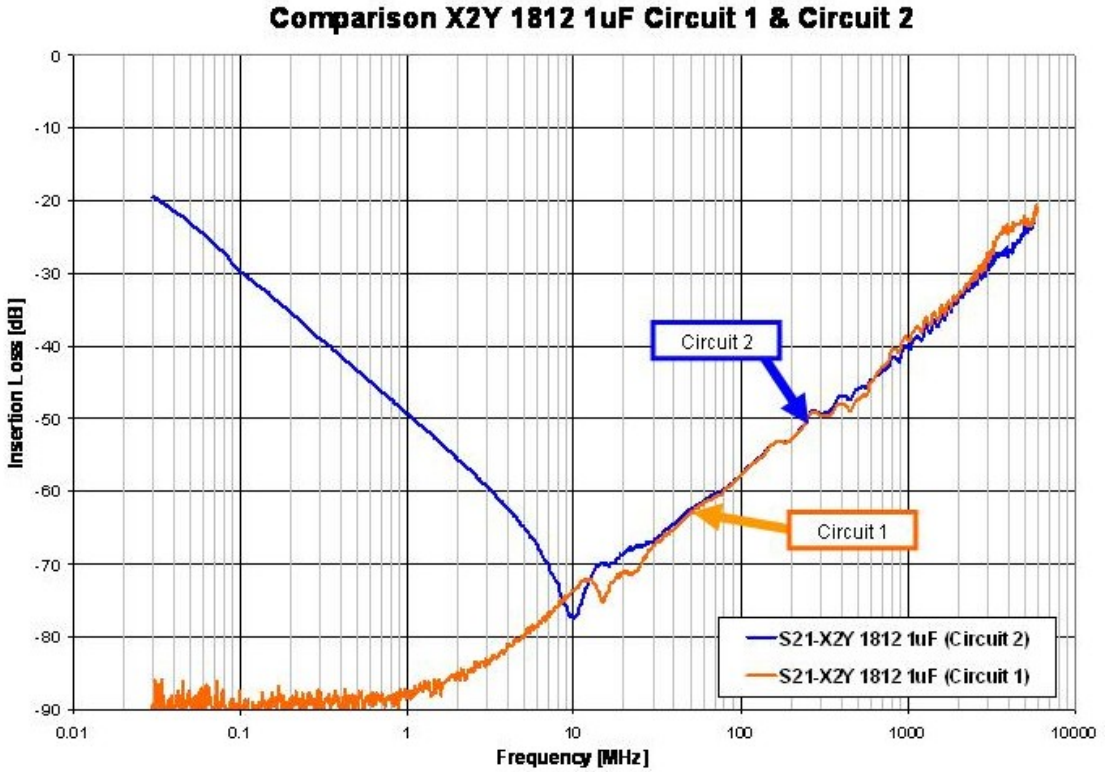


Figure 6. *S21 insertion loss plot of 1812 X2Y® 1uF in a Circuit 1 & Circuit 2 configuration. Circuit 1 and Circuit 2 were measured on a test PCB with a VNA. Each plot has 801 data points*.

Implementing the X2Y® Technology

This section provides a general overview of how to implement X2Y® components in an IC decoupling/EMI suppression application. Careful consideration should be made for proper placement and connection requirements. As shown in the previous section, Circuit 1 is the preferred connection that provides the greatest performance. Circuit 2 is the recommended alternative solution when Circuit 1 is not possible due to layout limitations. (For more information on Circuit 1 & Circuit 2 and proper attachment see Application Notes #1001 & 1002.)

Figure 7 depicts X2Y® components in a Circuit 1 configuration used to decouple an IC with a ball grid package mounted on a 3-layer PCB. This application allows for components mounted on both sides of the PCB. Note that multiple vias are used for each terminal of the X2Y® components. High frequency noise couples from the IC to the RF Image/Floating Plane. The RF Image/Floating Plane is used as a reference to passively cancel noise internal to the X2Y® components. (For more information on Image Planes see German, R. F., Ott, H. W., & Paul, C. R., Effect of an Image Plane on Printed Circuit Board Radiation, 1990 IEEE International Symposium on EMC, Washington, DC, 1990. http://www.hottconsultants.com/pdf_files/image_plane.pdf).

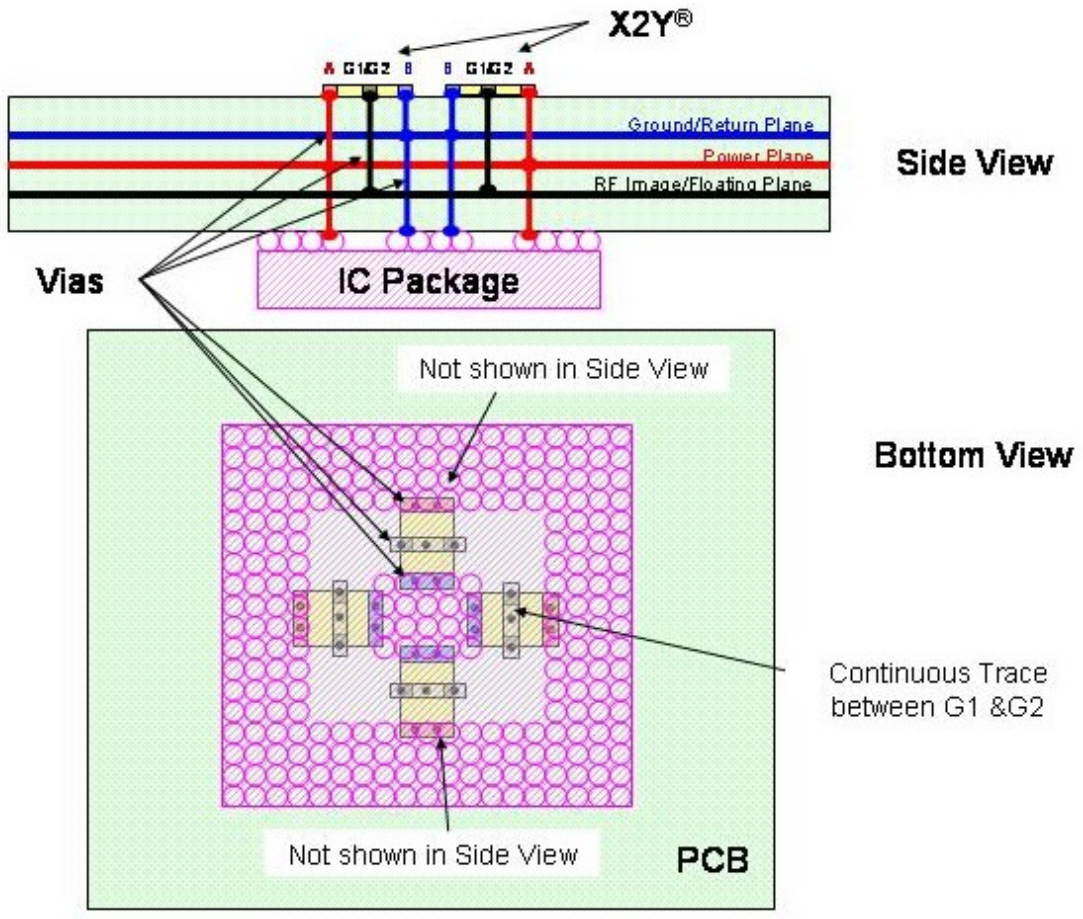


Figure 7. *Example, Circuit 1 implementation of X2Y® components.*

Figure 8 depicts X2Y® components in a Circuit 2 configuration used to decouple an IC with a ball grid package mounted on a 2-layer PCB. This application allows for components mounted on only one side of the PCB. Note that multiple vias are used for each terminal of the X2Y® components and that Figure 8 shows three different layout strategies depending on the appropriate package pin-out and layout options available.

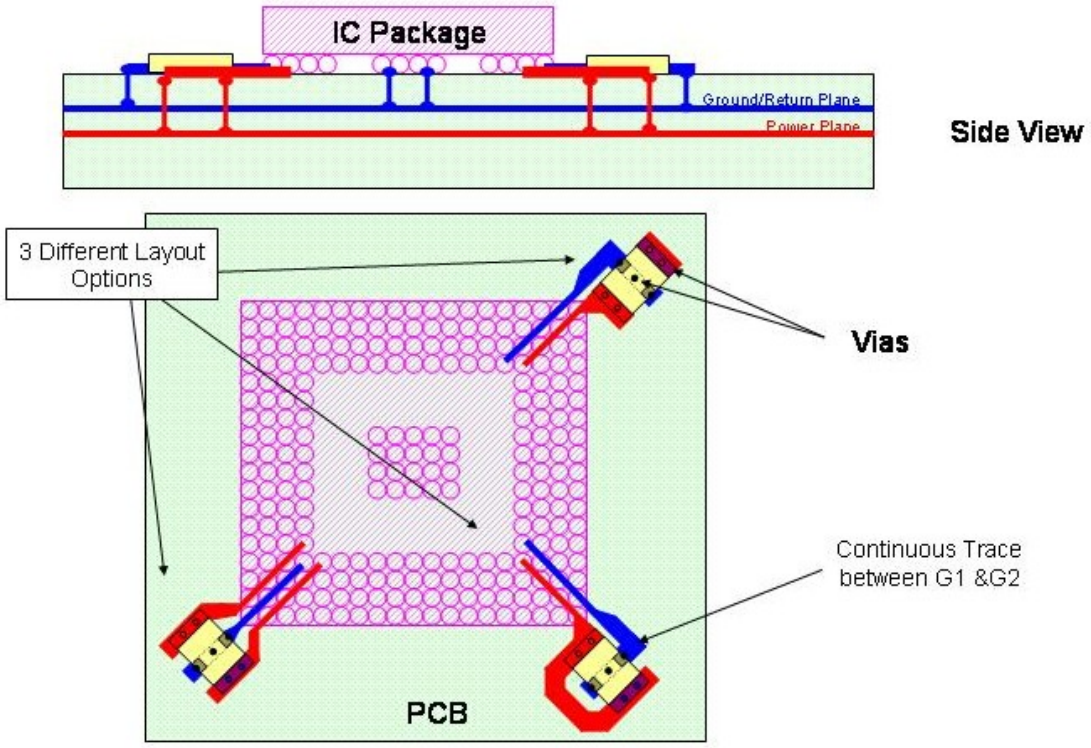


Figure 8. *Example, Circuit 2 implementation of X2Y® components*.

Figure 7 and Figure 8 provide the basic overview when implementing X2Y® components. As mentioned earlier, Circuit 1 is the preferred configuration (Figure 7). If the circuit is limited to a 2-layer PCB, but the application requires the extra performance that Circuit 1 offers, a creative attachment approach may be used. For example, mechanical structures that already exist in a packaged IC may provide the 'third layer' solution. Figure 9 shows a die mounted on a lead frame. The portion of the lead frame that the die resides on is there for mechanical reasons and is therefore electrically 'floating'. Note that the structure has 'leads' that extend at each of the corners.

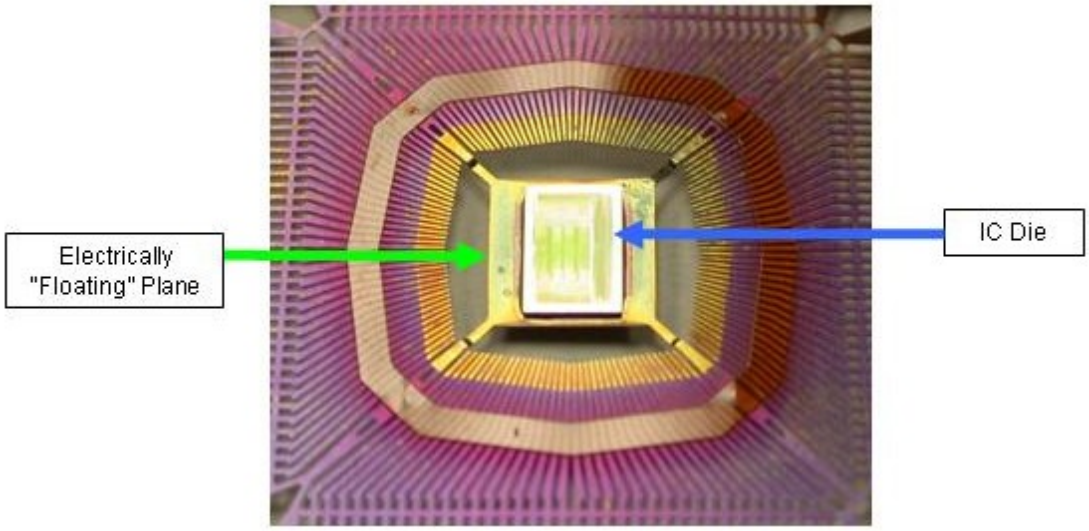


Figure 9. *Pre-packaged lead frame with IC die*.

The idea is to electrically connect the G1 and G2 terminals of the X2Y® component to the 'floating' portion of the lead frame and use it as a RF Image/Floating Plane. Figure 10 shows an actual IC where the corners have been grinded away with copper braid soldered to the exposed 'floating' portion of the lead frame.

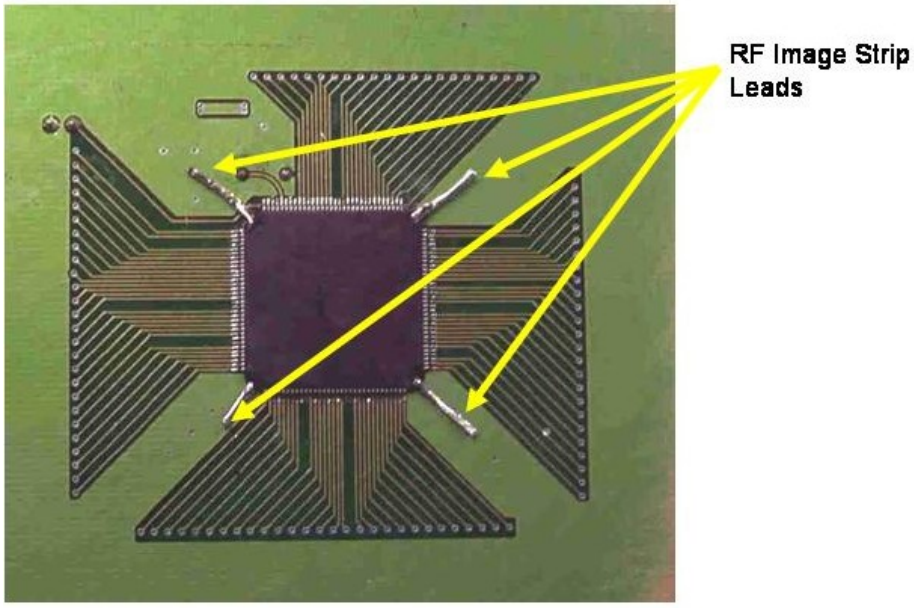
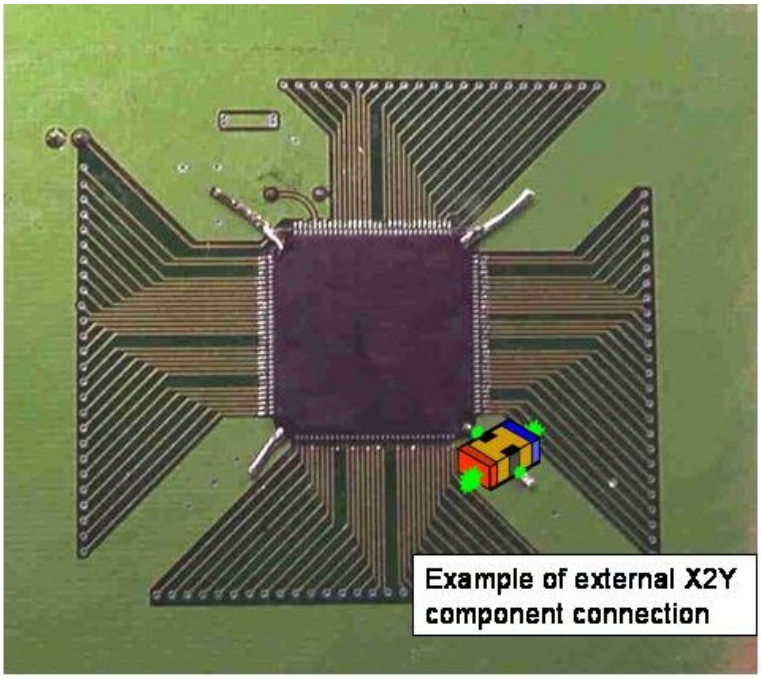


Figure 10. *Prototype microprocessor with soldered leads to package lead frame*.

If the power and ground/return pins are designated to corner pins, X2Y® components can be attached as shown in Figure 11. The same idea can also be applied to packages that utilize the heatspreader/heat plate/heatsink.



For optimum performance a low-inductance shorting or canceling device should be used between Pwr, GND, and Image Strip. The low-inductive device can be placed internally or externally of the IC package

Figure 11. *X2Y® attachment to Prototype microprocessor using lead frame as RF image plane*.

Building a Faraday Cage

To further provide EMI suppression a 'quasi' Faraday Cage can be constructed utilizing pre-existing structures. Structures such as heat sinks, image planes, lead frame, heatspreader, or heat plate can be used in combination to construct a Faraday Cage. The Faraday Cage should be referenced to the G1/G2 terminal and the A and B terminals connected across the power pins. Figure 12 and Figure 13 are two illustrations of such 'quasi' structures. Note when using the lead frame or similar structure as shown, the actual IC die should be orientated between the opposing structures of the Faraday Cage to maximize containment of the radiated fields.

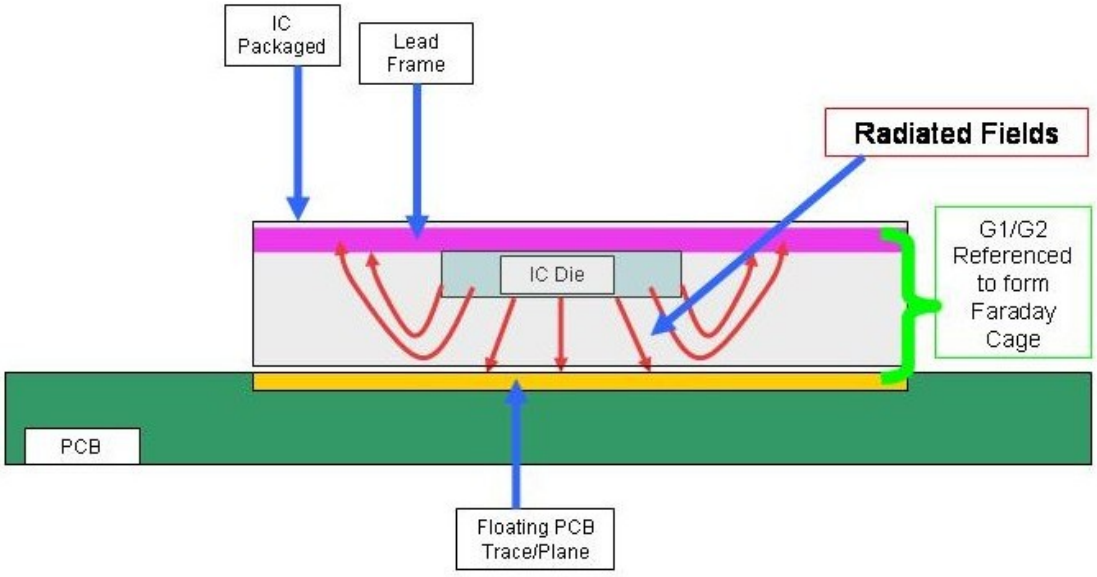


Figure 12. *Example 1 of pre-existing structures that can be made into a 'quasi' Faraday Cage.*

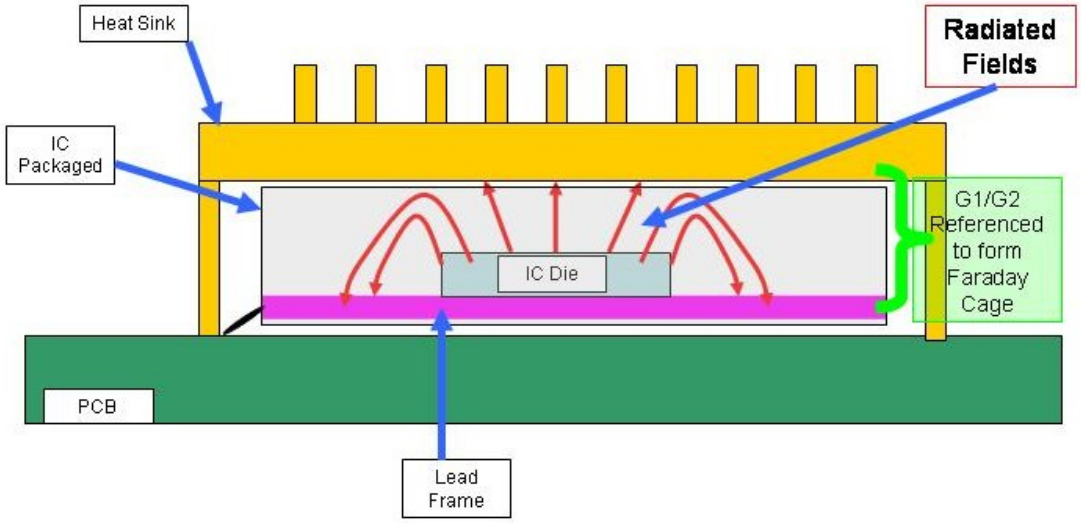


Figure 13. *Example 2 of pre-existing structures that can be made into a 'quasi' Faraday Cage. (For more information on using a Heatsink to build a Faraday Cage see Application Note # 2006.)*

Legal Patient Disclaimer

For more information on decoupling or specific questions unique to your applications, use the contact information at the end of this application note or visit us on the web, www.x2y.com.

The intellectual ideas discussed in this application note are patented, patent pending, or open to the public. These ideas are shared with the public for free use with X2Y® chip components purchased from any of our licensed X2Y® manufacturers only. Any unauthorized part, element, device, or circuit used with this disclosed information may infringe and/or violate U.S. and International Law.

Note: Performance results reported in this and other application notes can only be achieved with patented X2Y® components sourced from X2Y® licensed manufacturers or their authorized distribution channels.

References

[1] Shim, Hwan W., Theodore M. Zeeff, and Todd H. Hubing. "Decoupling Strategies for Printed Circuit Borards Without Power Planes". Vol 1, pages 258-261 of IEEE International Symposium on Electromagnetic Compatibility: Symposium Record. Minneapolis, Minnesota, August 19-23, 2002.

[2] Zeeff, Theodore M., Todd H. Hubing, Thomas P. Van Doren, and David Pommerenke. "Analysis of Simple Two-Capacitor Low-Pass Filter" Vol 45, Number 4, pages 595-601 of IEEE Transactions on Electromagnetic Compatibility. November 2003.

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