

## Considerations for Capacitor Selection in FPGA Designs

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## Abstract

Passive power bypass networks perform the critical system function of maintaining power rail stability in the face of IC switching currents. Traditionally, two terminal MLCC capacitors have provided an affordable and adequate bypass solution. However, FPGA capacity growth, coupled with ever decreasing power rail voltages imposes new low-impedance requirements that challenge both the economy and efficacy of traditional MLCC bypass capacitor solutions. We demonstrate economical realization of new generation low impedance power delivery, and the incomparable advantages that low-inductance capacitors offer towards: lower cost, reduced space, higher performance and improved manufacturability.

## Power Delivery Systems

An FPGA power delivery system, PDS serves three needs:

- Core power voltage stabilization
- I/O power stabilization
- I/O return current bypass

These roles can be seen from an overall view of the PDS:

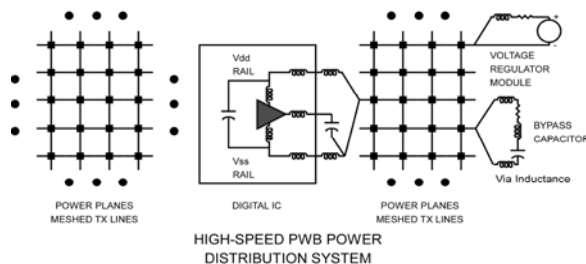


Figure 1, PDS Model w/FPGA I/O

In this model, we see the voltage regulator module as a perfect voltage source in series with a finite resistance and inductance attached to a mesh of transmission lines. These transmission lines represent the behavior of the power / ground planes in the PWB.

At the FPGA mounting, and internal package inductance together with internal capacitance, discrete in-package, and/or on die, form a low pass filter to supply current flow between the device die and the PWB. Significantly above the cut-off frequency of this filter, current flow between the

device core and the PWB is significantly impeded. It should therefore be clear that the PWB does not support high-speed I/O switching currents. These currents can only be supported by energy stored within the device itself.

Core power differs from I/O power in that a substantial amount of I/O switching current drives transmission lines back on the PWB, while core power does not. For totem pole signaling, ie CMOS, SSTL, and HSTL standards, internal device capacitance shunts the rails together and allows return current to enter the package through either the positive or negative rails.

I/O power also differs from core power in that a given FPGA may have as many as 14 I/O power domains, some served by as few as two BGA balls, but typically around seven to eleven balls. Given applications such as wide memory interfaces, power starvation is a very real threat in FPGAs, with the result that I/O power will often require priority over core power for the lowest impedance distribution.

Figure 2 depicts complete signal and return paths for totem pole signals routed on offset strip lines, as common practice in digital boards.

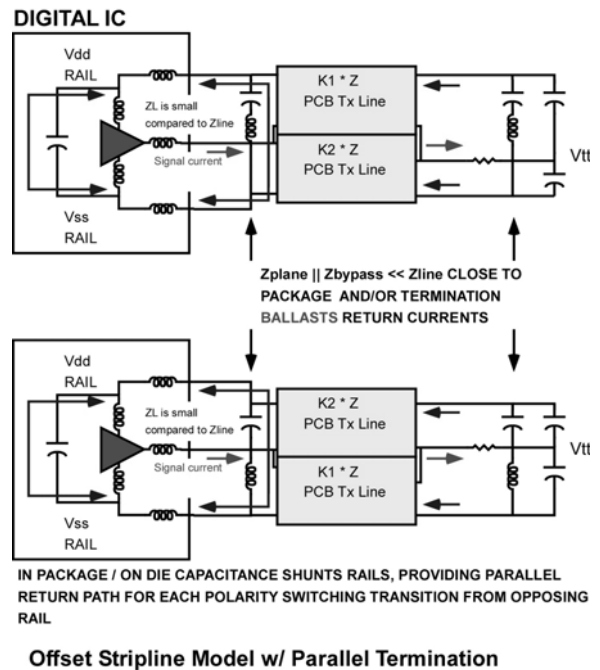


Figure 2, FPGA Signal / Return Paths

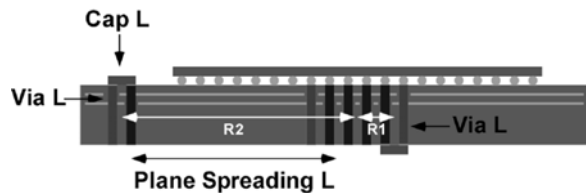
Essentially, signals traverse two parallel transmission lines. One transmission line forms between the signal route and the nearest voltage plane (K1), and the other with the further voltage plane (K2). The parallel combination of these lines sets the overall impedance seen by the signal. Typically, over 80% of the signal energy traverses the transmission line formed between the signal trace and the near plane, (K1).

Bypass capacitors near the driving FPGA ballast the return current independent of the transition, high to low, or low to high, allowing return current to reenter the IC package on both power rails. Bypass capacitors near the load close the AC path from both the dominant, and subordinate transmission lines.

### PCB Inductance: Vias and Planes

As previously noted, mounting, and in-package inductance separates the FPGA die from the PCB planes. PCB planes also exhibit finite spreading inductance from the FPGA power terminals to the radial location of the bypass capacitors.

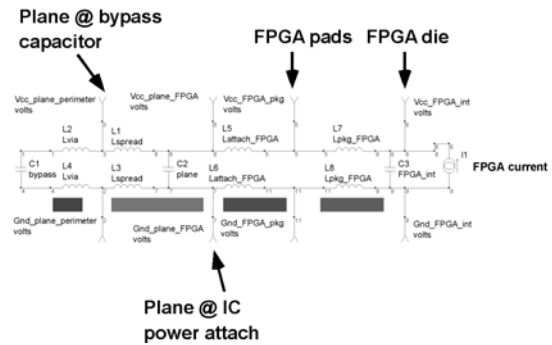
Figure 3, depicts spreading inductance for capacitors located away from power / ground pins, and the additional via inductance for capacitors mounted on the far side of the PWB from the FPGA.



**Figure 3, Via and Plane Spreading Inductance**

Via and plane spreading inductance both increase the impedance between the bypass capacitor and the FPGA. While much attention has been paid in the past to capacitor via attachment inductance, it should be noted that with current generation devices, FPGA via attachment inductance, and plane pair spreading inductance easily become the limiting factors for a design.

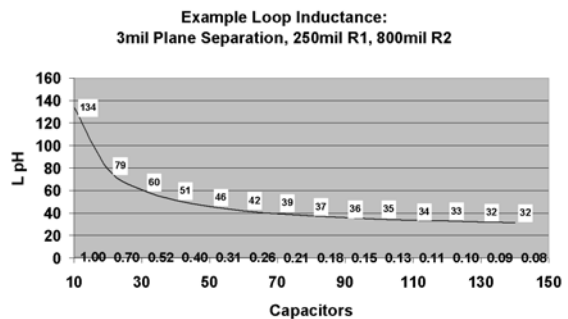
Figure 4, diagrams the elements from IC die to bypass capacitor:



**Figure 4, Parasitics, FPGA Die to Bypass Caps**

Note that at moderate to high frequencies, impedance is determined almost entirely by the combined inductances of the various elements.

Figure 5 demonstrates the impact of just plane spreading impedance on the effectiveness of bypass capacitors:



**Figure 5, Example Spreading Inductance**

The capacitors for this example are ordinary MLCC 0603s with a mounted inductance of 1.4nH, 3mil plane separation and 250mil radius from the FPGA center to power slug ring, and 800 mils from the FPGA center to the bypass capacitor ring. At each point on the chart, we track the incremental admittance of the combined capacitors and plane spreading inductance, compared to an arrangement with 10 capacitors only.

We note:

- Increasing capacitor count from 10 to 140 reduces overall inductance by only a factor of 4:1.
- Beyond 40 capacitors total, the incremental effectiveness of each capacitor is less than 50%, and drops rapidly.

It should therefore be apparent how dramatically the PCB plane design affects bypass capacitor utility. Device attachment vias have a similar impact. The critical consequence of these facts is:

**High performance power rails require thin dielectric planes located close to the FPGA mounting surface.**

**By corollary:**

**High performance power rails require low via inductance.**

In order to meet power distribution impedance targets, it is now common for a single FPGA to require 100 or more conventional MLCC capacitors.

### Capacitor Attachment Via Inductance

Via inductance may be determined accurately with the closed-form formula adapted from Johnson<sup>1</sup>:

#### Equation 1, Via Partial Inductance, Single Via

$$5.08nH * ((H_1^2 * (2 - K_1) / (S * K_1)) + (2 * H_2 * \ln(2 / K_1)))$$

$H_1$  Via length above the uppermost plane  
 $H_2$  Plane to plane separation  
 $D$  Via diameter  
 $S$  Via separation, on centers  
 $K_1 = D / S$

Equation 1 provides some interesting insights:

- Inductance from the portion of the vias above the plane cavity increases as the square of that height.
- Inductance from the portion of the vias within the plane cavity increases linearly with cavity height, and as a natural log function of via separation divided by via drill radius.

If we assume ground fill on the top PCB surface, or negligible via height outside the plane cavity, then we can readily tabulate via inductances for commonly used configurations:

| Configuration                  | D  | S  | pH/mil |
|--------------------------------|----|----|--------|
| 0603 side mount 0.05 via space | 10 | 50 | 23.5   |
| 0603 side mount 0.03 via space | 10 | 30 | 18.2   |
| 0603 side mount 0.03 via space | 15 | 35 | 15.7   |
| 0402 side mount 0.04 via space | 10 | 40 | 21.1   |
| 0612 0.032 via space           | 10 | 32 | 18.9   |
| 0612 0.032 via space           | 12 | 32 | 17.0   |

Table 1, Common Via Inductances

The inductances shown are for each via. For example an 0603 capacitor with vias at 0.05" mounted on a PWB with planes on L2, and L3 at 0.005, and 0.015 respectively would have a total via inductance of  $23.5pH / mil * (5 \text{ mils} + 10 \text{ mils}) = 352 \text{ pH}$ . A via pair to planes in the middle of an 0.062" board approach 1nH, while vias to planes in the middle of an 0.93 board approach 1.5nH.

Given that via inductance is often comparable to if not substantially greater than the ESL of an ordinary capacitor, it may appear that reducing capacitor ESL would provide limited benefit. However, this assumes that via count does not scale up as capacitor ESL scales down.

That assumption is dead wrong. All existing low inductance capacitors support two or more attachment via pairs.

The trick to effective use of low inductance capacitors is managing mutual inductance between vias. When we place multiple vias of the same polarity in near proximity, we effectively construct a solenoid cross section in the Z axis. The magnetic fields reinforce resulting in a net relative L greater than 1/N. It therefore becomes important to configure vias so that like polarities are not adjacent.

### The Dark Side of Vias

To an OEM, via cost is far more than drill and plating. Via holes have two insidious side effects: Plane perforation and blocked signal routes. It is a paradox that in order to reduce system impedance, more attachment vias are needed. However, increasing via density perforates planes, raising plane impedance, and offsetting gains.

Increased via count also results in blocked signal routing channels. For the most common construction method, through-hole vias, a single via blocks as many routing channels as the PCB has signal layers.

If too many channels are blocked, the OEM has no choice but to add signal routing layers. A need to add a single routing layer can in the worst-case force an OEM to add four copper layers to the PCB in order to provide a return current path and maintain board structural integrity.

OEMs can ill afford either the additional component count or layer count impact of excessive vias. Via efficiency, and total via count become increasingly important OEM considerations, particularly in high performance, sic high via count systems.

### Current Generation Low-Inductance Capacitors

Presently, there are four types of low inductance MLCC capacitors suitable for PCB use:

1. Reverse geometry capacitors
2. AVX's IDC™ capacitor
3. Array capacitors
4. X2Y™ style capacitors

#### Reverse Geometry Capacitors

Reverse geometry capacitors were the first low inductance capacitors, built around an obviously good idea: put the terminations on the long axis, and establish current flow across the short axis of the capacitor. This nearly doubles the width of the current path and nearly halves the length of the portion of the induction loop through the capacitor, substantially reducing device ESL. ESL ratings for reverse geometry capacitors vary widely depending on the measurement method employed. It can be shown from the device physics and carefully constructed measurements that in the best possible case, the ESL of a reverse geometry capacitor can be no less than one-fourth its standard geometry counterpart.

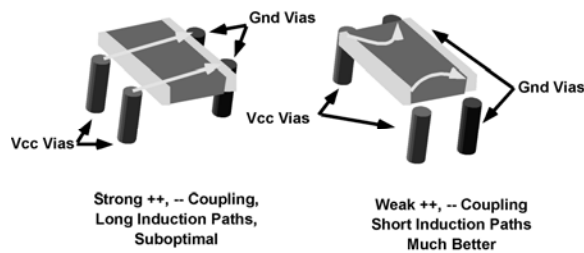


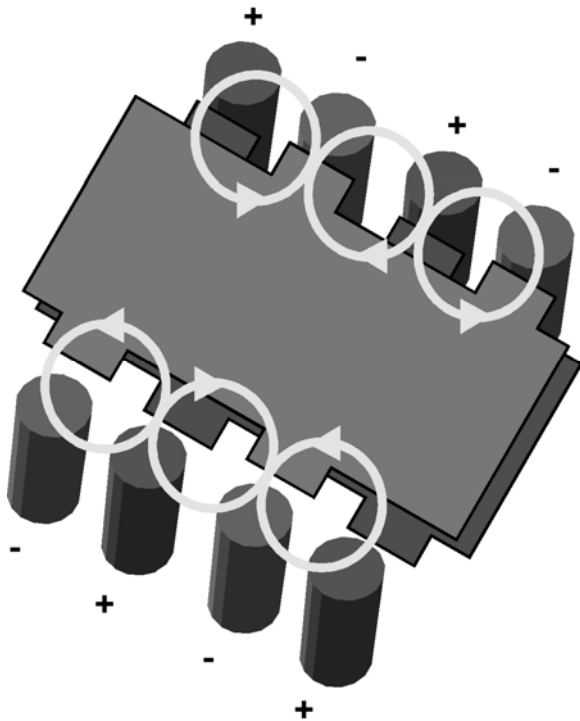
Figure 6, Reverse Geometry Capacitors, and Current Paths

We must take care with our choice of via location. If we locate vias along the long axis, then we end-up with comparatively long induction loops with strong reinforcing mutual coupling. Viewed from the top, the vias look exactly like the solenoid cross-section that they form.

If however, we locate the vias at the ends of the long axis, then we shorten the induction loops, and greatly reduce mutual coupling between like polarity vias. In a carefully designed environment, the mounted inductance of a 0306 capacitor approaches one-half that of its 0603 sibling, and total via count remains the same. Unfortunately, this is not remarkably better than what can be done by mounting a conventional 0603 capacitor with four via attachments.

#### AVX IDC™ Capacitors

AVX presents a substantial improvement over reverse geometry capacitors in the form of its patented IDC™ devices. These devices address both device and via attachment inductance concerns. First eight connection terminals per capacitor afford plentiful vias. Second, the polarity of each adjacent terminal alternates. The result is six very short induction loops: three along the top edge and three along the bottom edge as depicted in Figure 7:



**Figure 7, AVX IDC™ Capacitor, and Current Paths**

Ideally, the combination of eight vias in parallel would yield  $2/8 = 0.25$  times the inductance for two like vias attached to a conventional capacitor. However, current concentrates 2:1 on the inner four terminals and vias. The correct scaling factor may be found by taking the individual current distributions in parallel:

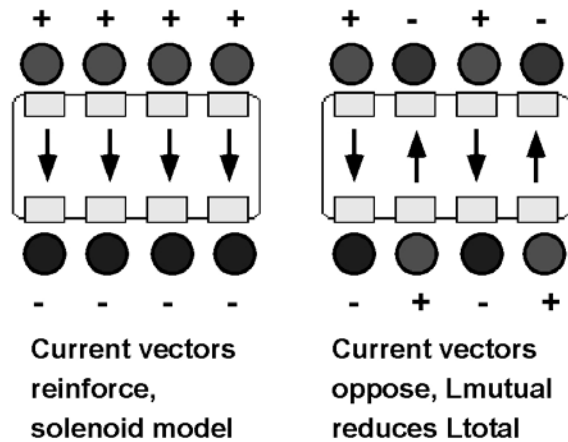
$$K = 2 / (2 \parallel 1 \parallel 2 \parallel 1) / 2 = 0.33$$

Essentially, the via array attached to an IDC™ capacitor exhibits inductance equivalent to six vias instead of eight. Nevertheless, mounted, IDC™ capacitors still represent one of the two lowest inductance options available today.

IDC™ devices are commonly available in both 0612 and 0508 packages with manufacturer ESL ratings of 120pH and 90pH respectively.

### Capacitor Arrays

Ordinary array capacitors are also available in 0612 and 0508 packages. Arrays pack four independent capacitors side by side along the long axis of the part.

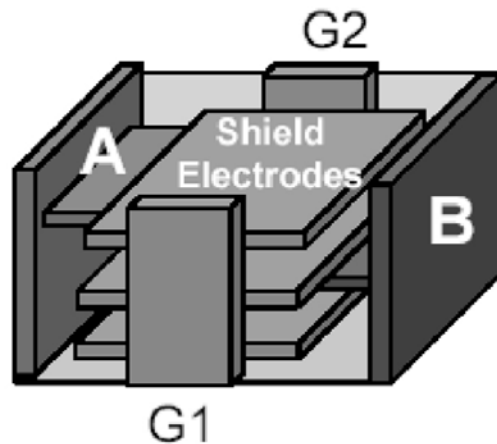


**Figure 8, Array Capacitors**

In microstrip fixtures using interleaved connections as shown in Figure 8, 0612 array capacitors demonstrate ESLs about twice that of similarly sized IDC™ capacitors. However, array capacitors exhibit better current distribution across terminals and vias than their IDC™ counterparts. In moderate performance applications with longer vias, these devices afford very similar performance as like-sized IDC™ capacitors.

### The X2Y™ Capacitor

X2Y capacitors are four terminal, three node devices. G1 and G2 plates connect completely across the short device axis, while A and B plates run the long device axis, similar to a conventional MLCC capacitor.



**Figure 9, The X2Y™ Capacitor**

The X2Y™ capacitor forms two discrete, but extremely well matched capacitors, and each by itself, a low-inductance capacitor. One capacitor forms from the A and G1/G2 plates, and the other forms from the B and G1/G2 plates.

In a single voltage bypass application, both capacitors connect in parallel. X2Y™ capacitors also uniquely provide the ability to bypass two independent voltage rails to ground in the same device.

Best practice attachment with X2Y™ capacitors capitalizes on the perpendicular plate arrangement of the devices. Rather than traversing along one device axis or another the current loop traverses the corners. The best economic practice 0603 size X2Y™ capacitors is a six via pattern.



**Figure 10, X2Y & Surface Induction Loops**

The unique perpendicular plate arrangement of the X2Y™ when combined with a six via attachment, results in four induction loops of comparable size to each of the loops in an IDC™. As with the four center terminals of the IDC™, the center terminals of the X2Y™ see twice the current density as the outer terminals. However, unlike the IDC™, this effect is confined to just the two terminals G1/G2 terminals. The resulting inductance for the via array is:

$$K = ( \frac{1}{2} + \frac{1}{4} ) / 2 = 0.375$$

This is only 13% higher than the optimal value of 0.333. Attached performance of a properly mounted X2Y with six vias is almost identical to that of an IDC™ that requires 33% more vias. In microstrip fixture measurements, the X2Y™ 0603 capacitor repeatably demonstrates less than 60pH. Due to the fact that X2Y™ inductance is defined by geometry across the corners and not the capacitor body size,

other package X2Y™ devices have demonstrated inductances under 30pH.

### Mounted Capacitor Measurements

Given accurate device ESL, and from: closed-form equations, field-solver, or actual test fixture measurements for via attachments, we can determine mounted inductance of any prospective capacitor. Measured results show excellent correlation to the closed form equations.

|                    | 4 Layer Test Fixture |       |
|--------------------|----------------------|-------|
| <b>H1</b>          | 0.012                | 0.012 |
| <b>H2</b>          | 0.038                | 0.038 |
| <b>S</b>           | 0.032                | 0.044 |
| <b>D</b>           | 0.02                 | 0.02  |
| <b>K1 D/S</b>      | 0.63                 | 0.45  |
| <b>L / via pH</b>  | 590                  | 629   |
| <b>L 0603 pH</b>   | 1680                 |       |
| <b>L X2Y pH</b>    |                      | 531   |
| <b>Measured pH</b> | 1700                 | 530   |

**Table 2, Example Closed Form, vs Measured Inductance**

### Low Inductance Capacitor Comparative Mounted Performance

For any attached low inductance capacitor and power plane configuration, we can develop a pair of useful metrics:

1. The number of conventional MLCC capacitors that may be replaced.
2. The relative number of vias used versus conventional MLCC capacitors.

The number of capacitors that may be replaced is a small matter of algebra based on the relative device ESL and via attachment inductances. A common attribute of all current low-inductance capacitors is an ESL much less than that of a conventional 0603 MLCC capacitor. Where via inductance is very low, ie thin power plane pair located very close to the IC surface, the replacement ratio approximates the ratio of 0603 capacitor ESL to the ESL of the low inductance capacitor. This configuration always corresponds to the lowest impedance rail to the FPGA, with thin plane dielectric located closest to the FPGA mounting surface.

At the opposite end of the spectrum, where via inductance is very large compared to conventional capacitor ESL, the replacement ratio follows the effective number of vias.

By setting a constant  $K_1$  as the inductance ratio of a single via pair on a conventional capacitor to the via array inductance for low-inductance capacitor attachment we get:

**Equation 2**

$$L_{LOW\_L} = ESL_{LOW\_L} + L_{VIA\_PAIR} / K_1$$

**Equation 3**

$$L_{NORMAL} = ESL_{NORMAL} + L_{VIA\_PAIR}$$

The number of low inductance capacitors  $N$  needed in place of a single conventional capacitor is:

**Equation 4**

$$N = L_{LOW\_L} / L_{NORMAL} = (K_1 * ESL_{LOW\_L} + L_{VIAS}) / (K_1 * (ESL_{NORMAL} + L_{VIAS}))$$

**Equation 5**

For  $L_{VIAS} \gg ESL_{NORMAL} = 1/K_1$

**Equation 6**

For  $L_{VIAS} \ll ESL_{NORMAL} = ESL_{LOW\_L} / ESL_{NORMAL}$

| Capacitor Type        | Net Caps |      | Net Vias |      |
|-----------------------|----------|------|----------|------|
|                       | Low      | High | Low      | High |
| 0603 conventional     | 1        | 1    | 1        | 1    |
| 0306 reverse geometry | 0.25     | 0.5  | 0.5      | 1    |
| 0612 IDC™             | 0.13     | 0.33 | 0.5      | 1.33 |
| 0612 Array            | 0.25     | 0.3  | 1        | 1.13 |
| 0603 X2Y              | 0.13     | 0.35 | 0.38     | 1.10 |

**Table 3, Relative Capacitor / Via Count Ranges**

Note that array capacitors have the tightest capacitor replacement range, that actually matches IDC™ performance, but only in situations where via inductance is very high. By definition those are only performance situations.

The extremes of via inductance do not occur in practice. As a result, the practical values converge

away from the extremes. Replacement ratios with IDC™ and X2Y™ capacitors most commonly range from about 1:3.8 conventional capacitors to 1:5.5 conventional capacitors. These cases reflect plane pairs in the same half of the board stack-up as the FPGA mounting surface and capacitors located on the same surface as the FPGA.

Capacitor Array Effects

When capacitors are arranged in arrays, mutual inductance between the vias and the capacitors themselves tends to raise effective inductance from  $1/N$ , where  $N$  is the number of capacitors in the array. We have conducted test board studies that indicate conventional capacitors work best when arranged end to end along the long axis, as turns-out to be the most common OEM practice.

When multiple columns of conventional capacitors are employed, degradation in admittance of 10% - 24% is readily observable, depending on via pattern in the array. Given that current FPGA applications require 100 or more conventional capacitors, multi-column arrays are inevitable with conventional capacitors. However with low-ESL capacitors, it is possible to still maintain a single ring of capacitors around the FPGA. As a result, these devices all enjoy a minimum additional performance benefit / device of 10% versus the figures shown in Table 3.

Unfortunately, reverse geometry capacitors tend not to enjoy this benefit. This is because the optimum via pattern for reverse geometry capacitors is at the ends, placing vias of adjacent capacitors in closer proximity than any of the other low-inductance capacitor alternatives, in an end-to-end configuration. The alternative configuration rotates reverse geometry capacitors by 90 degrees and closely resembles a conventional capacitor array configuration.



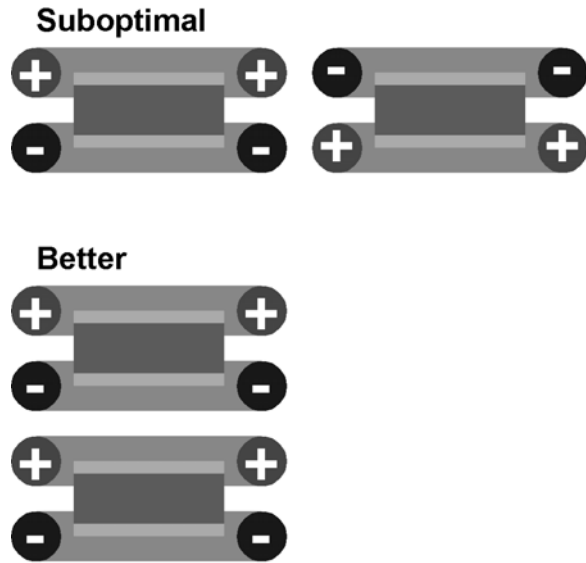


Figure 11, Reverse Geometry Array Configurations

### PCB Area Comparison

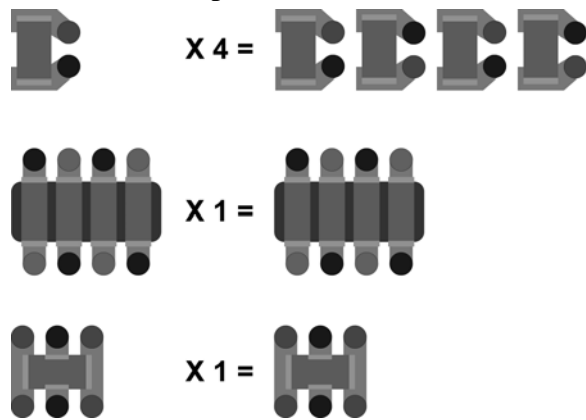


Figure 12, Area Comparisons, Like Mounted Inductance, Conventional 0603, IDC™ 0612, X2Y™ 0603

### OEM System Cost

Total OEM cost includes the raw component cost, component placement cost and via drill costs. It is not uncommon for either placement or via drill costs alone to exceed unit component cost in the fiercely competitive conventional MLCC market. Because low inductance capacitors afford dramatic placement cost reduction, and often via drill hole reduction as well, they offer greater latitude for raw unit pricing.

At the present time, only the X2Y™ and reverse geometry capacitors guarantee a net even, or net reduction in total via count for all practical cases. While both IDC™ and X2Y™ capacitors offer the lowest possible capacitor counts for situations where via inductance is small. IE, the IDC™ and X2Y™ capacitors gain component count advantage over all alternatives as power distribution performance requirements relentlessly rise.

### Conclusions

FPGA bypass networks serve all three needs:

- Core power,
- I/O power,
- Totem pole signal return current ballast.

Performance of each of these functions is limited by the mounted inductance of the bypass capacitor array.

FPGA attachment, and power plane pair spreading inductance both shrink the available mounted inductance budget for the bypass capacitor network.

Performance of conventional capacitors is rapidly falling short of FPGA application needs. Despite extremely low unit costs, the sheer quantity of devices needed has opened the door for manufacturers of low-inductance capacitors to capture this important market.

Contrary to popular misconceptions, low inductance capacitors afford substantial performance benefits over conventional capacitors in bypass applications, and can offer compelling system cost savings as well.

Of available low inductance capacitors, AVX IDC™, and X2Y™ capacitors deliver the highest possible performance. Array capacitor performance lags considerably, and reverse geometry capacitors provide the least performance gain over conventional devices.

X2Y™ 0603 capacitors perform identically to IDC™ 0612 capacitors while the IDC™ capacitors require 33% more vias to equal mounted X2Y™ performance in demanding applications, that are ever more commonplace.

<sup>i</sup> Johnson, Howard, “High Speed Signal Propagation”, 2003 Prentice Hall, pp 259