Considerations for Capacitor Selection in FPGA Designs

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Agenda

• What does an FPGA power delivery system look like?
• What \textit{really matters} in a FPGA PDS?
• Do low inductance capacitors help?
• Comparisons of low inductance capacitors for power bypass applications.
• Conclusions
FPGA Power Delivery Systems

• Power / ground planes model as meshed transmission lines

![Diagram of FPGA Power Delivery System]

POWER PLANE MESHED TX LINES

Vdd RAIL

Vss RAIL

HIGH-SPEED PWB POWER DISTRIBUTION SYSTEM

VOLTAGE REGULATOR MODULE

BYPASS CAPACITOR

Via Inductance

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FPGA Power Delivery Systems

- Voltage regulator module attaches into the mesh, whether bulk or point-of-load

![Diagram of FPGA Power Delivery System]
FPGA Power Delivery Systems

- Bypass capacitors locate at various points in the grid.
FPGA Power Delivery Systems

• FPGA mount and package, form a low-pass filter that limits HF current flow.
  – Usually less than 50MHz

• This frequency range is (FORTUNATELY!) within the range of discrete ceramic capacitors.
Bypass Significance to High-Speed Signal Returns

• Properly routed high speed signals reference a single voltage rail
• Properly routed high-speed signals DO NOT TRAVERSE the bypass network to switch routing layers!
• Properly routed high-speed signals DO NOT TRAVERSE plane cavity capacitance to switch routing layers!
FPGA Signal Propagation
Older Packages

Low frequency switching model

LF signalling current traverses bypass caps & plane cavity capacitance
FPGA Signal Propagation
New Packages

IC

Ydd
RAIL

Vss
RAIL

In-package Tx Line

No appreciable return current traverses bypass network or plane cavity capacitance

PCB Tx Line

High frequency switching model
Parasitics, FPGA to Bypass Caps

Plane noise measured away from power ring

Component specs voltage noise here

SSN on idle I/Os visible here

FPGA attachment, plane spreading, and capacitor attachment via inductance all work to decouple the bypass capacitors from the FPGA.
PCB Inductance

- For simple power / ground patterns, spreading inductance may be readily determined by application of the Biot-Savart law.
- Radial spreading inductance:

\[ \mu_0/2\pi \times H \times \ln\left( \frac{R_2}{R_1} \right) \]
Spreading Inductance Limits on Capacitor Effectiveness

Example Loop Inductance:
3mil Plane Separation, 250mil R1, 800mil R2

- Capacitor incremental effectiveness drops rapidly
Capacitor Attachment Via Inductance

- For vias contained within plane cavities, inductance varies linearly with height.

<table>
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<th>Configuration</th>
<th>D</th>
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<th>pH/mil</th>
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<td>32</td>
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The Dark Side of Vias: “Perforate the planes, Luke”

• Vias are a necessary but expensive part of power interconnect. Extra vias cause extra:
  – Plane perforation-
    • Increased plane spreading impedance
    • Degradation of signal return path
  – Blocked signal routes-
    • Alternatives: blind vias or more layers are expensive
  – Direct drilling costs-
    • Vias at $0.005/hole / $0.01 / capacitor typical, often COST MORE than the capacitors they connect!

• VIA utilization is an important system cost factor.
Current Gen. Low L Caps

• Reverse geometry capacitors:
  – 0612, 0508, 0306, etc.

• AVX Corp. IDC™ capacitors
  – 0612, 0508

• Array capacitors
  – 0612, 0508

• X2Y™ capacitors
  – 1206 (and larger), 0805, 0603
Reverse Geometry Capacitors

- Interconnect on long axis
- Induction loop across short axis
- Best, low-inductance attachment is at device ends.
  - Yields two capacitors each w/ X-Y plane induction loop about $\frac{1}{2}$ of traditional cap.
  - Can replace two to four regular caps depending on via and plane geometries
Reverse Geometry Capacitors

- Optimum via arrangement emulates two smaller geometry capacitors.
  - IE 2 X 0303 for 0306 parts

![Diagram showing reverse geometry capacitors with labels for Vcc Vias, Gnd Vias, Strong ++, -- Coupling, Long Induction Paths, Suboptimal, Weak ++, -- Coupling, Short Induction Paths, Much Better]
AVX Corp. IDC™ Capacitors

• Major improvement of reverse geometry concept:
  – Typically eight attachment terminals
  – Terminals interleave polarity to reduce BOTH via and device inductance
  – Eight terminal devices form **SIX SMALL X-Y plane induction loops**
AVX Corp. IDC™ Capacitors
AVX Corp. IDC™ Capacitors

• Via utilization affected by current crowding in the center vias and terminals.

• For eight terminal device, ideal via K factor would be 0.250, is 0.333, +33%.

• Can replace from three to six+ regular caps depending on via and plane geometries – 4:1 – 5.5:1 typical, with proper placement
Array Capacitors

• Four independent capacitors in parallel.
• Can be wired interdigitated like an IDC™
  – Induction loops are hybrid of six X-Y loops of IDC™ for the vias, and four loops across device short axis
  – Do not perform as well as IDC™s, BUT
  – Exhibit more even current distribution than IDC™s
• Can replace from three+ to four regular caps
  – Not an IDC™, but not bad for moderate performance applications.
Array Capacitors

• When wired in parallel, perform poorly.
  – Vias form solenoid like magnetic structure

• When wired like an IDC™, via induction is similar to IDC, but cap induction is much worse.
The X2Y™ Capacitor

- Instead of reverse geometry, the X2Y™ is a perpendicular geometry capacitor.
- X-Y plane current loops form around each corner.
  - Current distribution is extraordinarily even in large devices where eight vias may be used well.
  - Current distribution has similar asymmetry as IDC™ devices for smaller ( < 1206 ) devices.
    - Six terminal attach $K = 0.375$ vs. 0.333 ideal, +13%
The X2Y™ Capacitor
The X2Y™ Capacitor

- 0603 X2Y™ is smallest size low L cap
- Can replace from three to six+ regular caps depending on via and plane geometries
  - 4:1 – 5.5:1 typical, with proper placement
  - Performance of six via 0603 X2Y™ essentially identical to eight via IDC™ 0612 or 0508
- X-Y induction across corners for X2Y™ result in negligible increase in inductance in larger X2Y™ caps
  - X2Y 2220 inductance actually LOWER than X2Y 0603
  - X2Y 2220 w/eight vias, lowest mounted L of any ceramic cap
Capacitor Array Effects The Dark Side of Vias, Reduxe

• Low impedance systems require the equivalent of many conventional, two terminal MLCC caps.

• When placed in close proximity, mutual inductance between adjacent capacitors dilutes the benefit of each.
  
  – IE, two capacitors exhibit mounted L much greater than ½ the mounted L of just one capacitor.

• Example measurements on a four layer board:
  
  – 1 0603 mounted in isolation: 1700pH
  – 4 0603 mounted in array w/interdigitated power / gnd vias: 620pH, 45% higher than 425pH ideal.
Cap and Via Count Comparisons

- **IDC™** and **X2Y™** yield lowest capacitor counts
- **IDC™** increases via count over conventional caps significantly for low performance supplies, i.e., long vias.
- **X2Y™** yields lowest via count

<table>
<thead>
<tr>
<th>Capacitor Type</th>
<th>Net Caps</th>
<th></th>
<th>Net Vias</th>
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<tr>
<td></td>
<td>Low</td>
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<td>High</td>
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<td>1</td>
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<tr>
<td>0612 IDC™</td>
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<td>0.5</td>
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<tr>
<td>0612 Array</td>
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<td>0.3</td>
<td>1</td>
<td>1.13</td>
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<tr>
<td>0603 X2Y</td>
<td>0.13</td>
<td>0.35</td>
<td>0.38</td>
<td>1.10</td>
</tr>
</tbody>
</table>

Table 1, Relative Capacitor / Via Count Ranges
PCB Area Comparison

- X 4 = 8 Vias
- X 2 = 8 Vias
- X 1 = 8 Vias
- X 1 = 6 Vias

Reverse Geometry
IDC™ OR Array
X2Y™
Practical Example
Virtex2 FFBGA 896

PCB #6 & #7
100kHz - 300MHz Xilinx test Boards S21

- 20 ea X2Y xfer |Z| <= 104 ea 0402 @ pwr / gnd ring

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Practical Example
Virtex2 FFBGA 896

PCB #6 & #7
100kHz - 300MHz Xilinx test Boards S21

- 20 ea X2Y Xfer |Z| << 104 ea 0402
- Additional advantage for Virtex4 and similar
Conclusions

• Low inductance capacitors are becoming increasingly important to FPGA PDS designs

• Drill and placement costs dominate capacitor system cost
  – REDUCE COMPONENT COUNT!
  – REDUCE VIA COUNTS!

• As capacitor counts rise, incremental effectiveness diminishes

• X2Y™ capacitors offer the lowest in-system:
  – Mounted inductance
  – Component count
  – Via count
  – Real estate consumption