Integrating the Right Decoupling Capacitor: Busting the 9 Greatest Capacitor Myths

James P. Muccioli & Dale L. Sanders
Outline – 9 Greatest Capacitor Myths

1. Understanding the Role of Decoupling
2. Testing Decoupling Capacitors
   ✓ Myth #1
3. Evaluating Decoupling (Capacitors-Only)
   ✓ Myth #2
   ✓ Myth #3
   ✓ Myth #4
4. PDS Placement & Mounting Parasitics
   ✓ Myth #5
   ✓ Myth #6
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
   ✓ Myth #7
   ✓ Myth #8
7. Conclusion/Questions
   ✓ Myth #9
Understanding the Role of Decoupling

Power Distribution System (PDS)

- Is not a perfect DC supply due to parasitics.
- PDS needs defined voltage levels that include max & min values to ensure IC functionality.
- Voltage levels require the PDS to have a target impedance.
- Capacitors are used to meet target impedances to prevent:
  - Current Ripples – supply instantaneous current (energy).
  - Bypass transients – filter high frequency switching noise.
Decoupling capacitors consist of:

- Large value caps – bulk caps (mid-freq).
- Small value caps – bypass/H.F. caps (high-freq).

What are the PDS design issues?

- **Inductance**
  - Caps
  - Vias
  - Component mounting
  - PCB plane
  - Package

- **PCB real-estate**
  - Number of caps & vias
  - Location/effectiveness
  - Placement cost
  - Multiple power planes

- **Signal Integrity (SI)**
  - Number of vias (routing)
  - Manufacturing cost (multiple plane PCBs)
  - Functionality
Understanding the Role of Decoupling

PDS Example

Outline – 9 Greatest Capacitor Myths

1. Understanding the Role of Decoupling
2. Testing Decoupling Capacitors
   ✓ Myth #1
3. Evaluating Decoupling (Capacitors-Only)
   ✓ Myth #2
   ✓ Myth #3
   ✓ Myth #4
4. PDS Placement & Mounting Parasitics
   ✓ Myth #5
   ✓ Myth #6
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
   ✓ Myth #7
   ✓ Myth #8
7. Conclusion/Questions
   ✓ Myth #9
Myth #1 – Industry has uniform standards to test & evaluate the performance of decoupling capacitors.
There are 3 main tests to evaluate decoupling capacitors:

- **Network Analyzer**
  - Insertion Loss
- **Time-Domain Analysis**
  - Ripple
  - Transients
- **Impedance Analyzer**
  - Impedance
Test Fixtures – What is the test set-up to evaluate a capacitor?

Without an industry standard, there are 2 main schools of thought:

- Capacitor-in-system
- Capacitor-only
Capacitor-in-system

_advantages

- More “real world” measurements
- Allows vias to be included; current path in vias can be difficult to model at H.F. (specifically for multi-terminal capacitors).

-disadvantages

- Application specific measurement
  - Limited to specific parameters – PCB (material & thickness), via size, plane stack-up, etc.
Testing Decoupling Capacitors

Capacitor-in-system

- Passive PCB
  - Insertion Loss
  - Time-Domain
  - Impedance
- Sample PCB
  - Insertion Loss
  - Time-Domain
  - Impedance
- Active PCB
  - Time-Domain
Testing Decoupling Capacitors

Capacitor-in-system – type of measurement

- Across cap
  - Measure cap-only.
  - Not a true system measurement.

- PCB Edge
  - Not a true system measurement for IC

- IC package dimension
  - Measure PDS network.
  - Allows mounting, via, and plane impedance to be included.

Capacitor-only

- Advantages
  - Accurately measures capacitor
  - Allows for accurate models of capacitor

- Disadvantages
  - PCB structure parameters can be difficult to model.
  - Component mounting, current loops, via influence, plane stack-up, etc.
Testing Decoupling Capacitors

Capacitor-only Fixture

- Microwave solderless fixture
- 50 ohm coplanar/microstrip PCBs
Summary **Myth #1** – Industry has uniform standards to test & evaluate the performance of decoupling capacitors.

- There are no uniform industry standards to test and evaluate decoupling caps.

- Types of testing
  - Time-Domain Analysis
  - Network Analyzer
  - Impedance Analyzer

- Types of fixtures
  - Capacitor-in-system
  - Capacitor-only
Outline – 9 Greatest Capacitor Myths

1. Understanding the Role of Decoupling
2. Testing Decoupling Capacitors
   ✓ Myth #1
3. Evaluating Decoupling (Capacitors-Only)
   ✓ Myth #2
   ✓ Myth #3
   ✓ Myth #4
4. PDS Placement & Mounting Parasitics
   ✓ Myth #5
   ✓ Myth #6
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
   ✓ Myth #7
   ✓ Myth #8
7. Conclusion/Questions
   ✓ Myth #9
Myth #2 – Adding more capacitance will fix the problem.

Myth #3 – For bulk caps, ESR is main concern; and only electrolytic & tantalum can be used.
Evaluating Decoupling (Capacitors-Only)

Time-Domain Input signal = 10 MHz, 1 nsec rise/fall time, 5V amplitude, 80/20 duty cycle.

- Ripple – Tantalum and Electrolytic both need 47uF {Add more capacitance} vs. 1.0uF for the MLCC.
- Transients – 1.0uF MLCC substantially improved switching transients.

Evaluating Decoupling (Capacitors-Only)

Insertion Loss – ENA 100 kHz to 8.5GHz.

- 1.0uF MLCC shows comparable or better attenuation than both the electrolytic or tantalum capacitors with 2% the capacitance value.
- Inductance inhibits the transfer of energy (current) out of the cap.

Summary  Myth #2 – Adding more capacitance will fix the problem.

- Adding more capacitance will improve the ripple thus lowering the insertion loss/impedance at lower frequencies.
- However, capacitor parasitic inductance affects:
  - The efficiency of energy transfer out of the capacitor.
  - Reduces high frequency transient response.

PLAUSIBLE... BUT
Summary **Myth #3** – For bulk caps, ESR is the main concern; and only electrolytic & tantalum can be used.

- ESR is a concern, however, inductance should also be considered.
- MLCC Technology
  - Can significantly reduce the amount of capacitance required in a circuit.
  - Can be manufactured with comparable capacitance values as electrolytic and tantalum for decoupling applications.
Myth #4 – Smaller package size is always better for reducing inductance, the capacitance value has no affect on inductive behavior.
Evaluating Decoupling (Capacitors-Only)

MLCC – Smaller is better – 0603 has less inductance than 0805, 1206, & 1812.

- To meet total capacitance requirements typically small caps increase the number of caps needed. (Package size limits number of layers.)
- Larger number of caps require more vias & greater distance from IC. (More PCB space)

Evaluating Decoupling (Capacitors-Only)

X2Y® Technology – package size comparison.

- The X2Y® Technology maintains or improves low-inductive performance as package size increases.

Evaluating Decoupling (Capacitors-Only)

The capacitance value has no affect on the inductive behavior of a cap.

Physical geometry of the current loop through the capacitor affects the parasitic inductance.

Evaluating Decoupling (Capacitors-Only)

X2Y® Technology – capacitive value comparison.

The X2Y Technology maintains or improves low-inductive performance as capacitive value increases.

Summary **Myth #4** – Smaller package size is always better for reducing inductance, the capacitance value has no effect on inductive behavior.

- Std MLCC Technology - smaller is better.
- **X2Y® Technology**
  - Structure promotes mutual inductance cancellation that lowers over-all net inductance.
  - Inductance improves with:
    - Larger capacitance value (more layers).
    - Larger package (more layers).
Evaluating Decoupling (Capacitors-Only)

What is the performance benefit of low-inductive caps?

- Each MLCC measured individually
- Total (5) MLCC = 0.398uF
- X2Y® total capacitance value = 0.44uF
- Note: package size differences

- MLCC cumulative measured
- Total (5) MLCC = 0.5uF
- X2Y® total capacitance value = 0.44uF
- Note: package size differences

Measurements made on 50ohm Coplanar PCB with Ground Plane.


7/19/2005

Copyright © X2Y Attenuators, LLC all rights reserved.
Outline – 9 Greatest Capacitor Myths

1. Understanding the Role of Decoupling
2. Testing Decoupling Capacitors
   ✓ Myth #1
3. Evaluating Decoupling (Capacitors-Only)
   ✓ Myth #2
   ✓ Myth #3
   ✓ Myth #4
4. PDS Placement & Mounting Parasitics
   ✓ Myth #5
   ✓ Myth #6
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
   ✓ Myth #7
   ✓ Myth #8
7. Conclusion/Questions
   ✓ Myth #9
PDS Example

Myth #5 – Bypass capacitor placement with respect to ICs or other caps is not very critical.
Distance between IC and Cap:
- Larger current loop
- More inductance
- Less effective
Effects of spreading Inductance in PDS

- Using position 9 & 11 as I/O & core power position the effects of spreading inductance in the planes can be seen.
- Demonstrates why measuring across a cap for capacitor-in-system measurement isn’t accurate.

This paper uses the concept of proper capacitor placement on a PC board to improve circuit performance.

Decoupling Strategies for Printed Circuit Boards Without Power Planes

Hwan W. Shim, Theodore M. Zeef, Todd Hubing
EMC Labrotory
University Missouri-Rolla
Rolla, MO

* Presented at the August 2002 IEEE EMC Symposium, Minneapolis, MN - TU-PM-G-5, Volume 1, page258

Note: X2Y has expanded the testing with this PC board; further information can be found at this link:
#3001 - X2Y® Solution for Decoupling Printed Circuit Boards
PDS Placement & Mounting Parasitics

Measurements made on 50ohm Coplanar PCB with Ground Plane.

X2Y Application Note #3001 - X2Y® Solution for Decoupling Printed Circuit Boards.
PDS Placement & Mounting Parasitics

Measurements made on 50ohm Coplanar PCB with Ground Plane.
The X2Y® design maximizes mutual inductance to reduce parasitic inductance. Inside X2Y®, every other electrode layer within the single component body is in opposition to cancel the magnetic flux.

Flux lines cancel outside of component body boundaries

Flux lines cancel inside of component body boundaries

*Dell Patent #6,337,798*
Summary **Myth #5** – Bypass capacitor placement with respect to ICs or other caps is not very critical.

- Distance between caps and ICs should be minimized to reduce spreading inductance.
- Spacing between caps can reduce or improve performance if external coupling occurs.
  - Depends on the direction of current.
  - Inter-digitate current flow through std. MLCC Technology to improve performance.
  - Use technology that minimizes external coupling and inter-digitated current flow (X2Y® Technology).
Myth #6 – Low-inductive caps are not useful on typical PCBs because via and mounting parasitics limit their effectiveness.
Reverse-Aspect-Ratio (LL) Caps – Capacitor-only

LL caps show lower inductive performance on microstrip PCB.
Reverse-Aspect-Ratio (LL) Caps – Capacitor-in-system

- Mounted with vias, LL caps (6 vias) have the same performance as MLCC caps (4 vias).
- LL caps are limited by mounting parasitics.
Multi-Parallel Vias

- MLCC – going from 2 to 4 vias improves impedance by 150 mΩ @ 100 MHz.

MLCC 0603, 2 vias
799mΩ @ 100MHz

MLCC 0603, 4 vias,
556mΩ @ 100MHz

X2Y®, 6 vias
260mΩ @100MHz
### Via & Pad Geometries

- Optimized placement and routing of the vias & pads to minimize inductance.
- Considerations should include:
  - **Via**
    - Diameter
    - Length
    - Location
  - **Trace/Pad**
    - Width
    - Length

---

<table>
<thead>
<tr>
<th>Hole Diameter 0.020 inches</th>
<th>Via length:</th>
<th>0603 skinny</th>
<th>0603 fat</th>
<th>0603 end</th>
<th>0603 side</th>
<th>0402 end</th>
<th>0402 side</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(inches)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>.004</td>
<td>1.51</td>
<td>0.89</td>
<td>0.42</td>
<td>0.33</td>
<td>0.38</td>
<td>0.21</td>
<td></td>
</tr>
<tr>
<td>.006</td>
<td>1.66</td>
<td>1.12</td>
<td>0.53</td>
<td>0.38</td>
<td>0.44</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>.010</td>
<td>2.13</td>
<td>1.47</td>
<td>0.68</td>
<td>0.51</td>
<td>0.58</td>
<td>0.32</td>
<td></td>
</tr>
<tr>
<td>.020</td>
<td>2.68</td>
<td>2.07</td>
<td>1.07</td>
<td>0.67</td>
<td>0.82</td>
<td>0.43</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hole Diameter 0.010 inches</th>
<th>Via length:</th>
<th>0603 skinny</th>
<th>0603 fat</th>
<th>0603 end</th>
<th>0603 side</th>
<th>0402 end</th>
<th>0402 side</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(inches)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>.004</td>
<td>1.51</td>
<td>0.95</td>
<td>0.50</td>
<td>0.36</td>
<td>0.42</td>
<td>0.26</td>
<td></td>
</tr>
<tr>
<td>.006</td>
<td>1.77</td>
<td>1.17</td>
<td>0.59</td>
<td>0.46</td>
<td>0.50</td>
<td>0.32</td>
<td></td>
</tr>
<tr>
<td>.010</td>
<td>2.18</td>
<td>1.52</td>
<td>0.77</td>
<td>0.61</td>
<td>0.67</td>
<td>0.40</td>
<td></td>
</tr>
<tr>
<td>.020</td>
<td>2.87</td>
<td>2.23</td>
<td>1.16</td>
<td>0.85</td>
<td>1.01</td>
<td>0.60</td>
<td></td>
</tr>
</tbody>
</table>

---

Howard Johnson, PhD, “Parasitic Inductance of a Bypass Capacitor II,” HIGH-SPEED DIGITAL DESIGN – online newsletter Vol. 6 Issue 9, Signal Consulting, Inc.
Inter-digitated vias

- Mutual inductance between vias cancel.
- Lowers over-all net inductance of vias, thus mounting inductance of caps.
- Inter-digitated caps are ideal to use minimize pad/trace distance to vias.
PDS Placement & Mounting Parasitics

Minimize distance between PCB planes and capacitor (Via Length).

- Extra via length between capacitor pad and PCB planes adds inductance.

Height should be minimized.

Summary **Myth #6** – Low-inductive caps are not useful on typical PCBs because via and mounting parasitics limit their effectiveness.

- Lower Via/mounting Inductance
  - Multiple parallel vias
  - Inter-digitate vias – lower over-all net via inductance.
  - Use Inter-digitated caps – to minimize pad/trace distance from cap to via.
  - Minimize distance between planes and caps.
Outline – 9 Greatest Capacitor Myths

1. Understanding the Role of Decoupling
2. Testing Decoupling Capacitors
   ✓ Myth #1
3. Evaluating Decoupling (Capacitors-Only)
   ✓ Myth #2
   ✓ Myth #3
   ✓ Myth #4
4. PDS Placement & Mounting Parasitics
   ✓ Myth #5
   ✓ Myth #6
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
   ✓ Myth #7
   ✓ Myth #8
7. Conclusion/Questions
   ✓ Myth #9
MLCC vs. X2Y® on a Passive Xilinx FPGA PCB.

- (104) 0402 MLCC vs. (20) 0603 X2Y®
- (208) vias – MLCC vs. (120) vias – X2Y®
- Saves PCB real-estate!

### Table 1, Mounted Inductance, Comparative Conventional and X2Y³

<table>
<thead>
<tr>
<th></th>
<th>Capacitors on Component Side</th>
<th>Capacitors on Back side⁴</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>H1</td>
<td>H2</td>
</tr>
<tr>
<td></td>
<td>0.005 0.020 0.005 0.020 0.005 0.012 0.012</td>
<td>0.005 0.005 0.005</td>
</tr>
<tr>
<td></td>
<td>H2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.014 0.003 0.003 0.001 0.001 0.038 0.038</td>
<td>0.014 0.003 0.001</td>
</tr>
<tr>
<td></td>
<td>S</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.03 0.03 0.03 0.03 0.03 0.032 0.044</td>
<td>0.03 0.03 0.03</td>
</tr>
<tr>
<td></td>
<td>D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.01 0.01 0.01 0.01 0.01 0.02 0.02</td>
<td>0.01 0.01 0.01</td>
</tr>
<tr>
<td></td>
<td>K1 D/S</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.33 0.33 0.33 0.33 0.33 0.63 0.45</td>
<td>0.33 0.33 0.33</td>
</tr>
<tr>
<td></td>
<td>L / via pH</td>
<td></td>
</tr>
<tr>
<td></td>
<td>318 393 76 217 40 590 629</td>
<td>1580 1530 1540</td>
</tr>
<tr>
<td></td>
<td>L 0603</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1052 1290 662 935 579 1500b 1760</td>
<td>3670 3560 3590</td>
</tr>
<tr>
<td></td>
<td>L 0402</td>
<td></td>
</tr>
<tr>
<td></td>
<td>952 1190 552 835 479 1400 1660</td>
<td>3570 3460 3490</td>
</tr>
<tr>
<td></td>
<td>L X2Y</td>
<td></td>
</tr>
<tr>
<td></td>
<td>267 355 117 223 90 435 531b</td>
<td>1250 1210 1220</td>
</tr>
<tr>
<td></td>
<td>Caps req'd 0603</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.9 3.6 5.6 4.2 6.5 3.4 3.3</td>
<td>2.9 2.9 2.9</td>
</tr>
<tr>
<td></td>
<td>Caps req'd 0402</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.6 3.3 4.7 3.7 5.3 3.2 3.1</td>
<td>2.9 2.9 2.9</td>
</tr>
<tr>
<td></td>
<td>Caps req'd X2Y</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.0 1.0 1.0 1.0 1.0 1.0 1.0</td>
<td>1.0 1.0 1.0</td>
</tr>
</tbody>
</table>

---


7/19/2005
Outline – 9 Greatest Capacitor Myths

1. Understanding the Role of Decoupling
2. Testing Decoupling Capacitors
   ✓ Myth #1
3. Evaluating Decoupling (Capacitors-Only)
   ✓ Myth #2
   ✓ Myth #3
   ✓ Myth #4
4. PDS Placement & Mounting Parasitics
   ✓ Myth #5
   ✓ Myth #6
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
   ✓ Myth #7
   ✓ Myth #8
7. Conclusion/Questions
   ✓ Myth #9
Myth #7 – Low-inductive and multi-terminal caps are cost prohibitive.
# Component Cost vs. System Cost

<table>
<thead>
<tr>
<th>Cost/Build-of-Materials (BOM)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of cap</strong></td>
<td>X2Y® is a 1:3 to 1:7 replacement over standard MLCC Technology. (Ratio depends on PCB thickness and plane height.)</td>
</tr>
<tr>
<td><strong>Number of vias</strong></td>
<td>MLCC Technology typically used (2) vias per capacitor, where as X2Y® uses (6) vias. For a 1:3 ratio X2Y® uses the same number of via, for a 1:7 ratio X2Y® uses 6 vias and MLCC would use 14 which would be a 42.8% saving.</td>
</tr>
<tr>
<td><strong>Placement Cost</strong></td>
<td>Placement cost depends on process, materials and volume used during manufacturing and is largest and hardest value to quantify.</td>
</tr>
<tr>
<td><strong>PCB real-estate</strong></td>
<td>X2Y® saves space.</td>
</tr>
<tr>
<td><strong>Number of layers for routing</strong></td>
<td>Fewer vias for capacitor allows for more room for routing.</td>
</tr>
<tr>
<td><strong>Assembly time</strong></td>
<td>Fewer capacitors reduces assembly time.</td>
</tr>
<tr>
<td><strong>Number solder joints</strong></td>
<td>Fewer solder joints reduces assembly time.</td>
</tr>
<tr>
<td><strong>Number via drills</strong></td>
<td>Fewer via drills reduces assembly time and cost.</td>
</tr>
<tr>
<td><strong>Number pick-and-place machines</strong></td>
<td>Fewer capacitors reduces the number of pick-and-place machines needed in production (capital cost).</td>
</tr>
<tr>
<td><strong>Reliability</strong></td>
<td>Reliability affects warranty cost, manufacturing cost, and customer satisfaction.</td>
</tr>
<tr>
<td><strong>Number of attachments</strong></td>
<td>Reducing the number of attachments on PCB improves reliability.</td>
</tr>
<tr>
<td><strong>solder joints</strong></td>
<td>Reducing the number of solder joints on PCB improves reliability.</td>
</tr>
<tr>
<td><strong>Number of vias</strong></td>
<td>Reducing the number of vias on PCB improves reliability.</td>
</tr>
<tr>
<td><strong>Number of components</strong></td>
<td>Reducing the number of components on PCB improves reliability.</td>
</tr>
</tbody>
</table>
Summary Myth #7 – Low-inductive and multi-terminal caps are cost prohibitive.

- Component cost-only – low-inductive caps cost more.
- System cost – low-inductive caps (IPDs) offer substantial cost savings.
Multi-plane Decoupling

- Decoupling multiple power planes on PCB increases the number of standard caps needed.
- A single X2Y® can be used for 2 different power planes.
Myth #8 – Multiple power planes require more decoupling capacitors.
Cost/Build-of-Materials (BOM)

Note: Scale differences.
X2Y® crosstalk

Circuit 1

Cost/Build-of-Materials (BOM)
Summary **Myth #8** – Multiple power plane require more decoupling capacitors.

- All power planes require decoupling caps.
- Conventional capacitor technology can only decouple one plane.
- Using X2Y®’s differential property can simultaneously decouple 2 power planes, significantly reducing the number of caps typically required.

**But**
Outline – 9 Greatest Capacitor Myths

1. Understanding the Role of Decoupling
2. Testing Decoupling Capacitors
   ✓ Myth #1
3. Evaluating Decoupling (Capacitors-Only)
   ✓ Myth #2
   ✓ Myth #3
   ✓ Myth #4
4. PDS Placement & Mounting Parasitics
   ✓ Myth #5
   ✓ Myth #6
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
   ✓ Myth #7
   ✓ Myth #8
7. Conclusion/Questions
   ✓ Myth #9
Myth #9 – X2Y® is just a capacitor.
X2Y® Technology – Circuit 1 & Circuit 2

- Capacitive Circuit
  - Circuit 1 – 3 conductor
  - Circuit 2 – 2 conductor
- 4 terminal device
- Layout attachment is inter-digitated
- Note: X2Y® in this presentation has been Circuit 2 unless noted (multi-plane decoupling)
**X2Y® structural features for low-inductance.**

- **Shorter** current path to ground, therefore smaller current loops.
- **Dual** current path to ground.
- **Opposing current flow** internal to the device = *cancellation of mutual inductance*.
- The X2Y footprint results in lower mounted inductance.
X2Y® Structural Benefit – shorter path to ground, which creates a smaller current loop when attached to the PCB.

SRF 17MHz = 880pH
SRF 19MHz = 700pH

- Standard capacitor
- X2Y - Shorter current path with one ground
X2Y® Structural Benefit – dual ground connection to the PCB.

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>S21 (dB)</th>
<th>Standard capacitor</th>
<th>X2Y - Shorter current path with one ground</th>
<th>X2Y - Shorter current path with dual ground</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>-70</td>
<td>-70</td>
<td>-70</td>
<td>-70</td>
</tr>
<tr>
<td>0.1</td>
<td>-60</td>
<td>-60</td>
<td>-60</td>
<td>-60</td>
</tr>
<tr>
<td>1</td>
<td>-50</td>
<td>-50</td>
<td>-50</td>
<td>-50</td>
</tr>
<tr>
<td>10</td>
<td>-40</td>
<td>-40</td>
<td>-40</td>
<td>-40</td>
</tr>
<tr>
<td>100</td>
<td>-30</td>
<td>-30</td>
<td>-30</td>
<td>-30</td>
</tr>
<tr>
<td>1000</td>
<td>-20</td>
<td>-20</td>
<td>-20</td>
<td>-20</td>
</tr>
<tr>
<td>10000</td>
<td>-10</td>
<td>-10</td>
<td>-10</td>
<td>-10</td>
</tr>
</tbody>
</table>

SRF 17MHz = 880pH

SRF 22MHz = 520pH
X2Y® Structural Benefit – opposing current flow to a single ground connection and resulting benefit of flux cancellation.
**X2Y® Structural Benefit** – opposing current flow to a dual ground connection and resulting benefit of flux cancellation.
## X2Y® vs. other IPD (Integrated Passive Devices)

### The X2Y® Technology Advantage

<table>
<thead>
<tr>
<th></th>
<th>X2Y® Technology</th>
<th>Other IPD</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Package Size</strong></td>
<td>Can be manufactured in any package size and still maintain low-inductive performance.</td>
<td>Limited to 0612 or smaller package size to maintain low-inductive performance.</td>
</tr>
<tr>
<td><strong>Capacitance Value</strong></td>
<td>Can be manufactured in any capacitive value current technology allows and still maintain low-inductive performance due to package size advantage.</td>
<td>Limited to smaller package sizes for low-inductive performance, thus limited to the amount of capacitance smaller package sizes will allow.</td>
</tr>
<tr>
<td><strong>Number of Terminations</strong></td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td><strong>Number of Solder Joints</strong></td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td><strong>Number of Vias</strong></td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td><strong>Via Size</strong></td>
<td>Any</td>
<td>Small or micro-vias, large vias increase pad inductance.</td>
</tr>
<tr>
<td><strong>Low-Inductance</strong></td>
<td>Premier</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Sourcing</strong></td>
<td>Multiple Manufactures</td>
<td>Single Sourced</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>Good value</td>
<td>Expensive</td>
</tr>
</tbody>
</table>
Summary **Myth #9** – X2Y® is just a capacitor.

- X2Y® is a capacitive circuit capable of different modes of operation (Circuit 1 & Circuit 2).
- X2Y® requires connections at all 4 terminals to fully realize the performance benefits.
- X2Y® is the premier IPD Technology.
- For more application information on the X2Y® Technology go to [www.x2y.com](http://www.x2y.com).
Additional Resources


- X2Y Application Note #3001 - X2Y® Solution for Decoupling Printed Circuit Boards.

- Johnson, Howard, “Parasitic Inductance of a Bypass Capacitor II.”

