Decoupling Capacitors, A Designer’s Roadmap to Optimal Decoupling Networks for Integrated Circuits

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Dale L. Sanders, Applications Engineer – X2Y Attenuators, LLC.
Panel Discussion on Decoupling Capacitors – Are you Missing the Boat?

Low-Inductance caps are useless

I’m waiting for a majority before I take a stand on the issue

Inductance should be measured “in system”

Here we go again

The real issue is “Big V” vs. “Little V”

“Carpet Bombing” with capacitors reduces design time

Inductance is over-exaggerated
Outline

1. Understanding the Role of Decoupling
2. Testing Decoupling Capacitors
3. Evaluating Decoupling (Capacitors-Only)
4. PDS Placement & Mounting Parasitics
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
7. X2Y® Components (Overview)
8. IC Conducted/Radiated Emissions (Filtering)
9. Conclusion/Questions
Understanding the Role of Decoupling

Power Distribution System (PDS)

• Is not a perfect DC supply due to parasitics.
• PDS needs defined voltage levels that include max & min values to ensure IC functionality.
• Voltage levels require the PDS to have a target impedance.
• Capacitors are used to meet target impedances to prevent:
  ▪ Current Ripples – supply instantaneous current (energy).
  ▪ Bypass transients – filter high frequency switching noise.
• Decoupling capacitors consist of:
  - Large value caps – bulk caps (mid-freq).
  - Small value caps – bypass/H.F. caps (high-freq).

Understanding the Role of Decoupling

What are the PDS design issues?

- Inductance
  - Caps
  - Vias
  - Component mounting
  - PCB plane
  - Package
- PCB real-estate
  - Number of caps & vias
  - Location/effectiveness
  - Placement cost
  - Multiple power planes

- Signal Integrity (SI)
  - Number of vias (routing)
  - Manufacturing cost (multiple plane PCBs)
  - Functionality
  - Time-to-Market
Understanding the Role of Decoupling

PDS Example

Outline

1. Understanding the Role of Decoupling
2. **Testing Decoupling Capacitors**
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There are 3 main tests to evaluate decoupling capacitors:

• Network Analyzer
  - Insertion Loss
• Time-Domain Analysis
  - Ripple
  - Transients
• Impedance Analyzer
  - Impedance
Test Fixtures – What is the test set-up to evaluate a capacitor?

• Without an industry standard, there are 2 main schools of thought:
  ▪ Capacitor-in-system
  ▪ Capacitor-only
Testing Decoupling Capacitors

Capacitor-in-system

• Advantages
  ▪ More “real world” measurements
  ▪ Allows vias to be included; current path in vias can be difficult to model at H.F. (specifically for multi-terminal capacitors).

• Disadvantages
  ▪ Application specific measurement
    > Limited to specific parameters – PCB (material & thickness), via size, plane stack-up, etc.
Testing Decoupling Capacitors

Capacitor-in-system

• Passive PCB
  - Insertion Loss
  - Time-Domain
  - Impedance
• Sample PCB
  - Insertion Loss
  - Time-Domain
  - Impedance
• Active PCB
  - Time-Domain
Testing Decoupling Capacitors

Capacitor-in-system – type of measurement

• Across cap
  ▪ Measure cap-only.
    > Not a true system measurement.

• PCB Edge
  ▪ Not a true system measurement for IC

• IC package dimension
  ▪ Measure PDS network.
  ▪ Allows mounting, via, and plane impedance to be included.


Lt. blue (9 & 11) – IC I/O & Core Power.
Testing Decoupling Capacitors

Capacitor-only

• Advantages
  ▪ Accurately measures capacitor
  ▪ Allows for accurate models of capacitor

• Disadvantages
  ▪ PCB structure parameters can be difficult to model.
    > Component mounting, current loops, via influence, plane stack-up, etc.
Testing Decoupling Capacitors

Capacitor-only Fixture

- Microwave solderless fixture
- Universal Multi-port Microwave Fixture
- 50 ohm coplanar/microstrip PCBs
Testing Decoupling Capacitors

Capacitor-only Measurements (de-embedding)

- Microwave fixtures allow for calibrations (TRL/TOSL) for de-embedding of the fixture if accuracy is a premium.
Testing Decoupling Capacitors

Summary

• There are no uniform industry standards to test and evaluate decoupling caps.

• Types of testing
  ▪ Time-Domain Analysis
  ▪ Network Analyzer
  ▪ Impedance Analyzer

• Types of fixtures
  ▪ Capacitor-in-system
  ▪ Capacitor-only
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Evaluating Decoupling (Capacitors-Only)

Time-Domain Input signal = 10 MHz, 1 nsec rise/fall time, 5V amplitude, 80/20 duty cycle.

- Ripple – Tantalum and Electrolytic both need 47uF {Add more capacitance} vs. 1.0uF for the MLCC.
- Transients – 1.0uF MLCC substantially improved switching transients.

Evaluating Decoupling (Capacitors-Only)

Insertion Loss – ENA 100 kHz to 8.5GHz.

- 1.0uF MLCC shows comparable or better attenuations than both the electrolytic or tantalum capacitors with 2% the capacitance value.
- Inductance inhibits the transfer of energy (current) out of the cap.

Summary

• Adding more capacitance will improve the ripple thus lowering the insertion loss/impedance at lower frequencies.
• However, capacitor parasitic inductance affects:
  ▪ The efficiency of energy transfer out of the capacitor.
  ▪ Reduces high frequency transient response.
• ESR is a concern, however, inductance should also be considered.
• MLCC Technology
  ▪ Can significantly reduce the amount of capacitance required in a circuit.
  ▪ Can be manufactured with comparable capacitance values as electrolytic and tantalum for decoupling applications.
Smaller is better – 0603 has less inductance than 0805, 1206, 1812.

- To meet total capacitance requirements typically small caps increase the number of caps needed. (Package size limits number of layers.)
- Larger number of caps require more vias & greater distance from IC. (More PCB space)

Evaluating Decoupling (Capacitors-Only)

X2Y® Technology – package size comparison.

- The X2Y Technology maintains or improves low-inductive performance as package size increases.

Evaluating Decoupling (Capacitors-Only)

The capacitance value has no affect on the inductive behavior of a cap.

- Physical geometry of the current loop through the capacitor affects the parasitic inductance.

Evaluating Decoupling (Capacitors-Only)

X2Y® Technology – capacitive value comparison.
- The X2Y Technology maintains or improves low-inductive performance as capacitive value increases.

Summary

- Std MLCC Technology – smaller package will reduce internal parasitic inductance.
- X2Y® Technology
  - Structure promotes mutual inductance cancellation that lowers over-all net inductance.
  - Inductance improves with:
    > Larger capacitance value (more layers).
    > Larger package (more layers).
Evaluating Decoupling (Capacitors-Only)

What is the performance benefit of low-inductive caps?

- Each MLCC measured individually
- Total (5) MLCC = 0.398uF
- X2Y® total capacitance value = 0.44uF
- Note: package size differences

- MLCC cumulative measured
- Total (5) MLCC = 0.5uF
- X2Y® total capacitance value = 0.44uF
- Note: package size differences

Measurements made on 50ohm Coplanar PCB with Ground Plane.

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PDS Placement & Mounting Parasitics

PDS Example

Distance between IC and Cap:
• Larger current loop
• More inductance
• Less effective

Effects of spreading Inductance in PDS

• Using position 9 & 11 as I/O & core power position the effects of spreading inductance in the planes can be seen.
• Demonstrates why measuring across a cap for capacitor-in-system measurement isn’t accurate.

This paper uses the concept of proper capacitor placement on a PC board to improve circuit performance.

Decoupling Strategies for Printed Circuit Boards Without Power Planes

Hwan W. Shim, Theodore M. Zeef, Todd Hubing
EMC Laboratory
University Missouri-Rolla
Rolla, MO

* Presented at the August 2002 IEEE EMC Symposium, Minneapolis, MN - TU-PM-G-5, Volume 1, page 258

Note: X2Y has expanded the testing with this PC board; further information can be found at this link:
#3001 - X2Y® Solution for Decoupling Printed Circuit Boards
PDS Placement & Mounting Parasitics

- Measurements made on 50ohm Coplanar PCB with Ground Plane.

Graph showing s21 Insertion Loss (dB) vs Frequency for different capacitors and MLCCs.

- (2) Std Caps 100nF 50V (10mm)
- (2) Std Caps 100nF 50V (2mm)
- (2) X2Y 47nF 63V (10mm)
- (2) X2Y 1206 47nF 50-63V (2mm)
- MLCC 2mm
- MLCC 10mm
- X2Y® 2mm & 10mm
PDS Placement & Mounting Parasitics

End-to-End

Side-to-Side

X2Y®

Measurements made on 50ohm Coplanar PCB with Ground Plane.

(2) MLCC 1206 100nF (End-to-End)
(2) MLCC 1206 100nF (Side-by-Side)
X2Y 1206 100nF

X2Y Application Note #3001 - X2Y® Solution for Decoupling Printed Circuit Boards.

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Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners, © Freescale Semiconductor, Inc. 2005.
The X2Y® design maximizes mutual inductance to reduce parasitic inductance. Inside X2Y®, every other electrode layer within the single component body is in opposition to cancel the magnetic flux.

*Dell Patent #6,337,798*
Summary

- Distance between caps and ICs should be minimized to reduce spreading inductance.
- Distance between caps can reduce performance if external coupling occurs.
  - Use technology that minimizes external coupling (X2Y® Technology).
  - Inter-digitate current flow through std. MLCC Technology.
Reverse-Aspect-Ratio (LL) Caps – Capacitor-only

- LL caps show lower inductive performance on microstrip PCB.
Reverse-Aspect-Ratio (LL) Caps – Capacitor-in-system

- Mounted with vias, LL caps (6 vias) have the same performance as MLCC caps (4 vias).
- LL caps are limited by mounting parasitics.
Multi-Parallel Vias

- MLCC – going from 2 to 4 vias improves impedance by 150 mΩ @ 100 MHz.
PDS Placement & Mounting Parasitics

Via & Pad Geometries
- Optimized placement and routing of the vias & pads to minimize inductance.
- Considerations should include:
  - Via
    - Diameter
    - Length
    - Location
  - Trace/Pad
    - Width
    - Length

Howard Johnson, PhD, “Parasitic Inductance of a Bypass Capacitor II,” HIGH-SPEED DIGITAL DESIGN – online newsletter Vol. 6 Issue 9, Signal Consulting, Inc.
Inter-digitated vias

- Mutual inductance between vias cancel.
- Lowers overall net inductance of vias, thus mounting inductance of caps.
- Inter-digitated caps are ideal to use minimize pad/trace distance to vias.

Minimize distance between PCB planes and capacitor (Via Length).

- Extra via length between capacitor pad and PCB planes adds inductance.

Height should be minimized.
PDS Placement & Mounting Parasitics

Summary

• Lower Via/mounting Inductance
  ▪ Multiple parallel vias
  ▪ Inter-digitate vias – lower over-all net via inductance.
  ▪ Use Inter-digitated caps – to minimize pad/trace distance from cap to via.
  ▪ Minimize distance between planes and caps.
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MLCC vs. X2Y® on a Passive Xilinx FPGA PCB.

- (104) 0402 MLCC vs. (20) 0603 X2Y®
- (208) vias – MLCC vs. (120) vias – X2Y®
- Saves PCB real-estate!
# PDS with Low-Inductive Capacitors

<table>
<thead>
<tr>
<th></th>
<th>Capacitors on Component Side</th>
<th>Capacitors on Back side</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>H1</strong></td>
<td>0.005 0.020 0.005 0.020 0.005 0.012 0.012</td>
<td>0.005 0.005 0.005</td>
</tr>
<tr>
<td><strong>H2</strong></td>
<td>0.014 0.003 0.003 0.001 0.001 0.038 0.038</td>
<td>0.014 0.003 0.001</td>
</tr>
<tr>
<td><strong>S</strong></td>
<td>0.03 0.03 0.03 0.03 0.032 0.044</td>
<td>0.03 0.03 0.03</td>
</tr>
<tr>
<td><strong>D</strong></td>
<td>0.01 0.01 0.01 0.01 0.02 0.02</td>
<td>0.01 0.01 0.01</td>
</tr>
<tr>
<td><strong>K1 D/S</strong></td>
<td>0.33 0.33 0.33 0.33 0.63 0.45</td>
<td>0.33 0.33 0.33</td>
</tr>
<tr>
<td><strong>L / via pH</strong></td>
<td>318 393 76 217 40 590 629</td>
<td>1580 1530 1540</td>
</tr>
<tr>
<td><strong>L 0603</strong></td>
<td>1052 1290 662 935 579 1500 1760</td>
<td>3670 3560 3590</td>
</tr>
<tr>
<td><strong>L 0402</strong></td>
<td>952 1190 552 835 479 1400 1660</td>
<td>3570 3460 3490</td>
</tr>
<tr>
<td><strong>L X2Y</strong></td>
<td>267 355 117 223 90 435 531</td>
<td>1250 1210 1220</td>
</tr>
<tr>
<td><strong>Caps req'd 0603</strong></td>
<td>3.9 3.6 5.6 4.2 6.5 3.4 3.3</td>
<td>2.9 2.9 2.9</td>
</tr>
<tr>
<td><strong>Caps req'd 0402</strong></td>
<td>3.6 3.3 4.7 3.7 5.3 3.2 3.1</td>
<td>2.9 2.9 2.9</td>
</tr>
<tr>
<td><strong>Caps req'd X2Y</strong></td>
<td>1.0 1.0 1.0 1.0 1.0 1.0</td>
<td>1.0 1.0 1.0</td>
</tr>
</tbody>
</table>

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## Cost/Build-of-Materials (BOM)

### Component Cost vs. System Cost

<table>
<thead>
<tr>
<th>Cost/Build-of-Materials (BOM)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of cap</strong></td>
<td>X2Y® is a 1:3 to 1:7 replacement over standard MLCC Technology. (Ratio depends on PCB thickness and plane height.)</td>
</tr>
<tr>
<td><strong>Number of vias</strong></td>
<td>MLCC Technology typically used (2) vias per capacitor, where as X2Y® uses (6) vias. For a 1:3 ratio X2Y® uses the same number of via, for a 1:7 ratio X2Y® uses 6 vias and MLCC would use 14 which would be a 42.8% savings.</td>
</tr>
<tr>
<td><strong>Placement Cost</strong></td>
<td>Placement cost depends on process, materials and volume used during manufacturing and is largest and hardest value to quantify.</td>
</tr>
<tr>
<td><strong>PCB real-estate</strong></td>
<td>X2Y® saves space.</td>
</tr>
<tr>
<td><strong>Number of layers for routing</strong></td>
<td>Fewer vias for capacitor allows for more room for routing.</td>
</tr>
<tr>
<td><strong>Assembly time</strong></td>
<td>Fewer capacitors reduces assembly time.</td>
</tr>
<tr>
<td><strong>Number solder joints</strong></td>
<td>Fewer solder joints reduces assembly time.</td>
</tr>
<tr>
<td><strong>Number via drills</strong></td>
<td>Fewer via drills reduces assembly time and cost.</td>
</tr>
<tr>
<td><strong>Number pick-and-place machines</strong></td>
<td>Fewer capacitors reduces the number of pick-and-place machines needed in production (capital cost).</td>
</tr>
<tr>
<td><strong>Reliability</strong></td>
<td>Reliability affects warranty cost, manufacturing cost, and customer satisfaction.</td>
</tr>
<tr>
<td><strong>Number of attachments</strong></td>
<td>Reducing the number of attachments on PCB improves reliability.</td>
</tr>
<tr>
<td><strong>solder joints</strong></td>
<td>Reducing the number of solder joints on PCB improves reliability.</td>
</tr>
<tr>
<td><strong>Number of vias</strong></td>
<td>Reducing the number of vias on PCB improves reliability.</td>
</tr>
<tr>
<td><strong>Number of components</strong></td>
<td>Reducing the number of components on PCB improves reliability.</td>
</tr>
</tbody>
</table>
Multi-plane Decoupling

- Decoupling multiple power planes on PCB increases the number of standard caps needed.
- A single X2Y® can be used for 2 different power planes.
Cost/Build-of-Materials (BOM)

Circuit 1

Pwr 1

GND

Pwr 2

X2Y 0603 100nF

PCB Fixture
Note: Scale differences.
X2Y® crosstalk

- Circuit 1
Summary

• All power planes require decoupling caps.
• **Component cost-only** – low-inductive caps cost more.
• **System cost** – low-inductive caps (IPDs) offer substantial cost savings.
• Conventional capacitor technology can only decouple one plane.
• Using X2Y®’s differential property can simultaneously decouple 2 power planes, significantly reducing the number of caps typically required.

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X2Y® Technology – Circuit 1 & Circuit 2

• Capacitive Circuit
  ▪ Circuit 1 – 3 conductor
  ▪ Circuit 2 – 2 conductor

• 4 terminal device

• Layout attachment is inter-digitated

• Note: X2Y® in this presentation has been Circuit 2 unless noted (multi-plane decoupling)
X2Y® structural features for low-inductance.

- **Shorter** current path to ground, therefore smaller current loops.
- **Dual** current path to ground.
- **Opposing current flow** internal to the device = *cancellation of mutual inductance*.
- The X2Y footprint results in lower mounted inductance.
X2Y® Structural Benefit – shorter path to ground, which creates a smaller current loop when attached to the PCB.

- Standard capacitor
- X2Y - Shorter current path with one ground

SRF 17MHz = 880pH
SRF 19MHz = 700pH
X2Y® Components (Overview)

X2Y® Structural Benefit – dual ground connection to the PCB.

- Standard capacitor
- X2Y - Shorter current path with one ground
- X2Y - Shorter current path with dual ground

-70 -60 -50 -40 -30 -20 -10 0
0.01 0.1 1 10 100 1000 10000
s21 (dB)

SRF 17MHz = 880pH

SRF 22MHz = 520pH

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X2Y® Structural Benefit – opposing current flow to a **single** ground connection and resulting benefit of flux cancellation.

![Graph comparing standard capacitor and X2Y® capacitor performance.](image)

- **Standard capacitor**
  - SRF 17MHz = 880pH

- **X2Y® - Opposing current flow with one ground**
  - SRF 17MHz = 440pH
X2Y® Structural Benefit – opposing current flow to a **dual** ground connection and resulting benefit of flux cancellation.

- Standard capacitor
- X2Y - Opposing current flow with one ground
- X2Y - Opposing current flow with dual ground

SRF 17MHz = 880pH

SRF 34MHz = 110pH
X2Y® Components (Overview)

Time-Domain Testing (Clock Cycle)
• 50/50 Duty Cycle
• 70 ps rise/fall time
• 1 GHz Frequency
• 20 GS/s sampling rate

Data courtesy of Kevin Slattery, Intel Corporation.

<table>
<thead>
<tr>
<th>Component</th>
<th>Square Wave Peak-to-Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrolytic 10uF</td>
<td>571 mV</td>
</tr>
<tr>
<td>Tantalum 10uF</td>
<td>319 mV</td>
</tr>
<tr>
<td>Std. MLCC 10uF</td>
<td>134 mV</td>
</tr>
<tr>
<td>LL MLCC 1.0uF</td>
<td>128 mV</td>
</tr>
<tr>
<td><strong>IDC™ 1.0uF</strong></td>
<td><strong>25.3 mV</strong></td>
</tr>
<tr>
<td>X2Y® 0.56uF (1.12uF total)</td>
<td><strong>19.6 mV</strong></td>
</tr>
<tr>
<td>X2Y® 5.0uF (10uF total)</td>
<td>16.7 mV</td>
</tr>
<tr>
<td>X2Y® 6.5uF (13uF total)</td>
<td>13.2 mV</td>
</tr>
</tbody>
</table>

Time-Domain Testing (Random Pattern)

- 70 ps rise/fall time
- 1 GHz Frequency
- 20 GS/s sampling rate

Data courtesy of Kevin Slattery, Intel Corporation.

<table>
<thead>
<tr>
<th>Component</th>
<th>Random Δ Peak-to-Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrolytic 10uF</td>
<td>597 mV</td>
</tr>
<tr>
<td>Tantalum 10uF</td>
<td>311 mV</td>
</tr>
<tr>
<td>Std. MLCC 10uF</td>
<td>134 mV</td>
</tr>
<tr>
<td>LL MLCC 1.0uF</td>
<td>116 mV</td>
</tr>
<tr>
<td>IDC™ 1.0uF</td>
<td>25.3 mV</td>
</tr>
<tr>
<td>X2Y® 0.56uF (1.12uF total)</td>
<td>15.5 mV</td>
</tr>
<tr>
<td>X2Y® 5.0uF (10uF total)</td>
<td>17.2 mV</td>
</tr>
<tr>
<td>X2Y® 6.5uF (13uF total)</td>
<td>14.2 mV</td>
</tr>
</tbody>
</table>

Impedance Analyzer Measurements

- Impedance measurement taken on Agilent 4396B Impedance Analyzer
- Note: X2Y total capacitance value = 0.94uF

Data courtesy of Kevin Slattery, Intel Corporation.
# X2Y® Components (Overview)

## X2Y® vs. other IPD (Integrated Passive Devices)
- The X2Y® Technology Advantage

<table>
<thead>
<tr>
<th></th>
<th>X2Y® Technology</th>
<th>Other IPD</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Package Size</strong></td>
<td>Can be manufactured in any package size and still maintain low-inductive performance.</td>
<td>Limited to 0612 or smaller package size to maintain low-inductive performance.</td>
</tr>
<tr>
<td><strong>Capacitance Value</strong></td>
<td>Can be manufactured in any capacitve value current technology allows and still maintain low-inductive performance due to package size advantage.</td>
<td>Limited to smaller package sizes for low-inductive performance, thus limited to the amount of capacitance smaller package sizes will allow.</td>
</tr>
<tr>
<td><strong>Number of Terminations</strong></td>
<td>✅ 4</td>
<td>8</td>
</tr>
<tr>
<td><strong>Number of Solder Joints</strong></td>
<td>✅ 4</td>
<td>8</td>
</tr>
<tr>
<td><strong>Number of Vias</strong></td>
<td>✅ 6</td>
<td>8</td>
</tr>
<tr>
<td><strong>Via Size</strong></td>
<td>✅ Any</td>
<td>Small or micro-vias, large vias increase pad inductance.</td>
</tr>
<tr>
<td><strong>Low-Inductance</strong></td>
<td>✅ Premier</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Sourcing</strong></td>
<td>✅ Multiple Manufactures</td>
<td>Single Sourced</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>✅ Good value</td>
<td>Expensive</td>
</tr>
</tbody>
</table>
Summary

• X2Y® is a capacitive circuit capable of different modes of operation (Circuit 1 & Circuit 2).
• X2Y® requires connections at all 4 terminals to fully realize the performance benefits.
• X2Y® is the premier IPD Technology.
• For more application information on the X2Y® Technology go to www.x2y.com.
Outline

1. Understanding the Role of Decoupling
2. Testing Decoupling Capacitors
3. Evaluating Decoupling (Capacitors-Only)
4. PDS Placement & Mounting Parasitics
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
7. X2Y® Components (Overview)
8. IC Conducted/Radiated Emissions (Filtering)
9. Conclusion/Questions
Comparison Of Decoupling Capacitors Using A 150-ohm Measurement Resistor

IEC 61967-4 Document 47A/566/CD Measurement of conducted emissions, 1 ohm/150 ohm direct coupling method

- No Decoupling Caps
- Bottom-Layer Caps (4x100nF)
- Top-Layer Caps (5x100nF)
- X2Y (5x100nF)
IC Conducted/Radiated Emissions (Filtering)

Existing Structures – “quasi” Faraday Cage

• Lead frame
• Heat sinks
• Image planes
• Housings

The Heat Sink and Lead Frame Create a Faraday Cage.

The PCB Trace/Plane and Lead Frame Create a Faraday Cage.

X2Y Application Note #3002 - IC Decoupling and EMI Suppression using X2Y® Technology
Applying X2Y® to cancel emissions

- “A” and “B” terminal attach to power and ground
- “G1” and “G2” attach to Faraday Cage structure (i.e. image plane, heatsink, lead frame, housing).

**Circuit 1**

```
  Pwr
 /   \\  
|     |
Faraday Cage
  \   /
    Rtn
```

For optimum performance, a low-inductance shorting or canceling device should be used between Pwr, GND, and Image Strip. The low-inductive device can be placed internally or externally of the IC package.
IC Radiated Emissions Testing

IEC 68167: Integrated Circuits, Measurement of radiated emissions - TEM-cell and wideband TEM-cell method

Test Board looking from Inside of TEM-cell

Test Board looking from outside of TEM-cell

ETS-LINDGREN GTEM Model 5402  www.emctest.com
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Questions?
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Additional Resources

- X2Y Application Note #3001 - X2Y® Solution for Decoupling Printed Circuit Boards.
- Johnson, Howard, “Parasitic Inductance of a Bypass Capacitor II,”