

Orlando  
2005

# Freescale Technology Forum

Network. Connect. Explore.

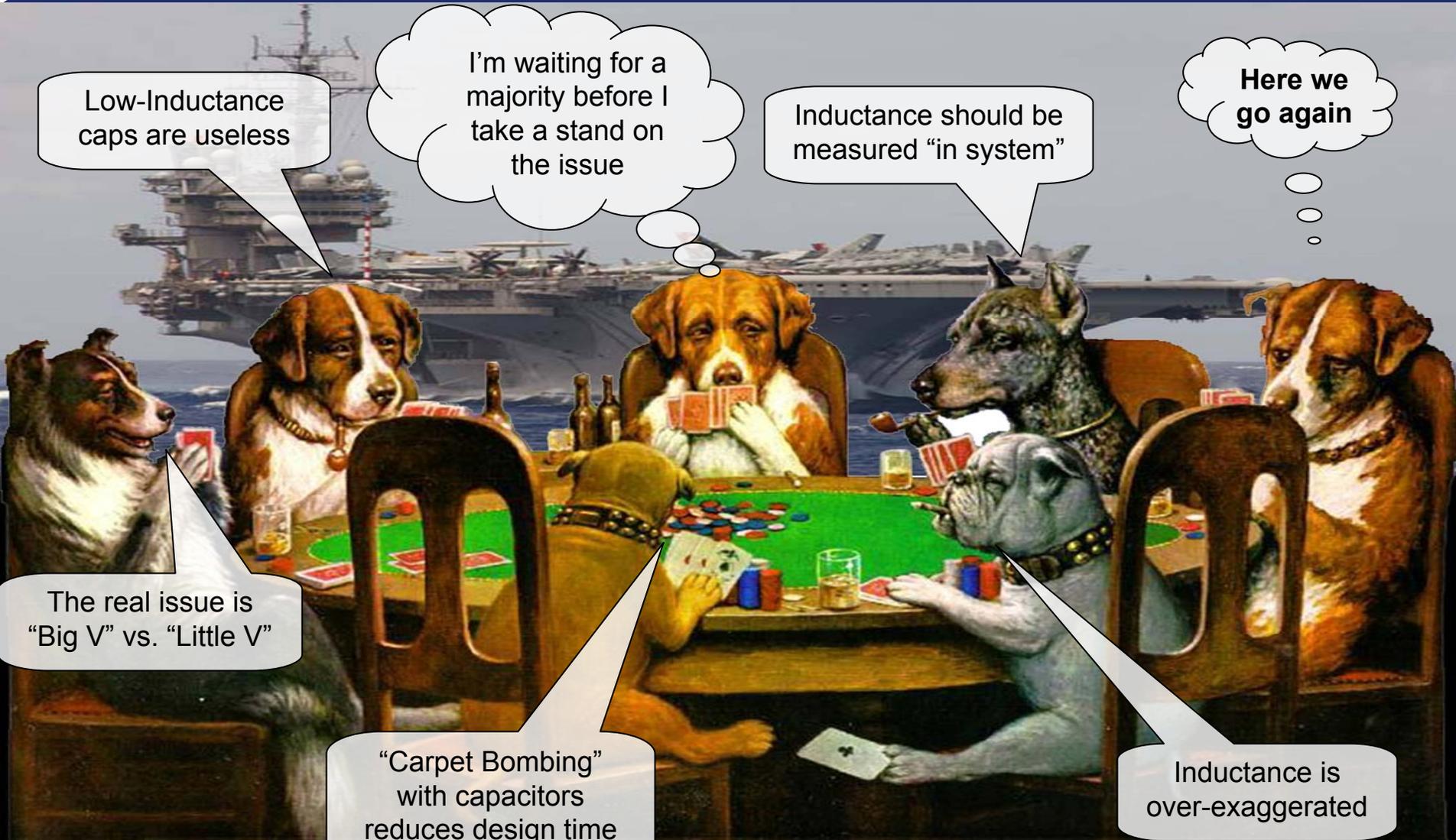
Decoupling Capacitors, A  
Designer's Roadmap to Optimal  
Decoupling Networks for  
Integrated Circuits



James P. Muccioli, CTO – X2Y Attenuators, LLC.

Dale L. Sanders, Applications Engineer – X2Y Attenuators, LLC.

# Panel Discussion on Decoupling Capacitors – Are you Missing the Boat?



Low-Inductance caps are useless

I'm waiting for a majority before I take a stand on the issue

Inductance should be measured "in system"

Here we go again

The real issue is "Big V" vs. "Little V"

"Carpet Bombing" with capacitors reduces design time

Inductance is over-exaggerated

1. **Understanding the Role of Decoupling**
2. Testing Decoupling Capacitors
3. Evaluating Decoupling (Capacitors-Only)
4. PDS Placement & Mounting Parasitics
5. PDS with Low-Inductance Capacitors
6. Cost/Build-of-Materials (BOM)
7. X2Y<sup>®</sup> Components (Overview)
8. IC Conducted/Radiated Emissions (Filtering)
9. Conclusion/Questions

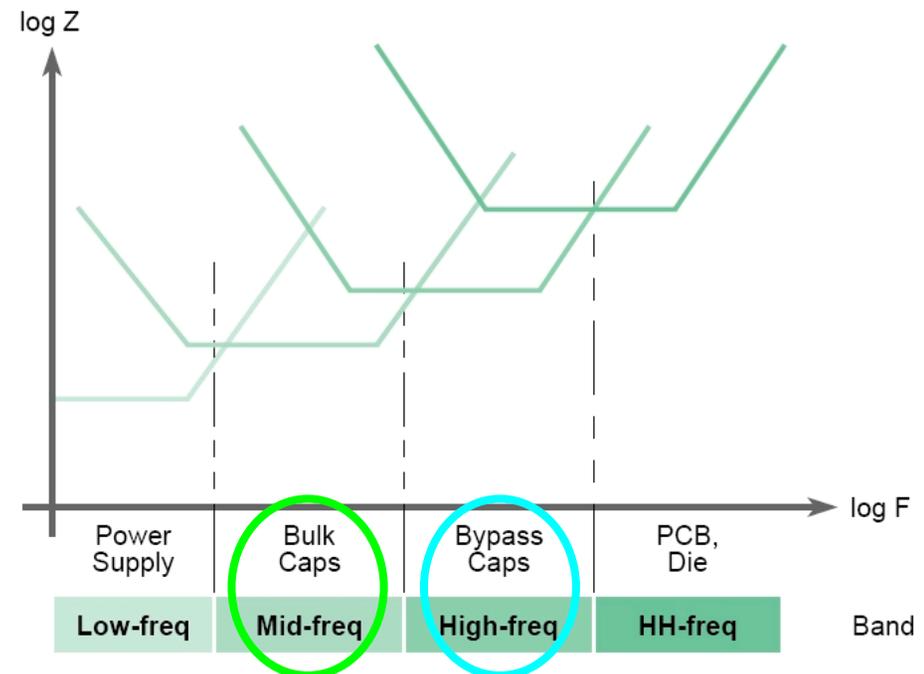
# Understanding the Role of Decoupling

## Power Distribution System (PDS)

- Is not a perfect DC supply due to parasitics.
- PDS needs defined voltage levels that include max & min values to ensure IC functionality.
- Voltage levels require the PDS to have a target impedance.
- Capacitors are used to meet target impedances to prevent:
  - Current Ripples – supply instantaneous current (energy).
  - Bypass transients – filter high frequency switching noise.

# Understanding the Role of Decoupling

- Decoupling capacitors consist of:
  - Large value caps – bulk caps (mid-freq).
  - Small value caps – bypass/H.F. caps (high-freq).



Milliorn, Gary, "[Power Supply Design for PowerPCTM Processors](#)," Freescale Semiconductor Application Note AN2447, Rev. 1.1, Sept 2004.

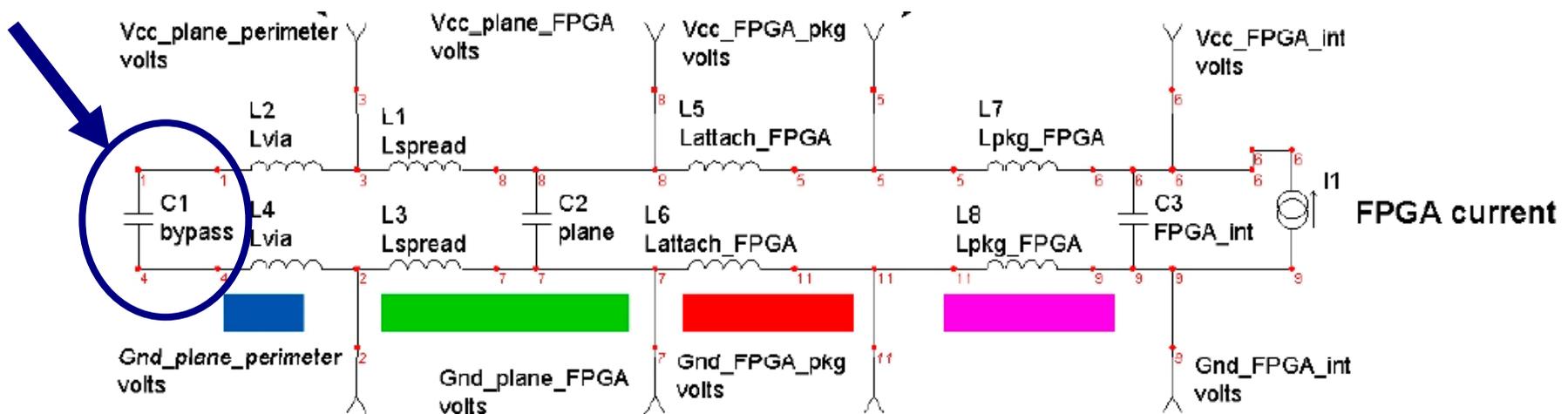
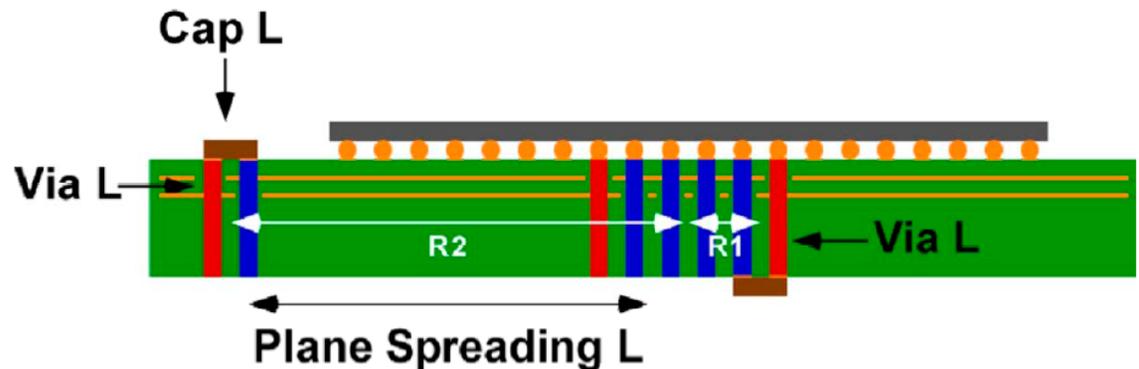
# Understanding the Role of Decoupling

## What are the PDS design issues?

- Inductance
  - Caps
  - Vias
  - Component mounting
  - PCB plane
  - Package
- PCB real-estate
  - Number of caps & vias
  - Location/effectiveness
  - Placement cost
  - Multiple power planes
- Signal Integrity (SI)
  - Number of vias (routing)
  - Manufacturing cost (multiple plane PCBs)
  - Functionality
  - Time-to-Market

# Understanding the Role of Decoupling

## PDS Example



Steve Weir, Scott McMorow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

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## There are 3 main tests to evaluate decoupling capacitors:

- Network Analyzer
  - Insertion Loss
- Time-Domain Analysis
  - Ripple
  - Transients
- Impedance Analyzer
  - Impedance

## Test Fixtures – What is the test set-up to evaluate a capacitor?

- Without an industry standard, there are 2 main schools of thought:
  - Capacitor-in-system
  - Capacitor-only

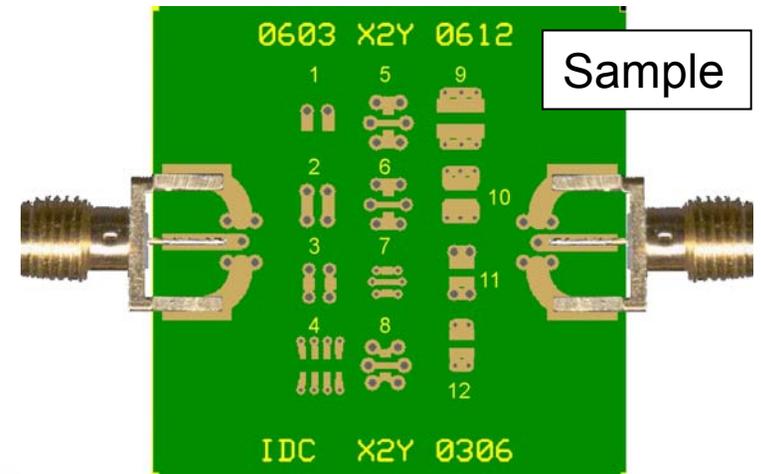
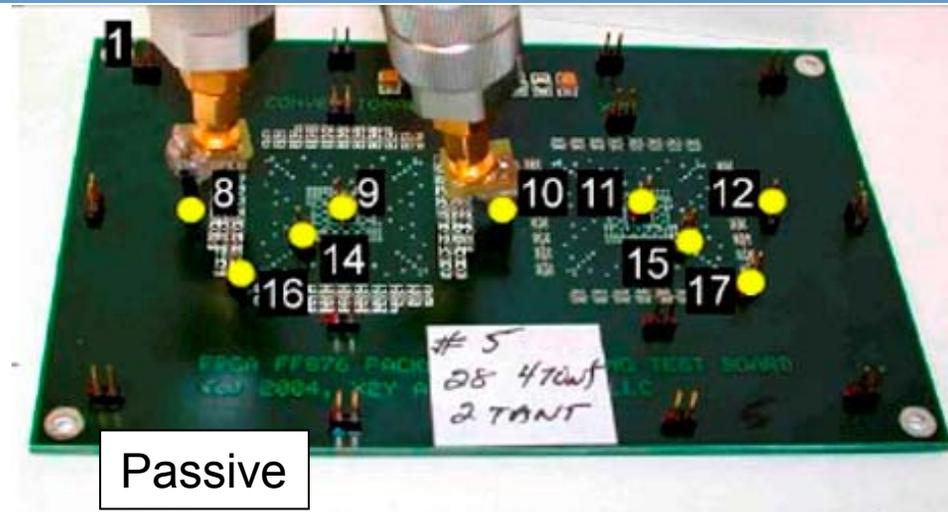
## Capacitor-in-system

- Advantages
  - More “real world” measurements
  - Allows vias to be included; current path in vias can be difficult to model at H.F. (specifically for multi-terminal capacitors).
- Disadvantages
  - Application specific measurement
    - > Limited to specific parameters – PCB (material & thickness), via size, plane stack-up, etc.

# Testing Decoupling Capacitors

## Capacitor-in-system

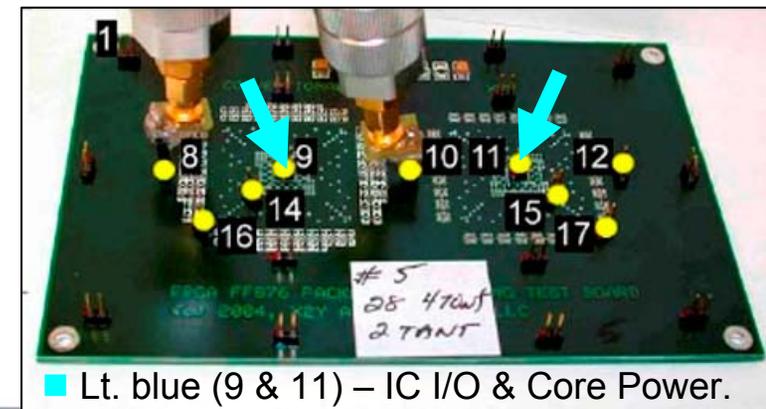
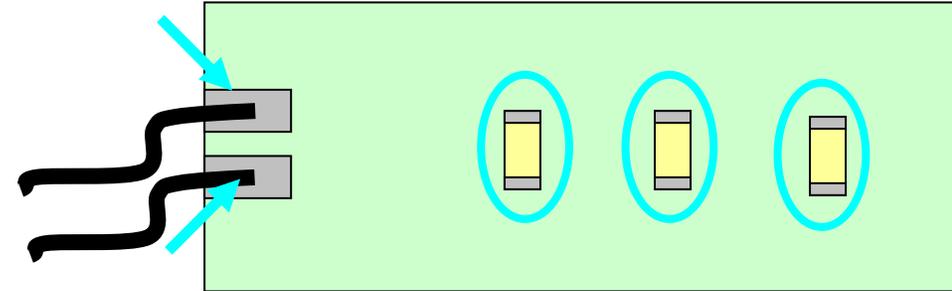
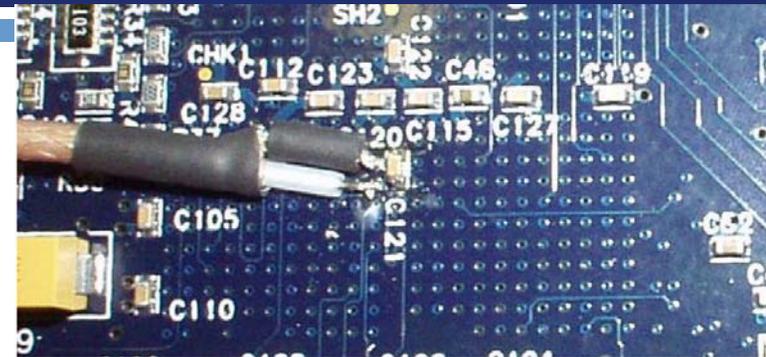
- Passive PCB
  - Insertion Loss
  - Time-Domain
  - Impedance
- Sample PCB
  - Insertion Loss
  - Time-Domain
  - Impedance
- Active PCB
  - Time-Domain



# Testing Decoupling Capacitors

## Capacitor-in-system – type of measurement

- Across cap
  - Measure cap-only.
    - > Not a true system measurement.
- PCB Edge
  - Not a true system measurement for IC
- IC package dimension
  - Measure PDS network.
  - Allows mounting, via, and plane impedance to be included.



■ Lt. blue (9 & 11) – IC I/O & Core Power.

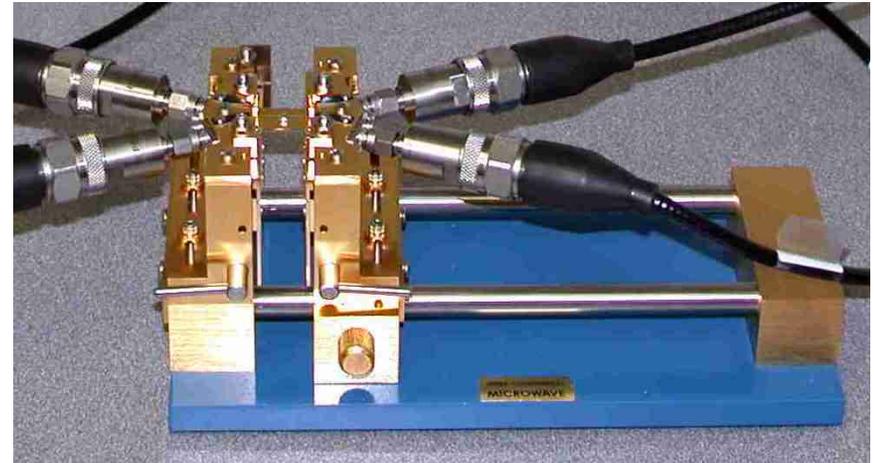
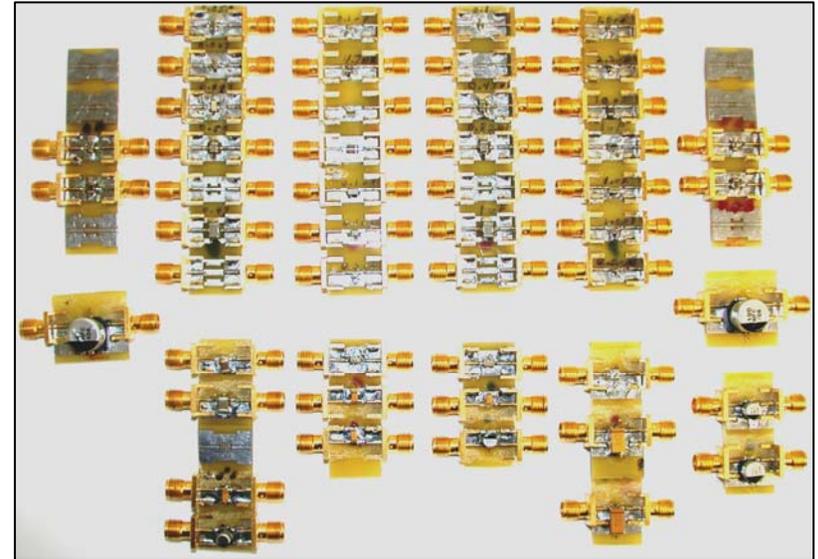
## Capacitor-only

- Advantages
  - Accurately measures capacitor
  - Allows for accurate models of capacitor
- Disadvantages
  - PCB structure parameters can be difficult to model.
    - > Component mounting, current loops, via influence, plane stack-up, etc.

# Testing Decoupling Capacitors

## Capacitor-only Fixture

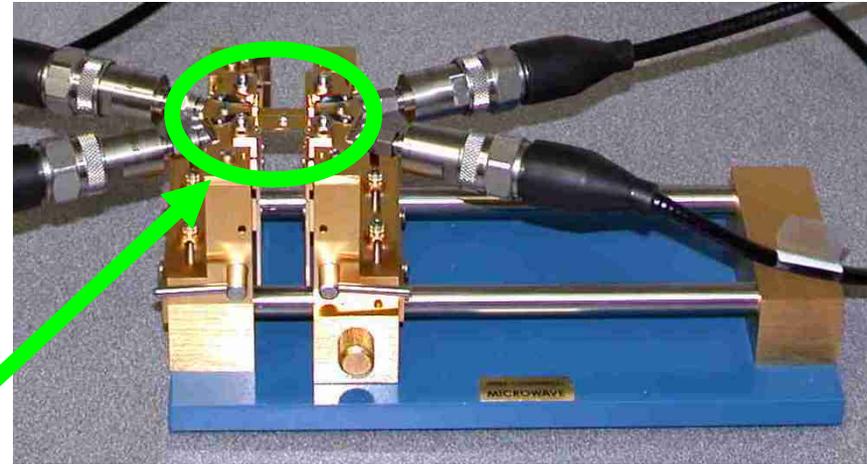
- Microwave solderless fixture
- Universal Multi-port Microwave Fixture
- 50 ohm coplanar/microstrip PCBs



# Testing Decoupling Capacitors

## Capacitor-only Measurements (de-embedding)

- Microwave fixtures allow for calibrations (TRL/TOSL) for de-embedding of the fixture if accuracy is a premium.



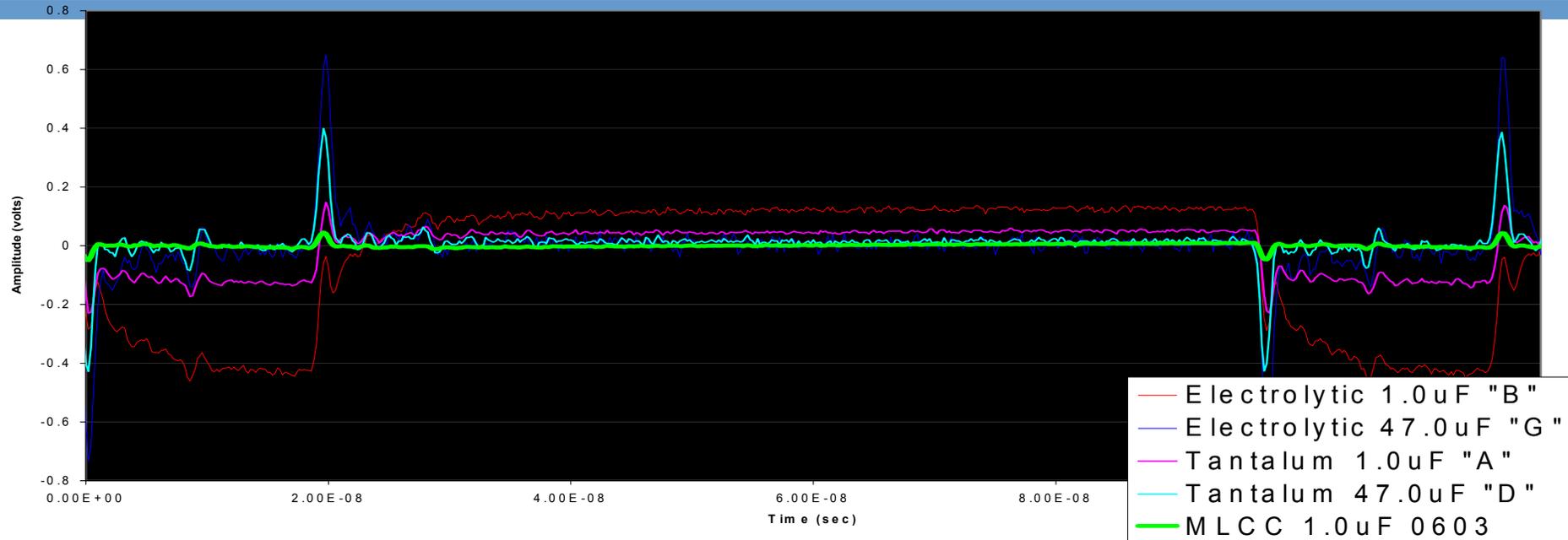
**CAL Standards**

## Summary

- There are no uniform industry standards to test and evaluate decoupling caps.
- Types of testing
  - Time-Domain Analysis
  - Network Analyzer
  - Impedance Analyzer
- Types of fixtures
  - Capacitor-in-system
  - Capacitor-only

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# Evaluating Decoupling (Capacitors-Only)

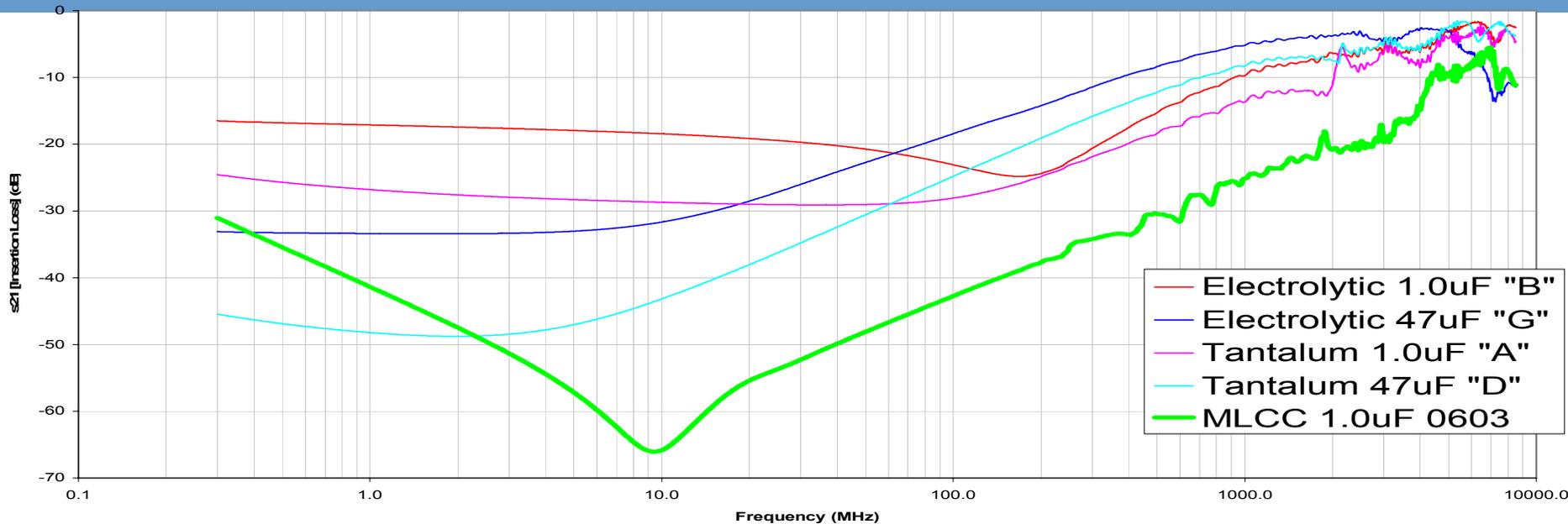


**Time-Domain Input signal = 10 MHz, 1 nsec rise/fall time, 5V  
applitude, 80/20 duty cycle.**

- Ripple – Tantalum and Electrolytic both need 47uF {Add more capacitance} vs. 1.0uF for the MLCC.
- Transients – 1.0uF MLCC substantially improved switching transients.

Sanders, Muccioli, North, and Slattery, "[The Quantitative Measurement of the Effectiveness of Decoupling Capacitors in Controlling Switching Transients from Microprocessors](#)," CARTS 2005 USA, Palm Springs, CA, March 2005.

# Evaluating Decoupling (Capacitors-Only)



## Insertion Loss – ENA 100 kHz to 8.5GHz.

- 1.0uF MLCC shows comparable or better attenuations than both the electrolytic or tantalum capacitors with 2% the capacitance value.
- Inductance inhibits the transfer of energy (current) out of the cap.

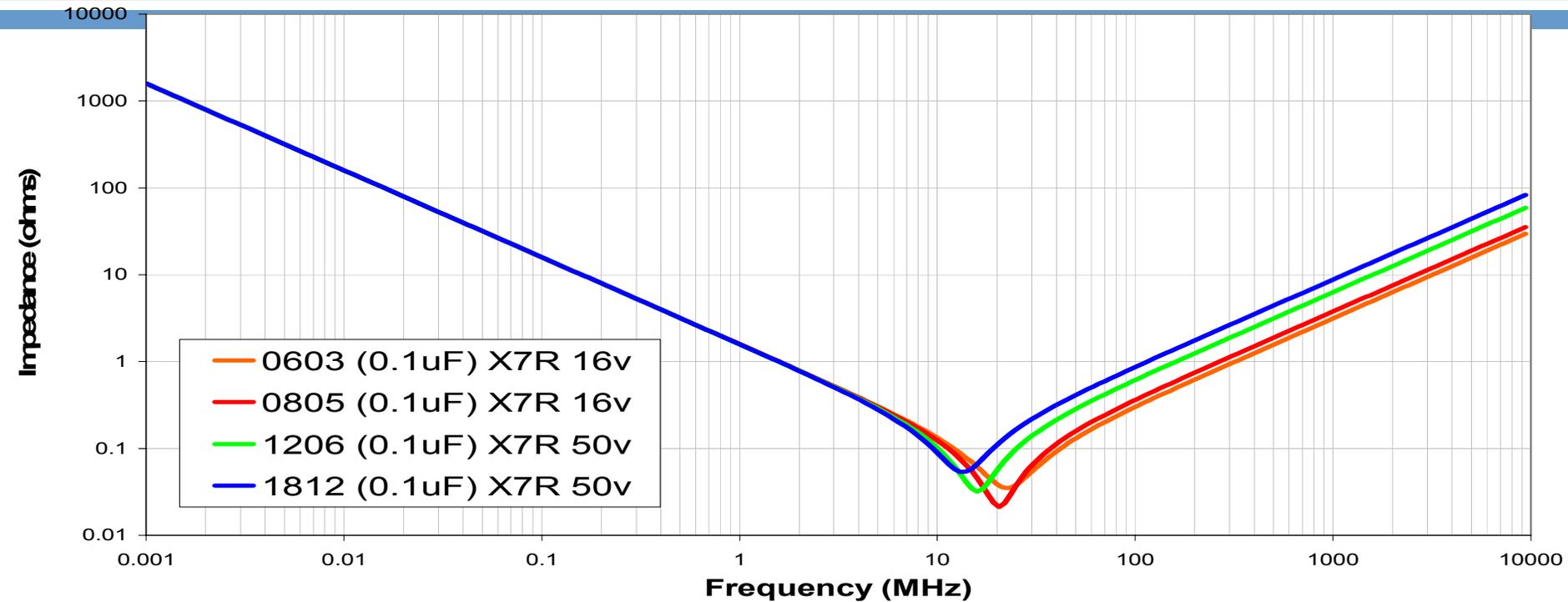
Sanders, Muccioli, North, and Slattery, " [The Quantitative Measurement of the Effectiveness of Decoupling Capacitors in Controlling Switching Transients from Microprocessors](#)," CARTS 2005 USA, Palm Springs, CA, March 2005.

# Evaluating Decoupling (Capacitors-Only)

## Summary

- Adding more capacitance will improve the ripple thus lowering the insertion loss/impedance at lower frequencies.
- However, capacitor parasitic inductance affects:
  - The efficiency of energy transfer out of the capacitor.
  - Reduces high frequency transient response.
- ESR is a concern, however, inductance should also be considered.
- MLCC Technology
  - Can significantly reduce the amount of capacitance required in a circuit.
  - Can be manufactured with comparable capacitance values as electrolytic and tantalum for decoupling applications.

# Evaluating Decoupling (Capacitors-Only)

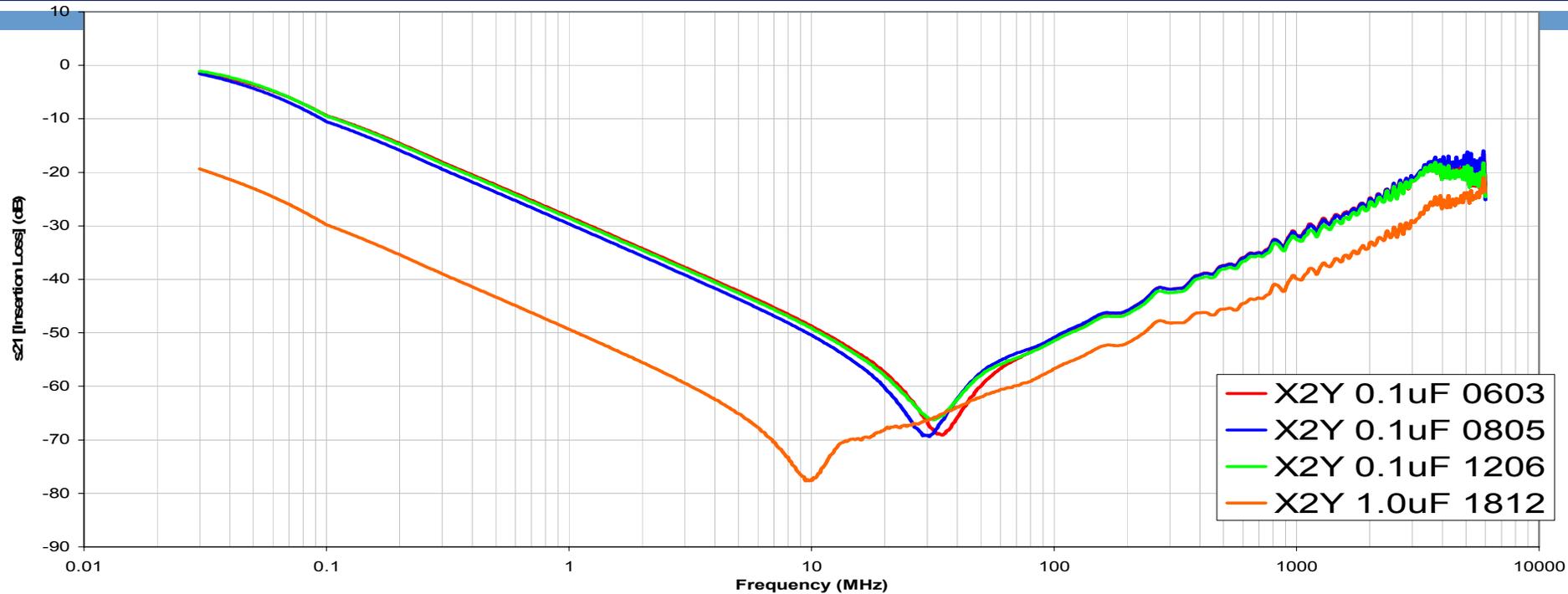


**Smaller is better – 0603 has less inductance than 0805, 1206, 1812.**

- To meet total capacitance requirements typically small caps increase the number of caps needed. (Package size limits number of layers.)
- Larger number of caps require more vias & greater distance from IC. (More PCB space)

D.L. Sanders, J.P. Muccioli, A.A. Anthony, and D.J. Anthony, "[X2Y® Technology Used for Decoupling](#)," Published by the IEE, New EMC issues in Design: Techniques, Tools and Components Event Symposium, April 28, 2004.

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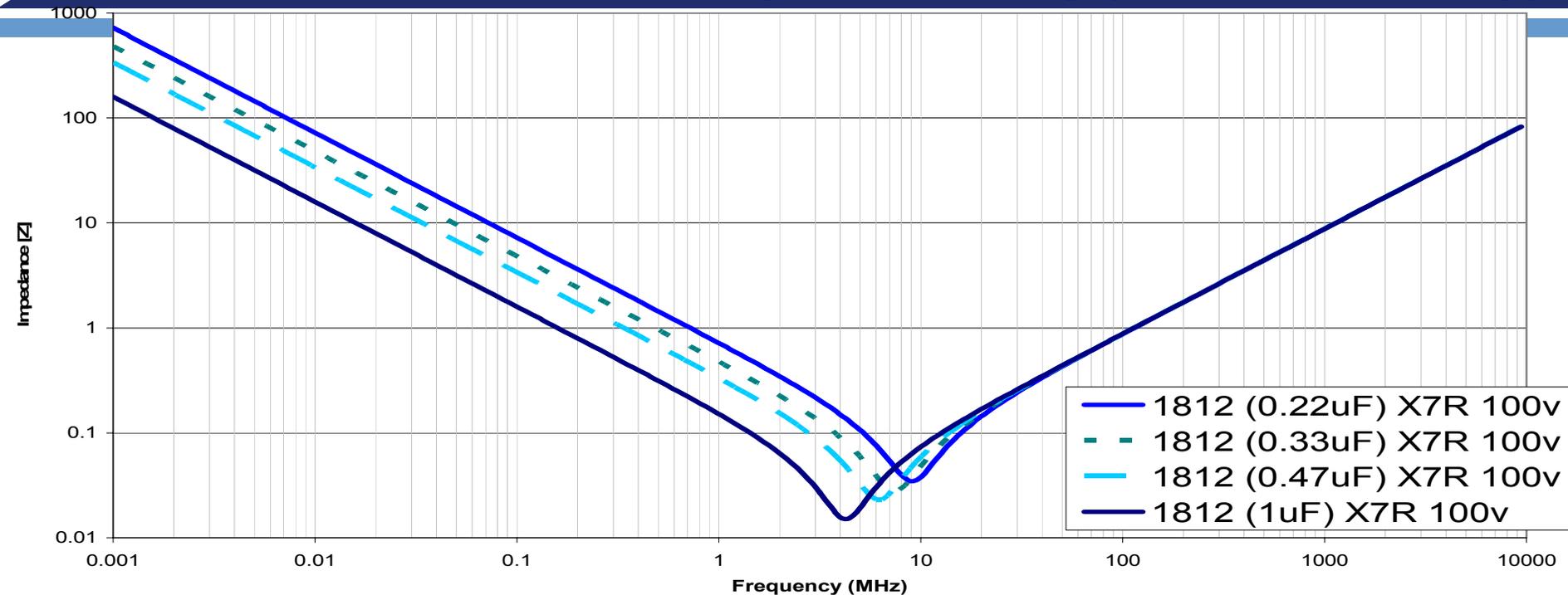


## X2Y<sup>®</sup> Technology – package size comparison.

- The X2Y Technology maintains or improves low-inductive performance as package size increases.

D.L. Sanders, J.P. Muccioli, A.A. Anthony, and D.J. Anthony, "[X2Y<sup>®</sup> Technology Used for Decoupling](#)," Published by the IEE, New EMC issues in Design: Techniques, Tools and Components Event Symposium, April 28, 2004.

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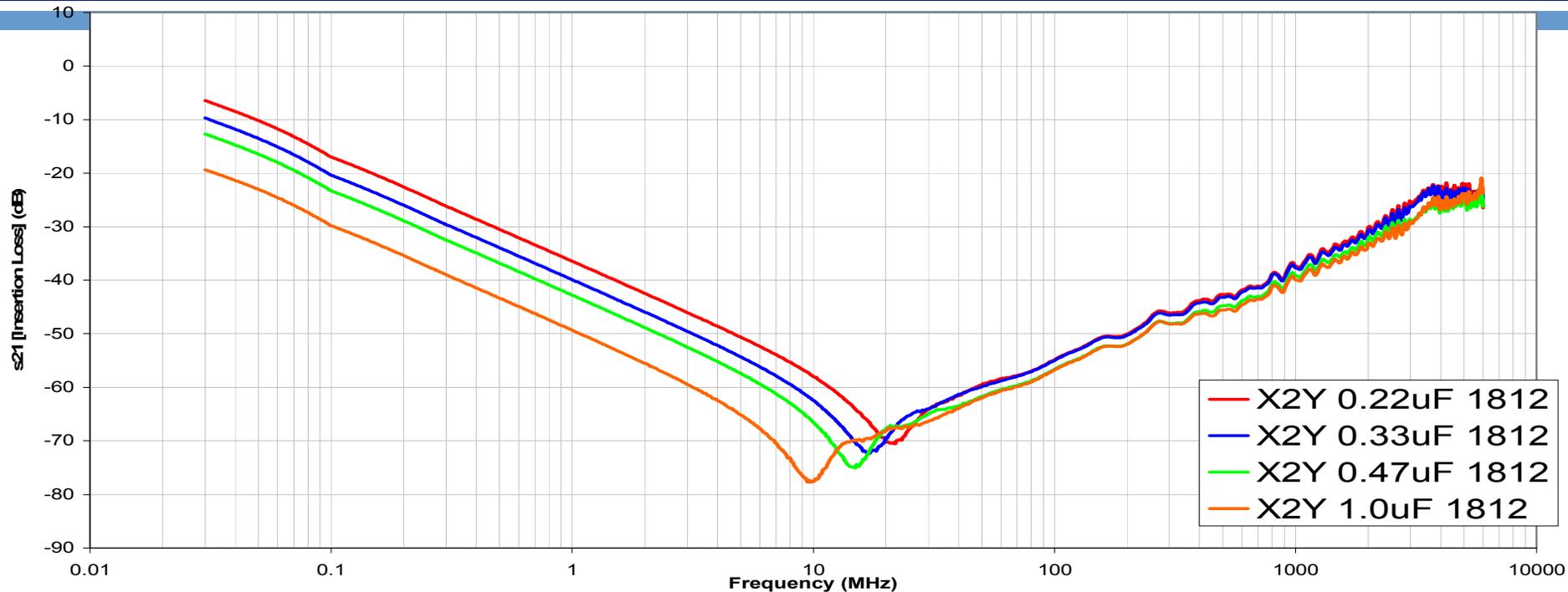


**The capacitance value has no affect on the inductive behavior of a cap.**

- Physical geometry of the current loop through the capacitor affects the parasitic inductance.

D.L. Sanders, J.P. Muccioli, A.A. Anthony, and D.J. Anthony, "[X2Y® Technology Used for Decoupling](#)," Published by the IEE, New EMC issues in Design: Techniques, Tools and Components Event Symposium, April 28, 2004.

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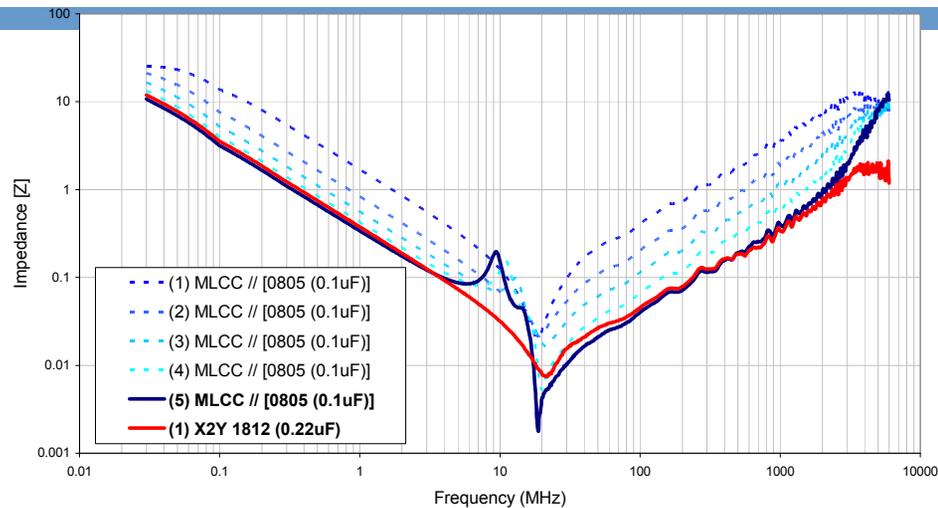
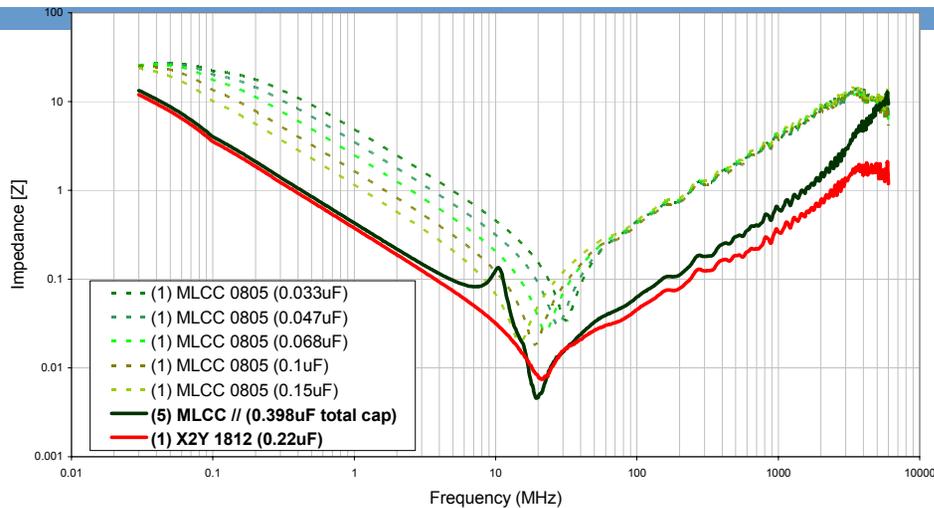
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# Evaluating Decoupling (Capacitors-Only)

## Summary

- Std MLCC Technology – smaller package will reduce internal parasitic inductance.
- X2Y<sup>®</sup> Technology
  - Structure promotes mutual inductance cancellation that lowers over-all net inductance.
  - Inductance improves with:
    - > Larger capacitance value (more layers).
    - > Larger package (more layers).

# Evaluating Decoupling (Capacitors-Only)



## What is the performance benefit of low-inductive caps?

- Each MLCC measured individually
- Total (5) MLCC = 0.398uF
- X2Y<sup>®</sup> total capacitance value = 0.44uF
- Note: package size differences

- MLCC cumulative measured
- Total (5) MLCC = 0.5uF
- X2Y<sup>®</sup> total capacitance value = 0.44uF
- Note: package size differences



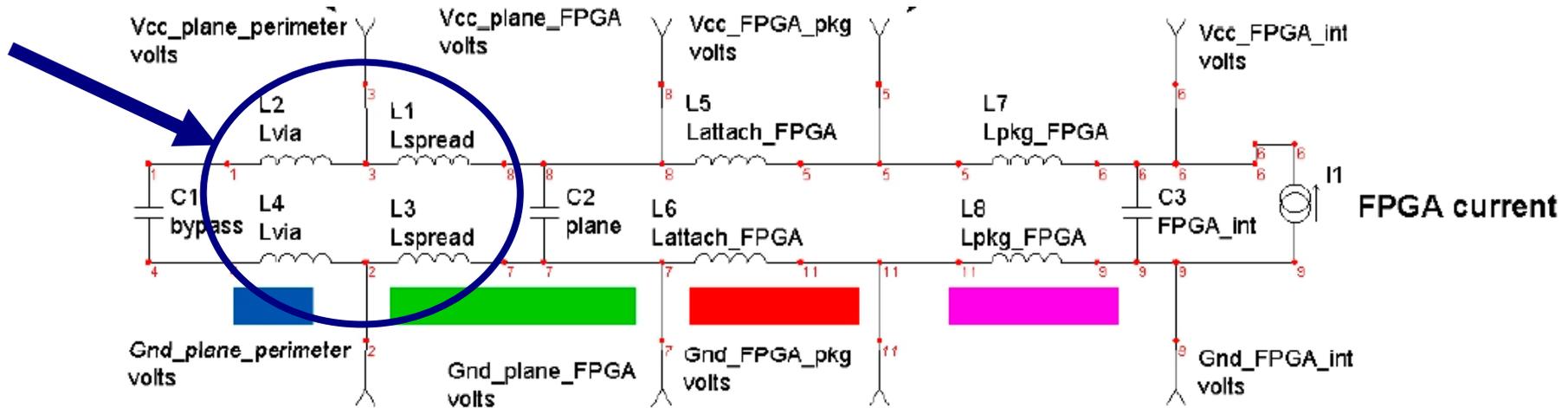
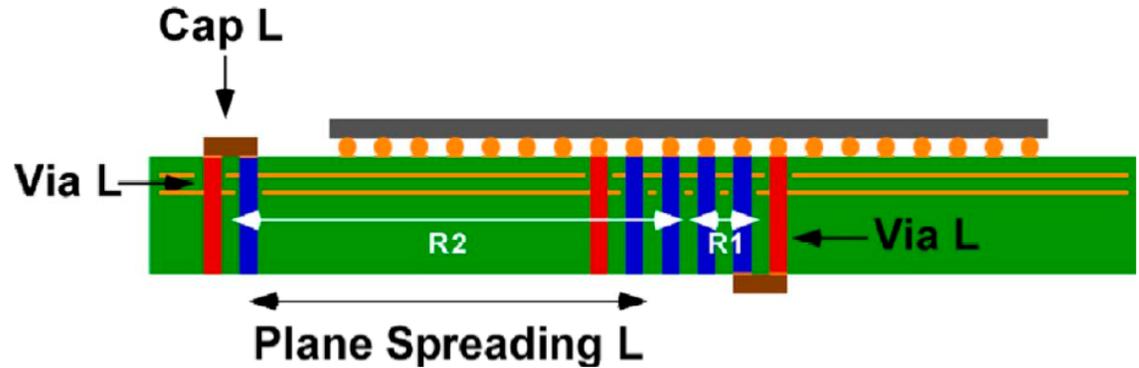
✓ Measurements made on 50ohm Coplanar PCB with Ground Plane.

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# PDS Placement & Mounting Parasitics

## PDS Example

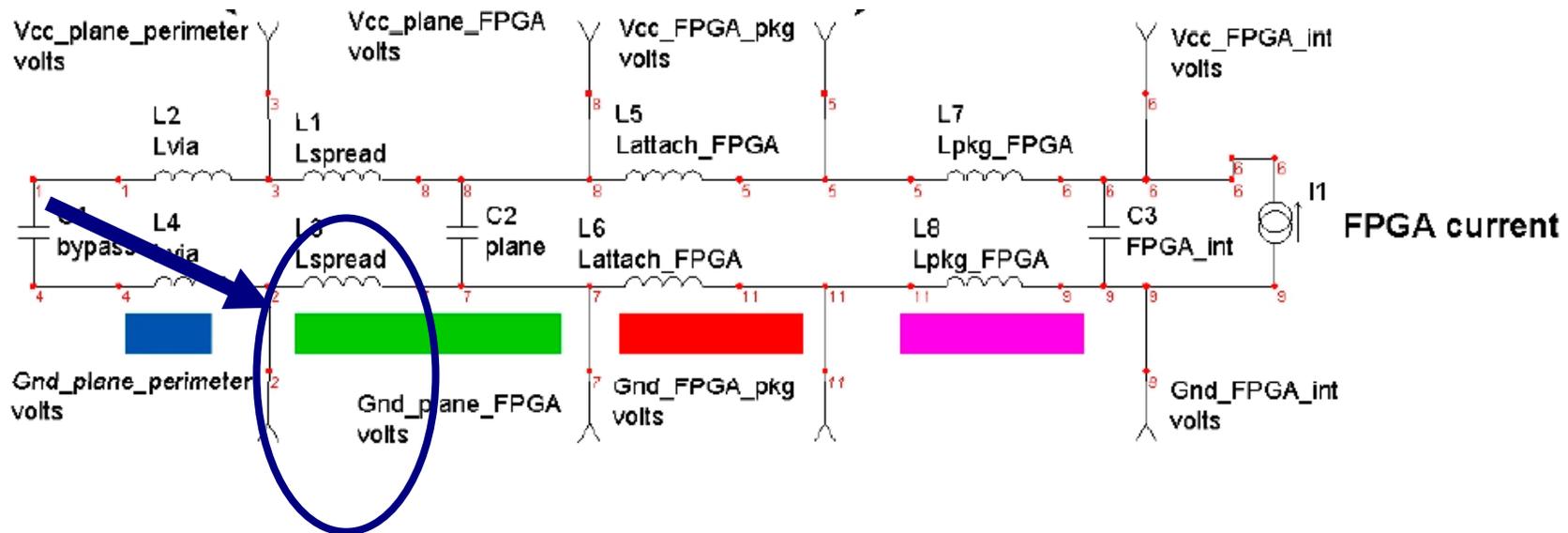
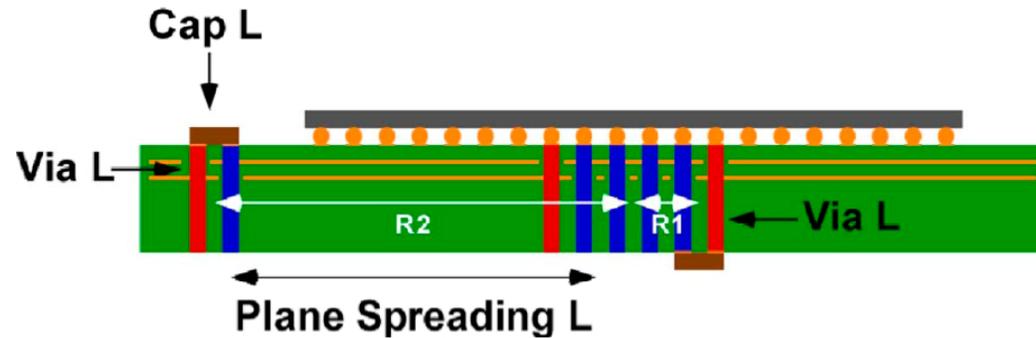


Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

# PDS Placement & Mounting Parasitics

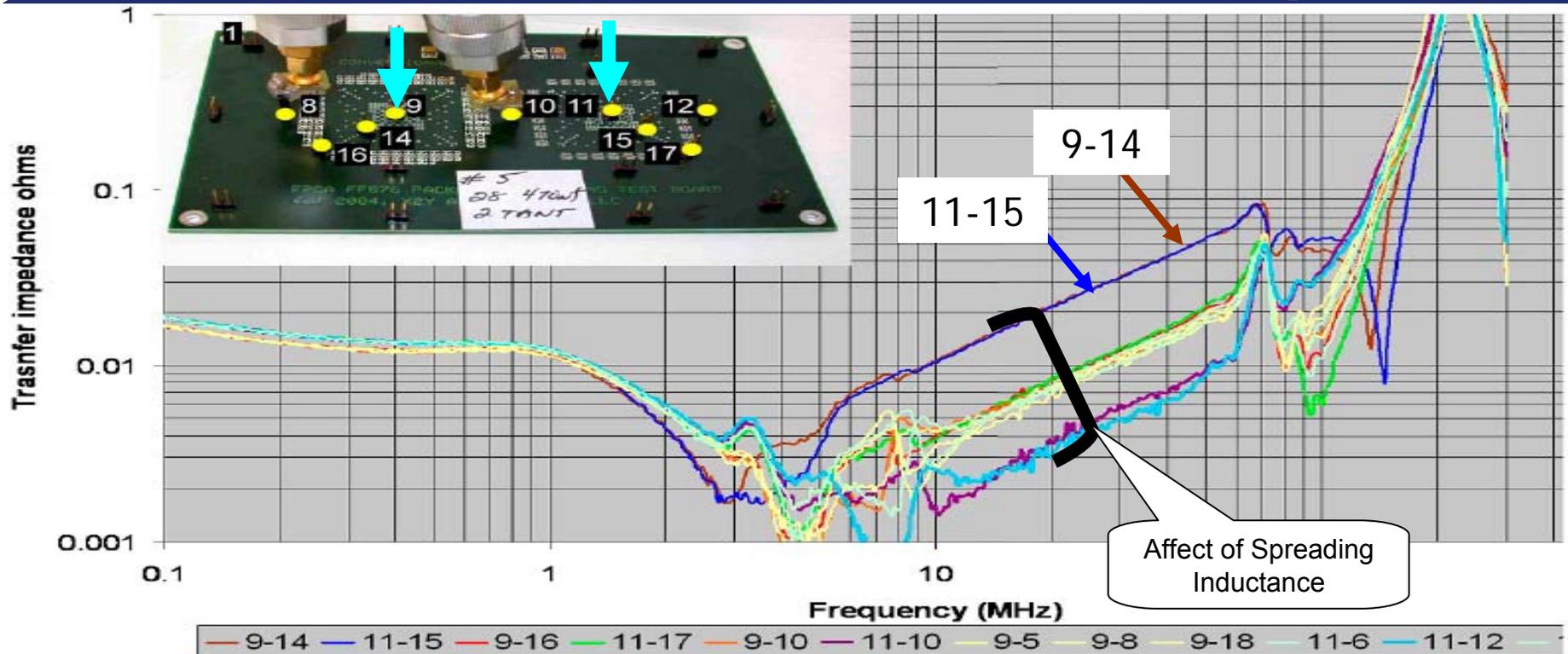
## Distance between IC and Cap:

- Larger current loop
- More inductance
- Less effective



Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "[High Performance FPGA Bypass Filter Networks](#)," DesignCon 2005, Santa Clara, CA, February 2005.

# PDS Placement & Mounting Parasitics



## Effects of spreading Inductance in PDS

- Using position 9 & 11 as I/O & core power position the effects of spreading inductance in the planes can be seen.
- Demonstrates why measuring across a cap for capacitor-in-system measurement isn't accurate.

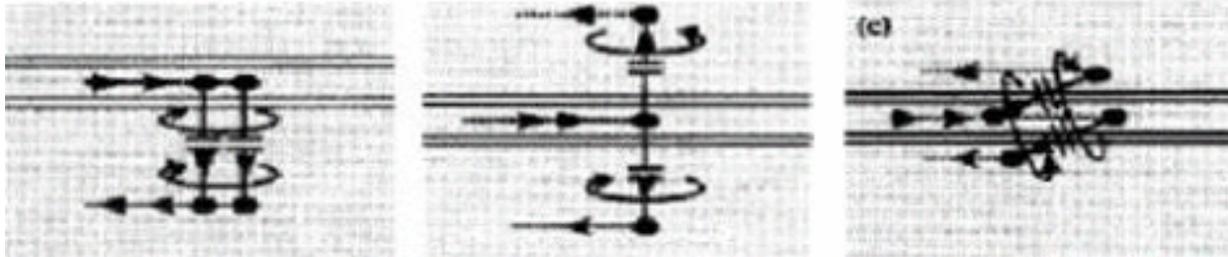
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# PDS Placement & Mounting Parasitics

This paper uses the concept of proper capacitor placement on a PC board to improve circuit performance.

## Decoupling Strategies for Printed Circuit Boards Without Power Planes

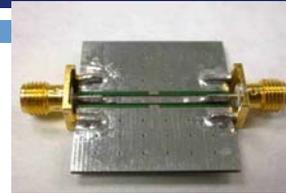
Hwan W. Shim, Theodore M. Zeef, Todd Hubing  
EMC Labrotory  
University Missouri-Rolla  
Rolla, MO



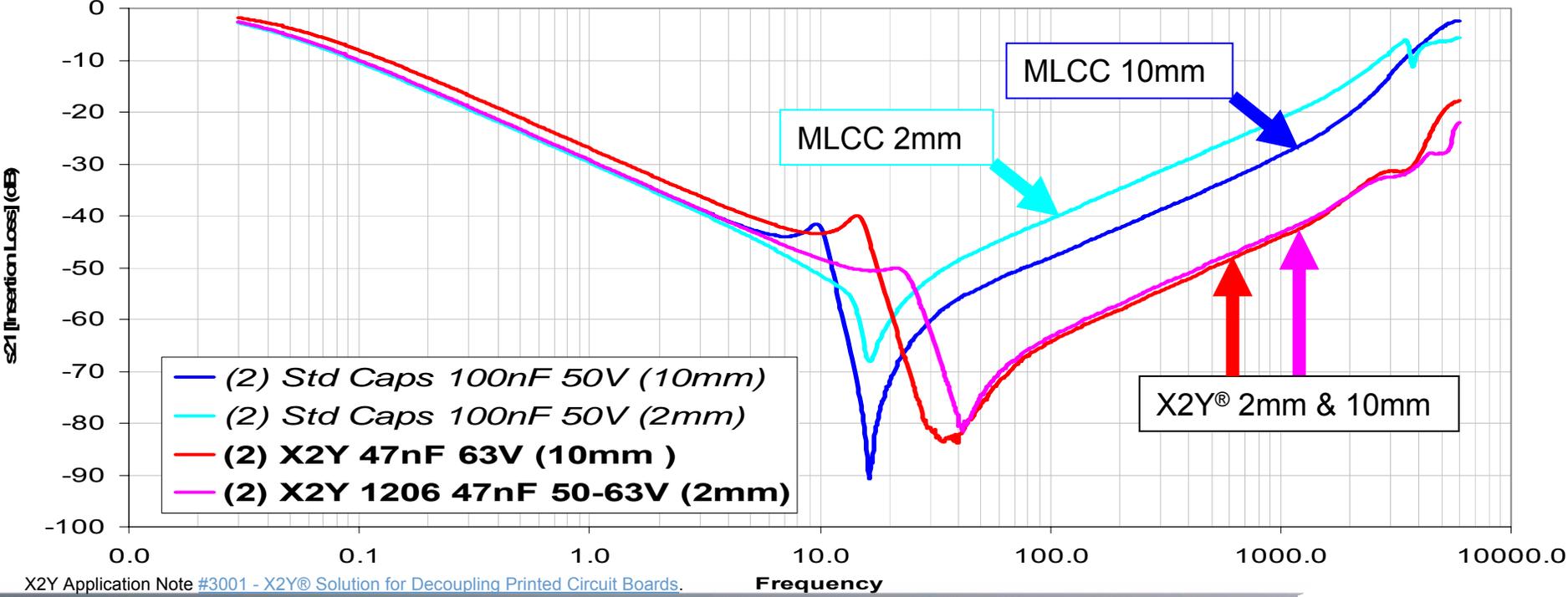
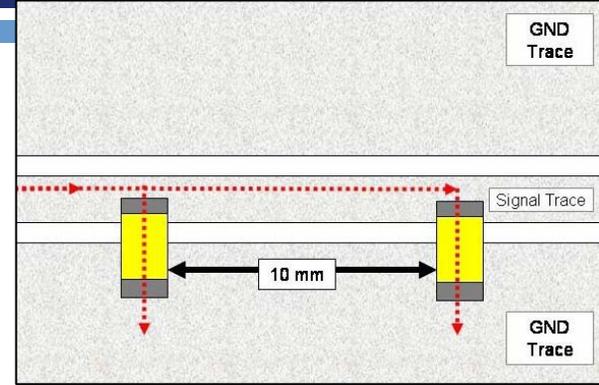
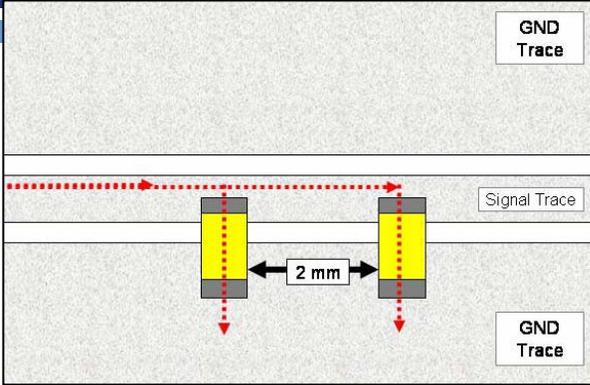
\* Presented at the August 2002 IEEE EMC Symposium, Minneapolis, MN - TU-PM-G-5, Volume 1, page258

Note: X2Y has expanded the testing with this PC board; further information can be found at this link:  
[#3001 - X2Y® Solution for Decoupling Printed Circuit Boards](#)

# PDS Placement & Mounting Parasitics



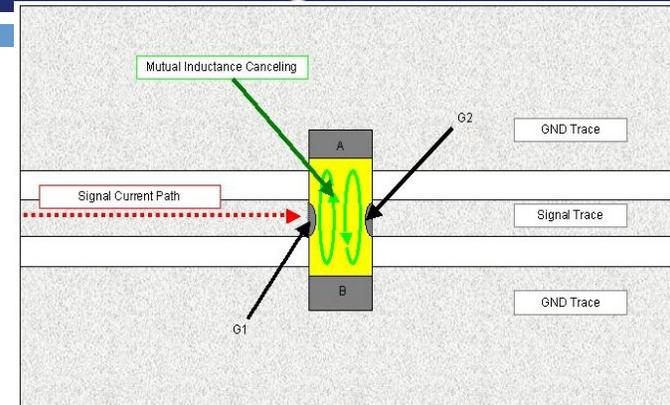
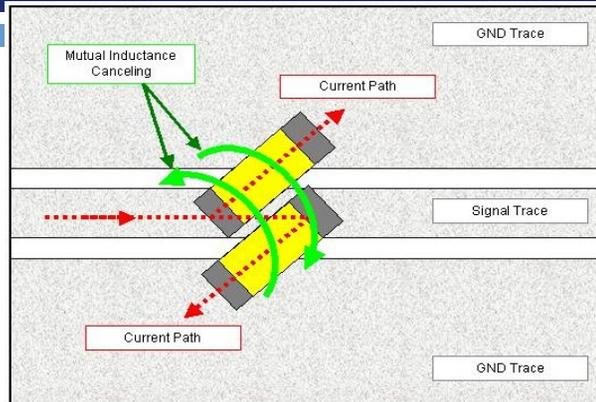
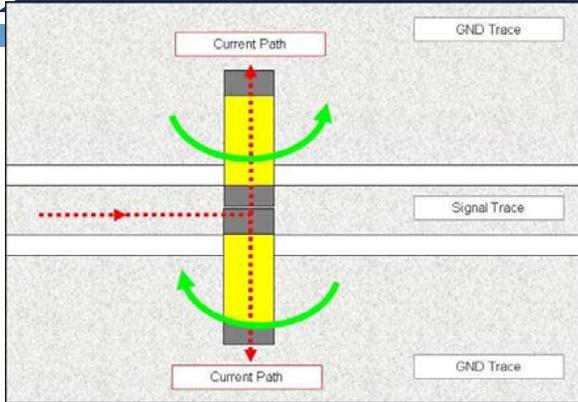
✓ Measurements made on 50ohm Coplanar PCB with Ground Plane.



X2Y Application Note #3001 - X2Y<sup>®</sup> Solution for Decoupling Printed Circuit Boards.



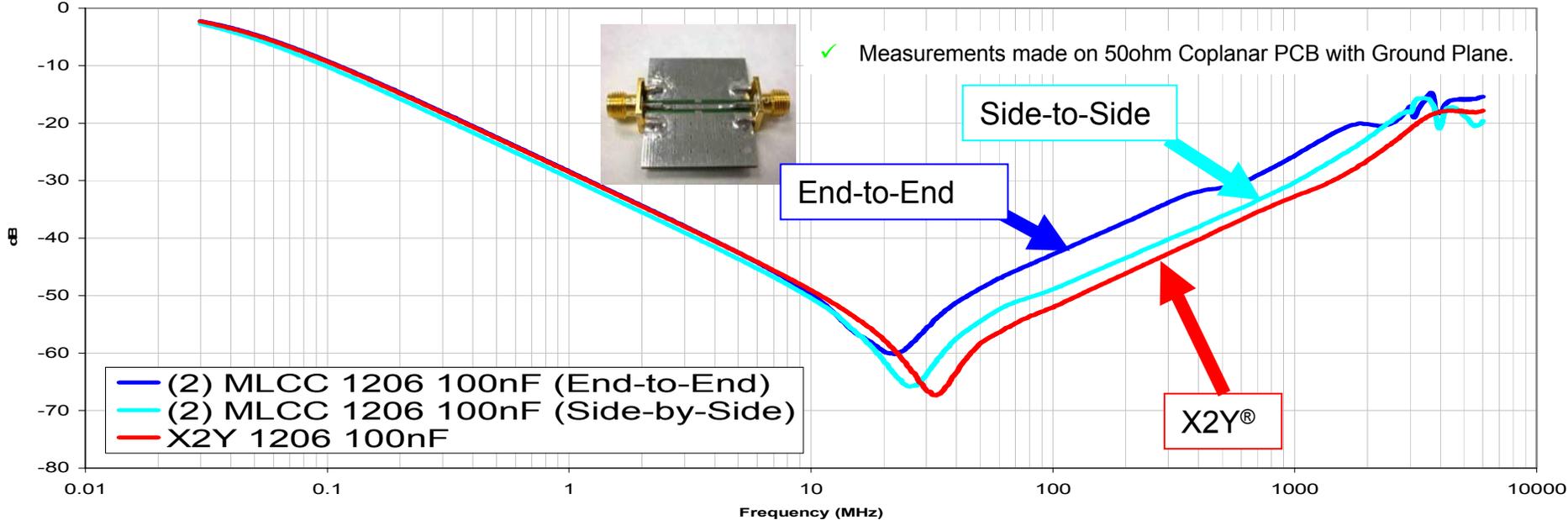
# PDS Placement & Mounting Parasitics



End-to-End

Side-to-Side

X2Y®

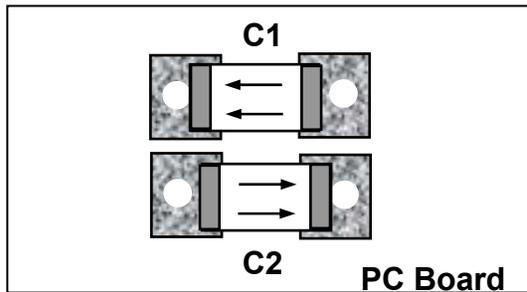


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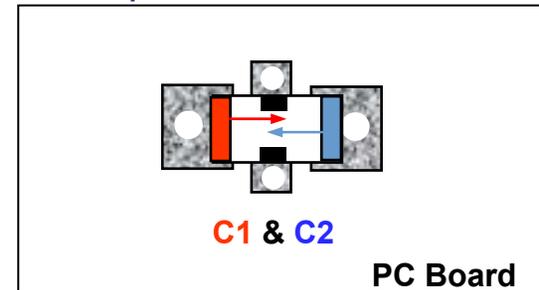
The X2Y<sup>®</sup> design maximizes mutual inductance to reduce parasitic inductance. Inside X2Y<sup>®</sup>, every other electrode layer within the single component body is in opposition to cancel the magnetic flux.

Top-view Standard Capacitor

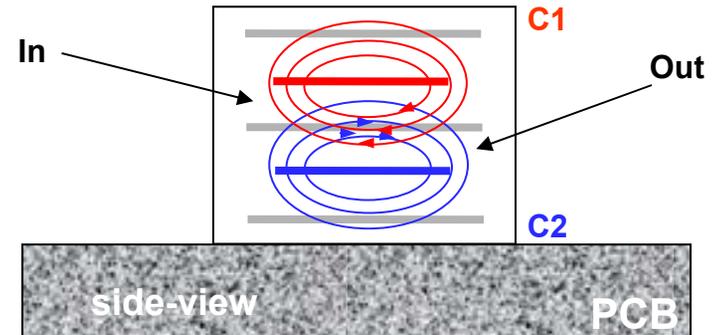
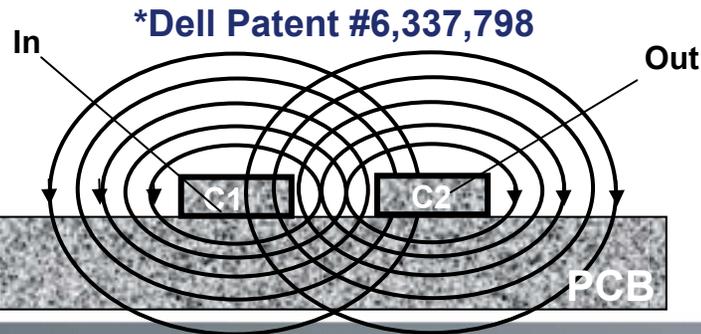


Flux lines cancel outside of component body boundaries

Top-view X2Y<sup>®</sup> Circuit



Flux lines cancel inside of component body boundaries

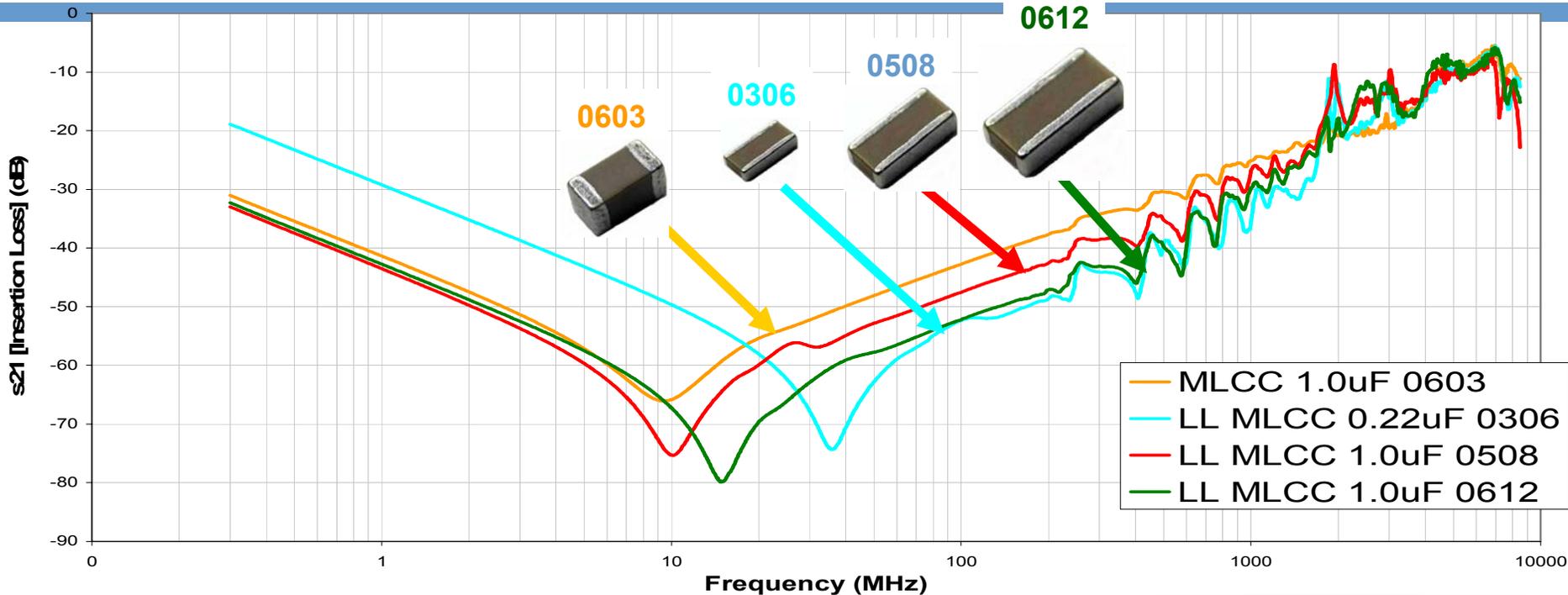


# PDS Placement & Mounting Parasitics

## Summary

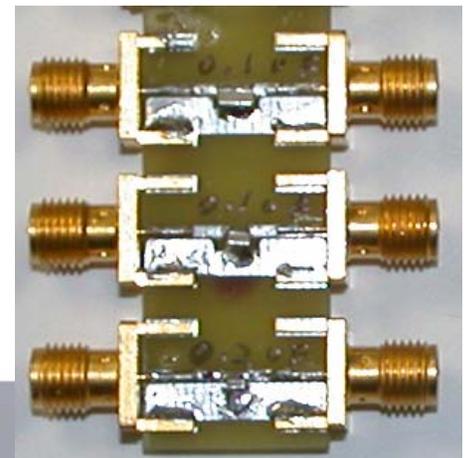
- Distance between caps and ICs should be minimized to reduce spreading inductance.
- Distance between caps can reduce performance if external coupling occurs.
  - Use technology that minimizes external coupling (X2Y<sup>®</sup> Technology).
  - Inter-digitate current flow through std. MLCC Technology.

# PDS Placement & Mounting Parasitics

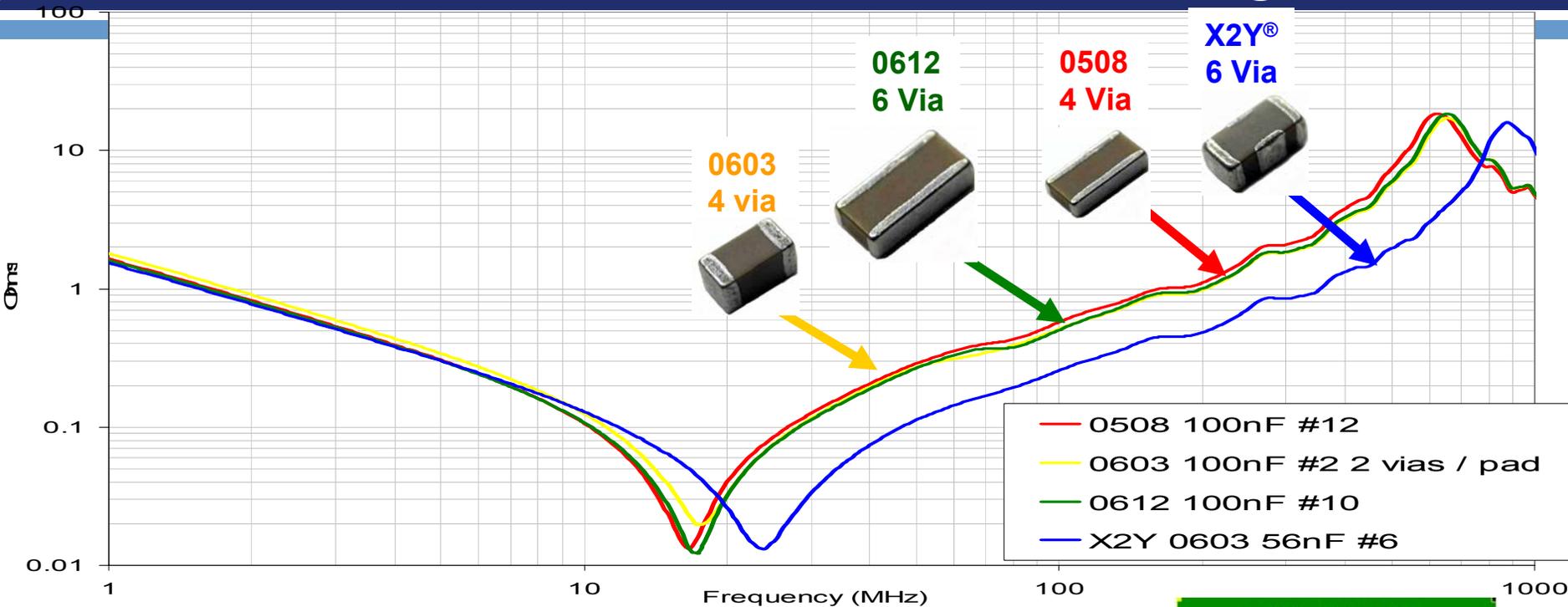


## Reverse-Aspect-Ratio (LL) Caps – Capacitor-only

- LL caps show lower inductive performance on microstrip PCB.

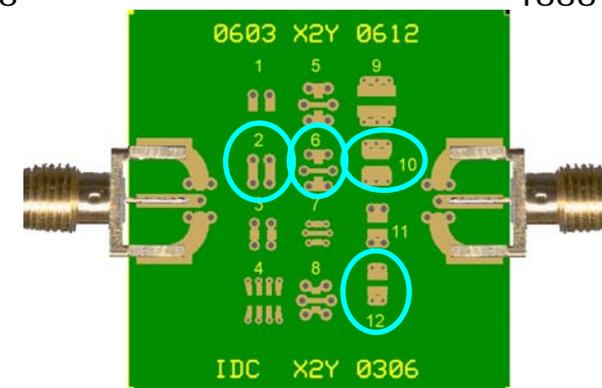


# PDS Placement & Mounting Parasitics

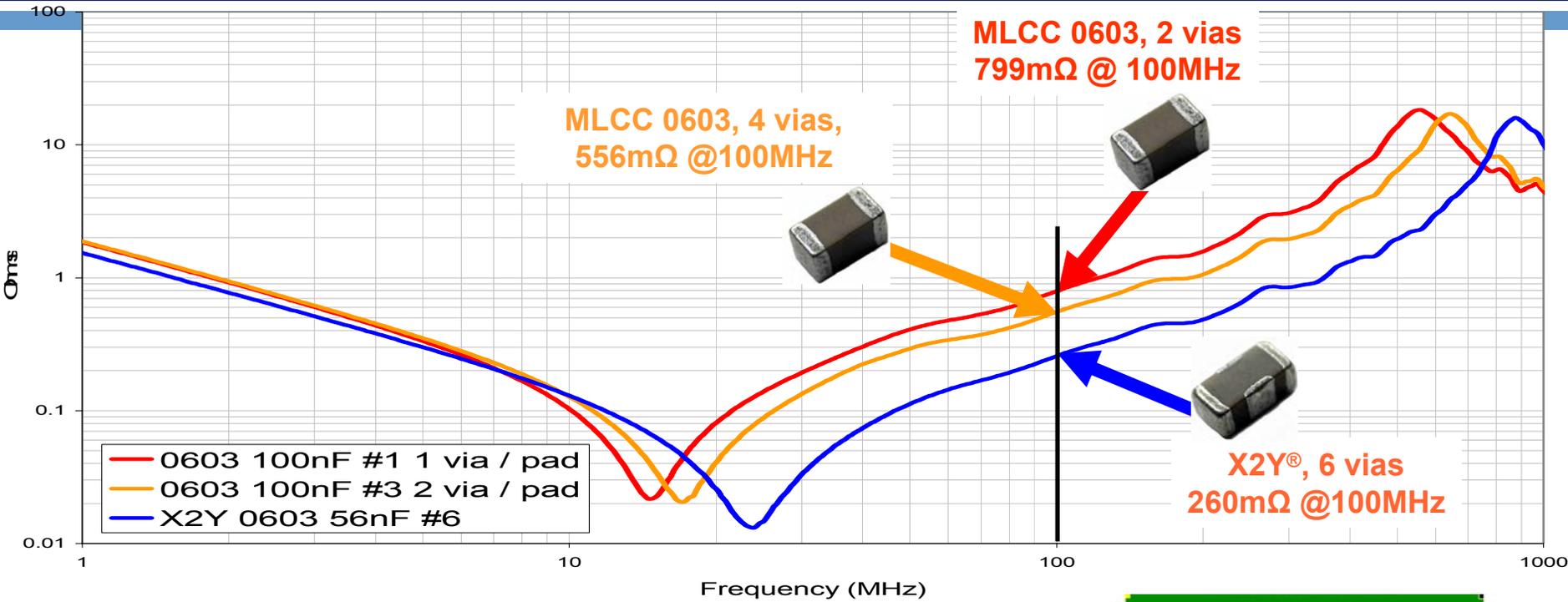


## Reverse-Aspect-Ratio (LL) Caps – Capacitor-in-system

- Mounted with vias, LL caps (6 vias) have the same performance as MLCC caps (4 vias).
- LL caps are limited by mounting parasitics.

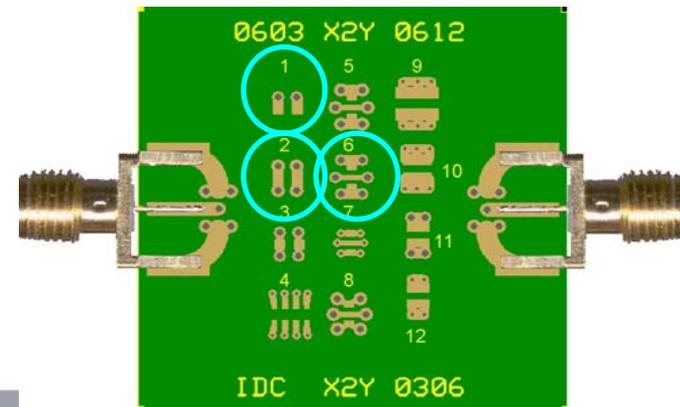


# PDS Placement & Mounting Parasitics



## Multi-Parallel Vias

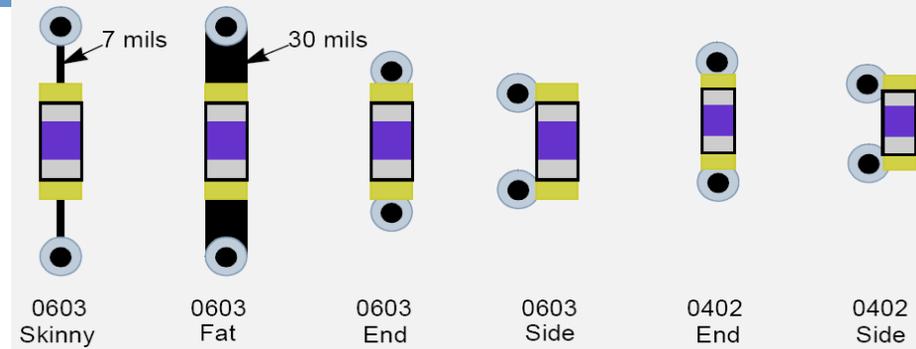
- MLCC – going from 2 to 4 vias improves impedance by 150 mΩ @ 100 MHz.



# PDS Placement & Mounting Parasitics

## Via & Pad Geometries

- Optimized placement and routing of the vias & pads to minimize inductance.
- Considerations should include:
  - Via
    - > Diameter
    - > Length
    - > Location
  - Trace/Pad
    - > Width
    - > Length



Hole Diameter 0.020 inches						
Via length: (inches)	0603 skinny	0603 fat	0603 end	0603 side	0402 end	0402 side
.004	1.51	0.89	0.42	0.33	0.38	0.21
.006	1.66	1.12	0.53	0.38	0.44	0.25
.010	2.13	1.47	0.68	0.51	0.58	0.32
.020	2.68	2.07	1.07	0.67	0.82	0.43
Hole Diameter 0.010 inches						
Via length: (inches)	0603 skinny	0603 fat	0603 end	0603 side	0402 end	0402 side
.004	1.51	0.95	0.50	0.36	0.42	0.26
.006	1.77	1.17	0.59	0.46	0.50	0.32
.010	2.18	1.52	0.77	0.61	0.67	0.40
.020	2.87	2.23	1.16	0.85	1.01	0.60

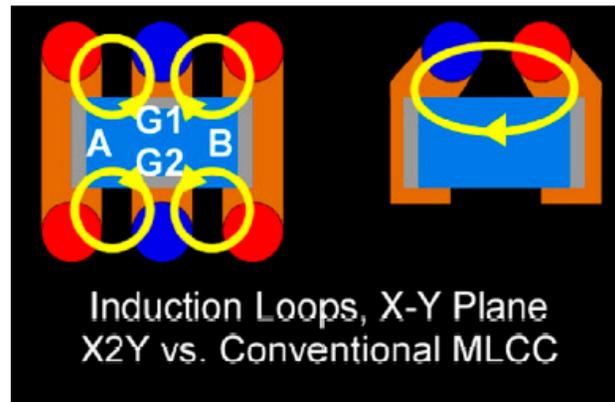
Howard Johnson, PhD, "[Parasitic Inductance of a Bypass Capacitor II](#)," HIGH-SPEED DIGITAL DESIGN – online newsletter Vol. 6 Issue 9, Signal Consulting, Inc.

Milliom, Gary, "[Power Supply Design for PowerPCTM Processors](#)," Freescale Semiconductor Application Note AN2447, Rev. 1.1, Sept 2004.

# PDS Placement & Mounting Parasitics

## Inter-digitated vias

- Mutual inductance between vias cancel.
- Lowers over-all net inductance of vias, thus mounting inductance of caps.
- Inter-digitated caps are ideal to use minimize pad/trace distance to vias.

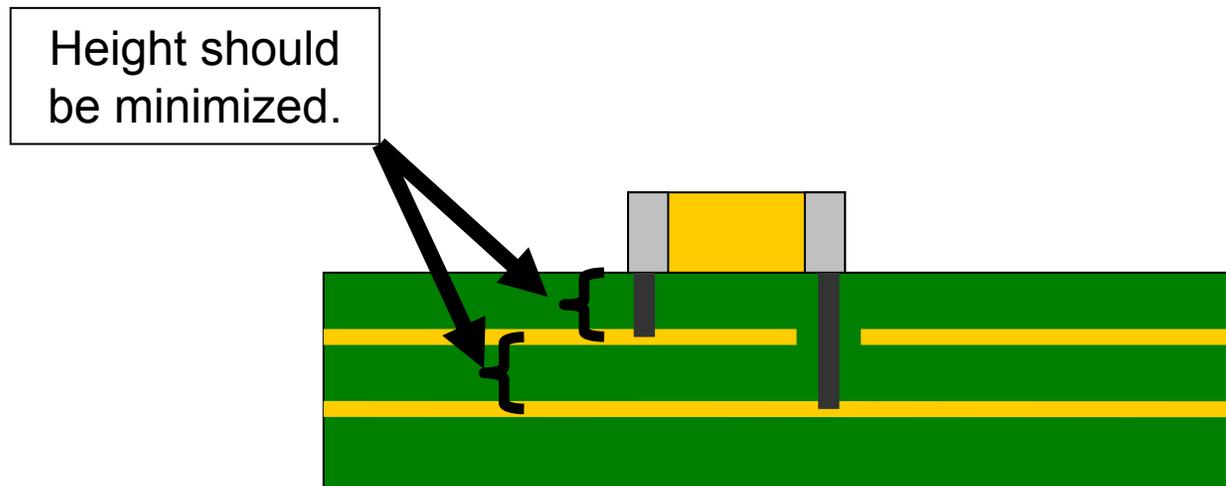


Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "[High Performance FPGA Bypass Filter Networks](#)," DesignCon 2005, Santa Clara, CA, February 2005.

# PDS Placement & Mounting Parasitics

## Minimize distance between PCB planes and capacitor (Via Length).

- Extra via length between capacitor pad and PCB planes adds inductance.



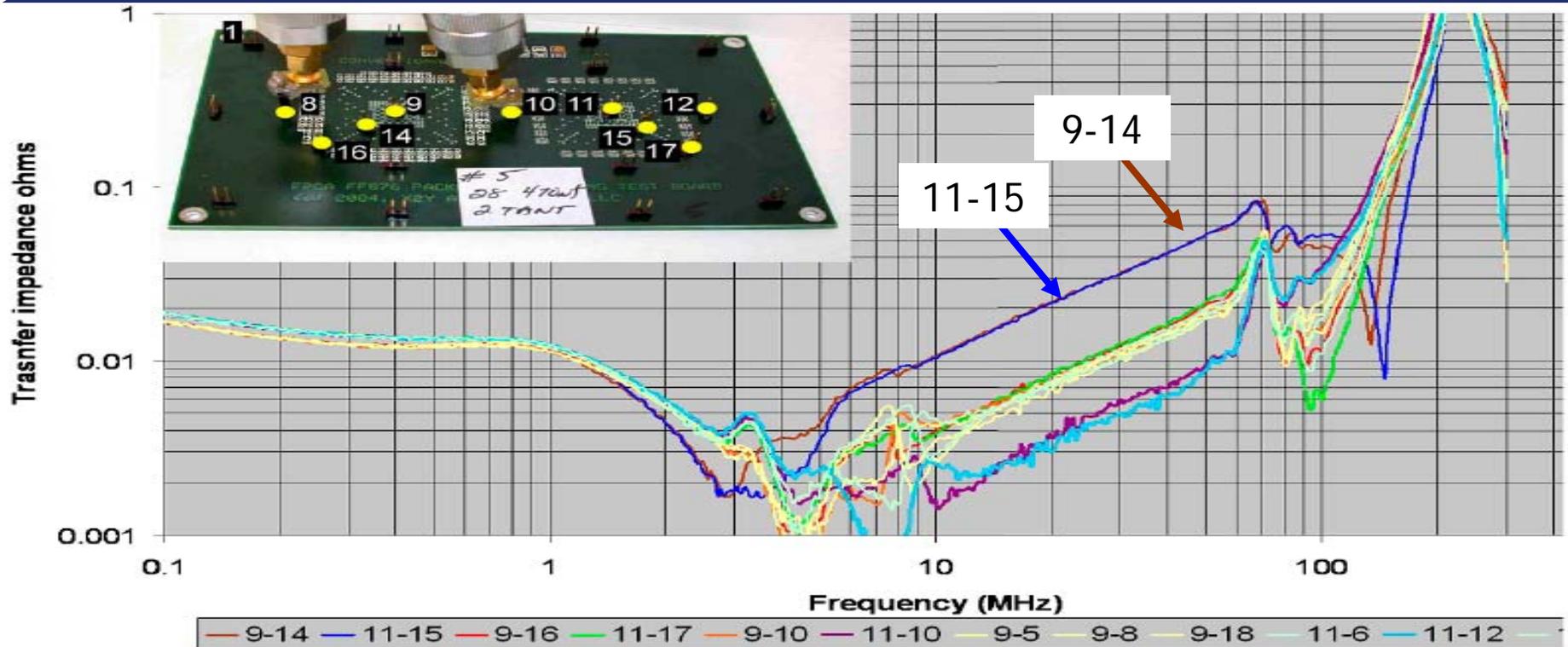
Larry Smith, Raymond Anderson, Doug Forehand, Tom Pelc, and Tanmoy Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," IEEE Transaction on Advanced Packaging, August 1999, pages 284-291.

## Summary

- Lower Via/mounting Inductance
  - Multiple parallel vias
  - Inter-digitate vias – lower over-all net via inductance.
  - Use Inter-digitated caps – to minimize pad/trace distance from cap to via.
  - Minimize distance between planes and caps.

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3. Evaluating Decoupling (Capacitors-Only)
4. PDS Placement & Mounting Parasitics
- 5. PDS with Low-Inductance Capacitors**
6. Cost/Build-of-Materials (BOM)
7. X2Y<sup>®</sup> Components (Overview)
8. IC Conducted/Radiated Emissions (Filtering)
9. Conclusion/Questions

# PDS with Low-Inductive Capacitors



## MLCC vs. X2Y® on a Passive Xilinx FPGA PCB.

- (104) 0402 MLCC vs. (20) 0603 X2Y®
- (208) vias – MLCC vs. (120) vias – X2Y®
- Saves PCB real-estate!

Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "[High Performance FPGA Bypass Filter Networks](#)," DesignCon 2005, Santa Clara, CA, February 2005.

# PDS with Low-Inductive Capacitors

Table 1, Mounted Inductance, Comparative Conventional and X2Y<sup>3</sup>

	Capacitors on Component Side							Capacitors on Back side <sup>4</sup>		
H1	0.005	0.020	0.005	0.020	0.005	0.012	0.012	0.005	0.005	0.005
H2	0.014	0.003	0.003	0.001	0.001	0.038	0.038	0.014	0.003	0.001
S	0.03	0.03	0.03	0.03	0.03	0.032	0.044	0.03	0.03	0.03
D	0.01	0.01	0.01	0.01	0.01	0.02	0.02	0.01	0.01	0.01
K1 D/S	0.33	0.33	0.33	0.33	0.33	0.63	0.45	0.33	0.33	0.33
L / via pH	318	393	76	217	40	590	629	1580	1530	1540
L 0603	1052	1290	662	935	579	1500 <sup>b</sup>	1760	3670	3560	3590
L 0402	952	1190	552	835	479	1400	1660	3570	3460	3490
L X2Y	267	355	117	223	90	435	531 <sup>b</sup>	1250	1210	1220
Caps req'd 0603	3.9	3.6	5.6	4.2	6.5	3.4	3.3	2.9	2.9	2.9
Caps req'd 0402	3.6	3.3	4.7	3.7	5.3	3.2	3.1	2.9	2.9	2.9
Caps req'd X2Y	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

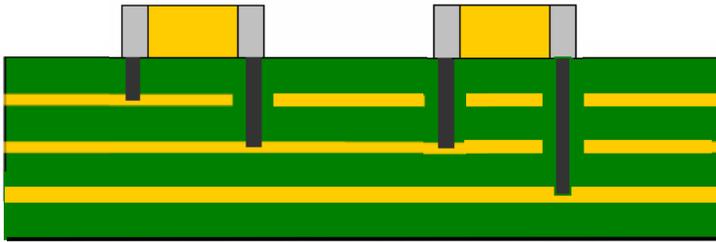
Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

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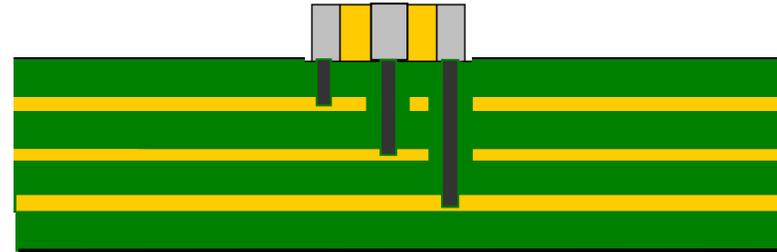
# Cost/Build-of-Materials (BOM)

## Component Cost vs. System Cost

Cost/Build-of-Materials (BOM)	
<b>Number of cap</b>	X2Y <sup>®</sup> is a 1:3 to 1:7 replacement over standard MLCC Technology. (Ratio depends on PCB thickness and plane height.)
<b>Number of vias</b>	MLCC Technology typically used (2) vias per capacitor, where as X2Y <sup>®</sup> uses (6) vias. For a 1:3 ratio X2Y <sup>®</sup> uses the same number of via, for a 1:7 ratio X2Y <sup>®</sup> uses 6 vias and MLCC would use 14 which would be a 42.8% savings.
<b>Placement Cost</b>	Placement cost depends on process, materials and volume used during manufacturing and is largest and hardest value to quantify.
<b>PCB real-estate</b>	X2Y <sup>®</sup> saves space.
<b>Number of layers for routing</b>	Fewer vias for capacitor allows for more room for routing.
<b>Assembly time</b>	Fewer capacitors reduces assembly time.
<b>Number solder joints</b>	Fewer solder joints reduces assembly time.
<b>Number via drills</b>	Fewer via drills reduces assembly time and cost.
<b>Number pick-and-place machines</b>	Fewer capacitors reduces the number of pick-and-place machines needed in production (capital cost).
<b>Reliability</b>	Reliability affects warranty cost, manufacturing cost, and customer satisfaction.
<b>Number of attachments</b>	Reducing the number of attachments on PCB improves reliability.
<b>solder joints</b>	Reducing the number of solder joints on PCB improves reliability.
<b>Number of vias</b>	Reducing the number of vias on PCB improves reliability.
<b>Number of components</b>	Reducing the number of components on PCB improves reliability.



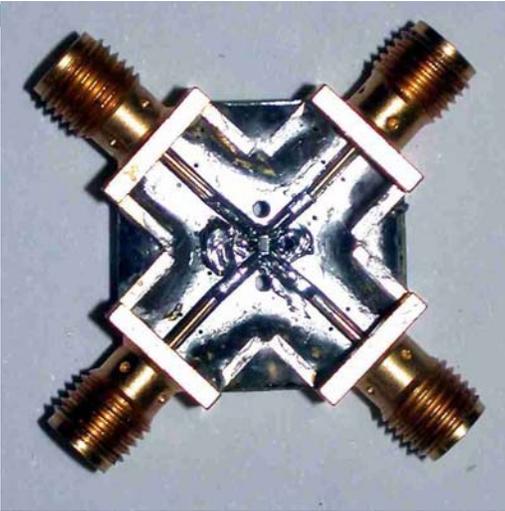
VS.



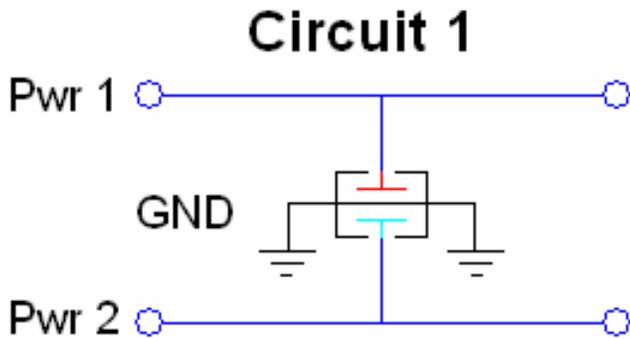
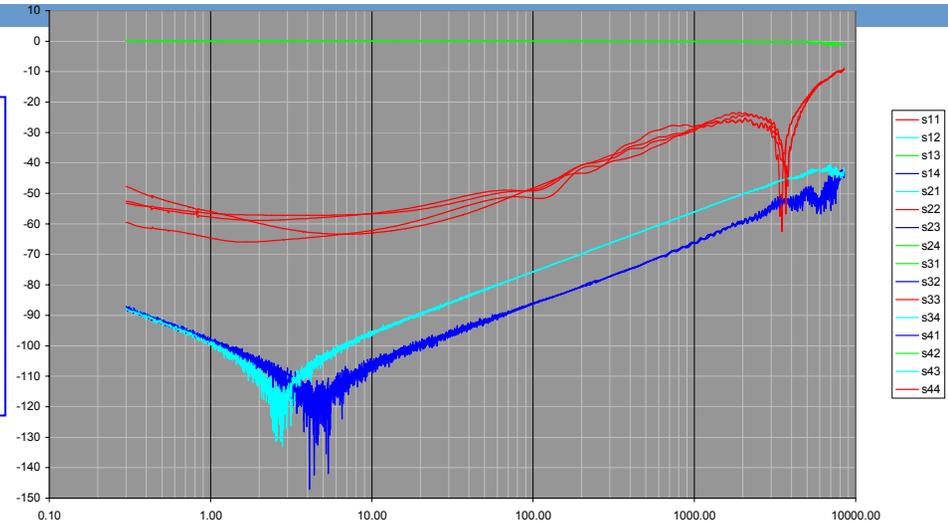
## Multi-plane Decoupling

- Decoupling multiple power planes on PCB increases the number of standard caps needed.
- A single X2Y<sup>®</sup> can be used for 2 different power planes.

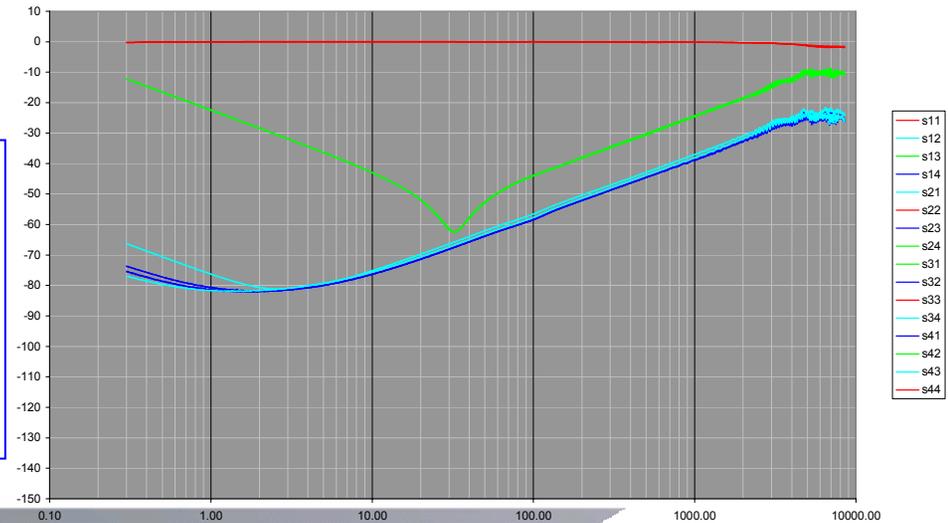
# Cost/Build-of-Materials (BOM)



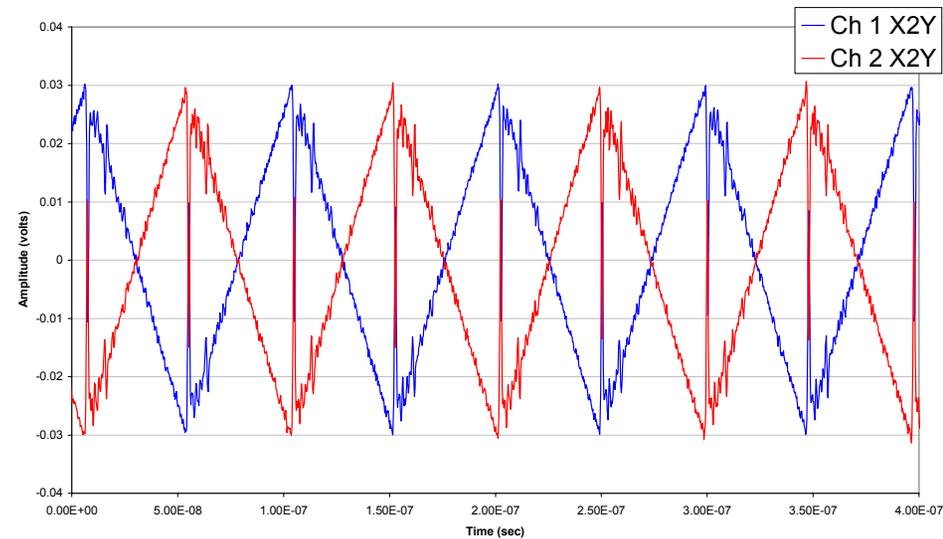
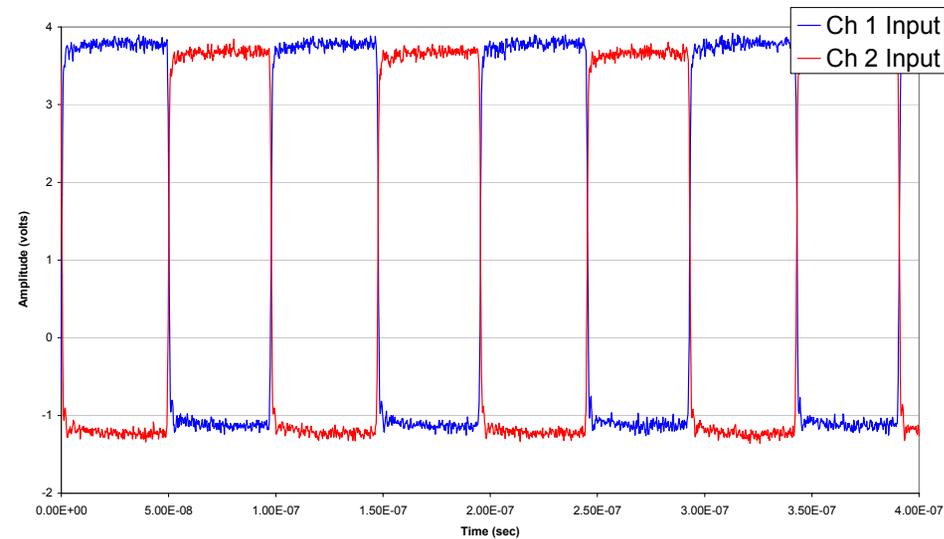
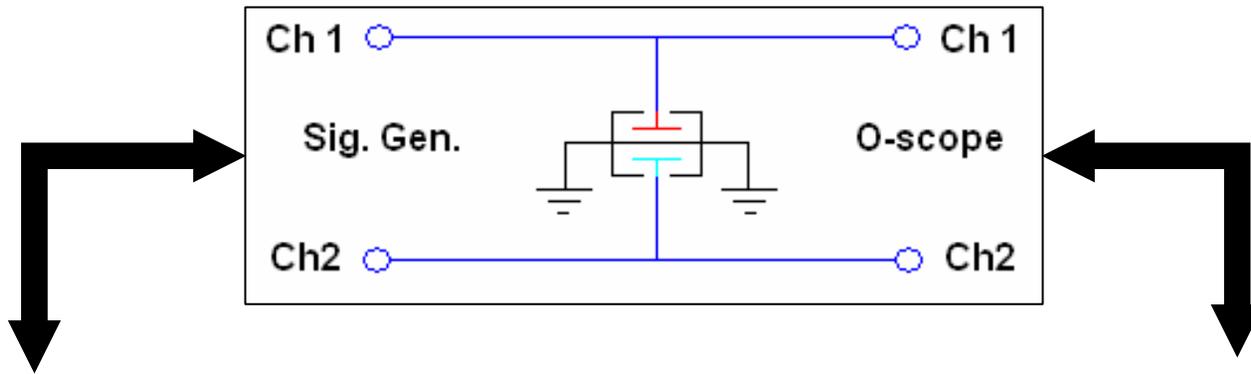
PCB Fixture



X2Y 0603 100nF



# Cost/Build-of-Materials (BOM)

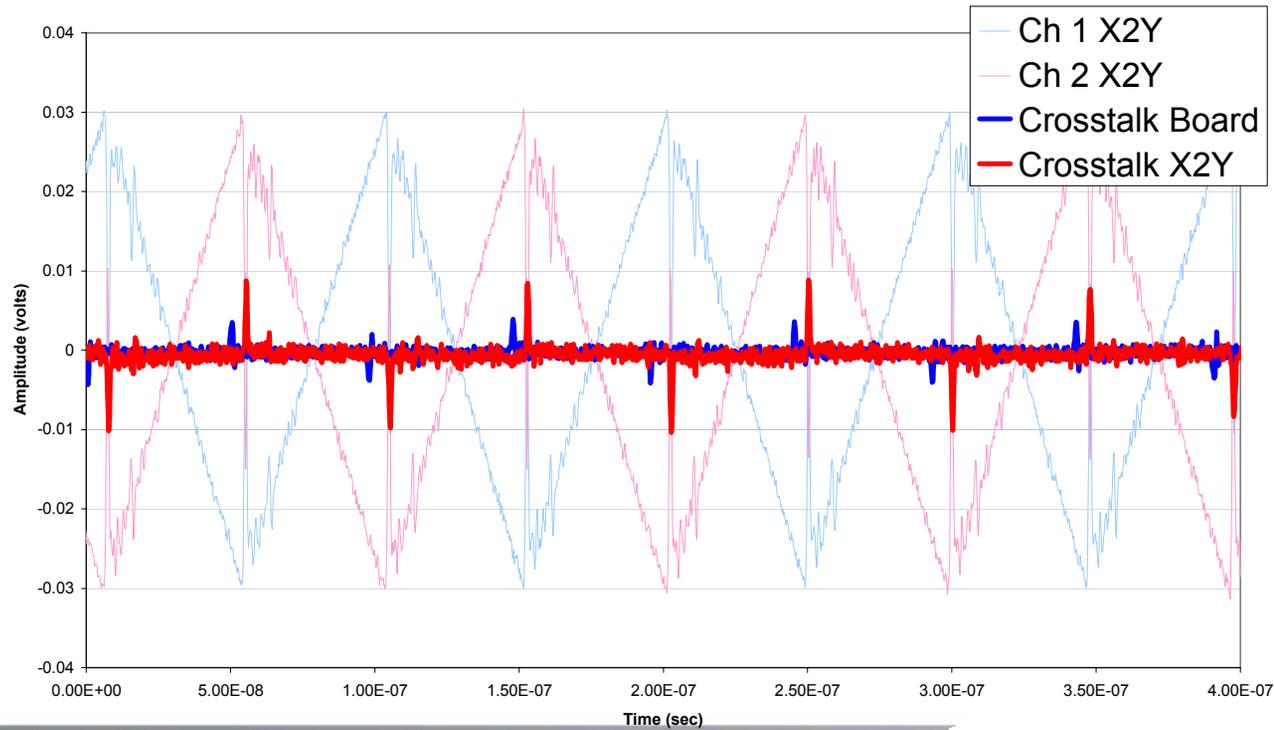
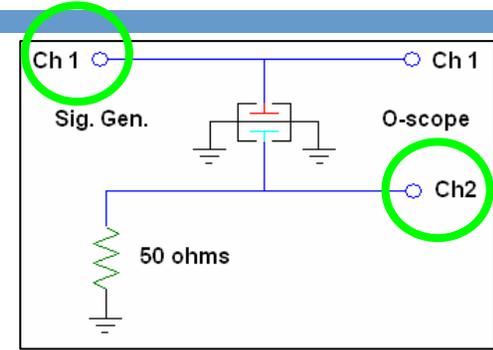
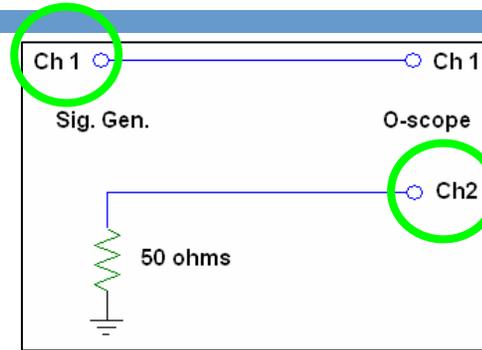


Note: Scale differences.

# Cost/Build-of-Materials (BOM)

## X2Y<sup>®</sup> crosstalk

- Circuit 1



## Summary

- All power planes require decoupling caps.
- Component cost-only – low-inductive caps cost more.
- System cost – low-inductive caps (IPDs) offer substantial cost savings.
- Roadmap for NEMI published in 2003 predicted cost savings for IPDs starting in 2005.
- Conventional capacitor technology can only decouple one plane.
- Using X2Y<sup>®</sup>'s differential property can simultaneously decouple 2 power planes, significantly reducing the number of caps typically required.

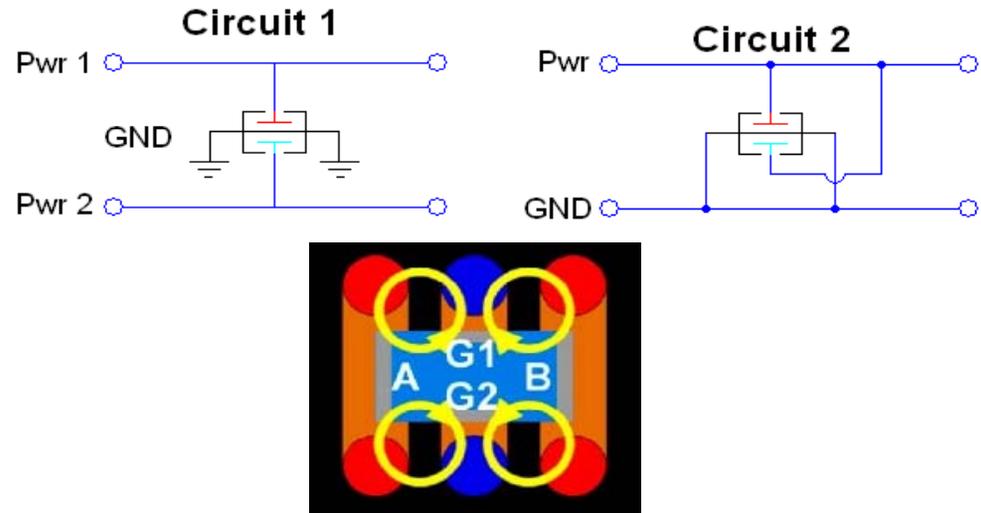
Joseph Dougherty, John Galvagni, Larry Marcanti, Rob Sheffield, Peter Sandborn, and Richard Ulrich, "The NEMI Roadmap: Integrated Passives Technology and Economics," CARTS 2003, Scottsdale, AZ, April 2003.

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# X2Y<sup>®</sup> Components (Overview)

## X2Y<sup>®</sup> Technology – Circuit 1 & Circuit 2

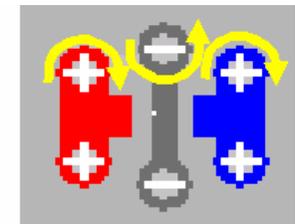
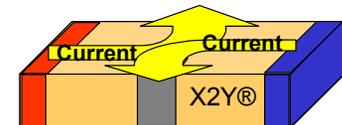
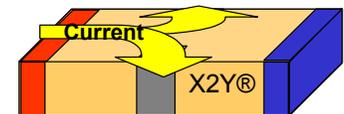
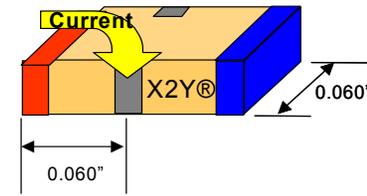
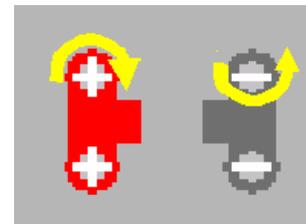
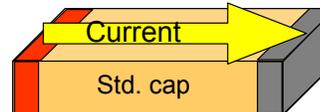
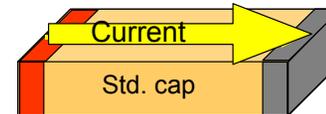
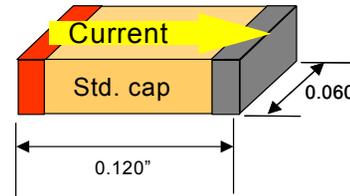
- Capacitive Circuit
  - Circuit 1 – 3 conductor
  - Circuit 2 – 2 conductor
- 4 terminal device
- Layout attachment is inter-digitated
- Note: X2Y<sup>®</sup> in this presentation has been Circuit 2 unless noted (multi-plane decoupling)



# X2Y® Components (Overview)

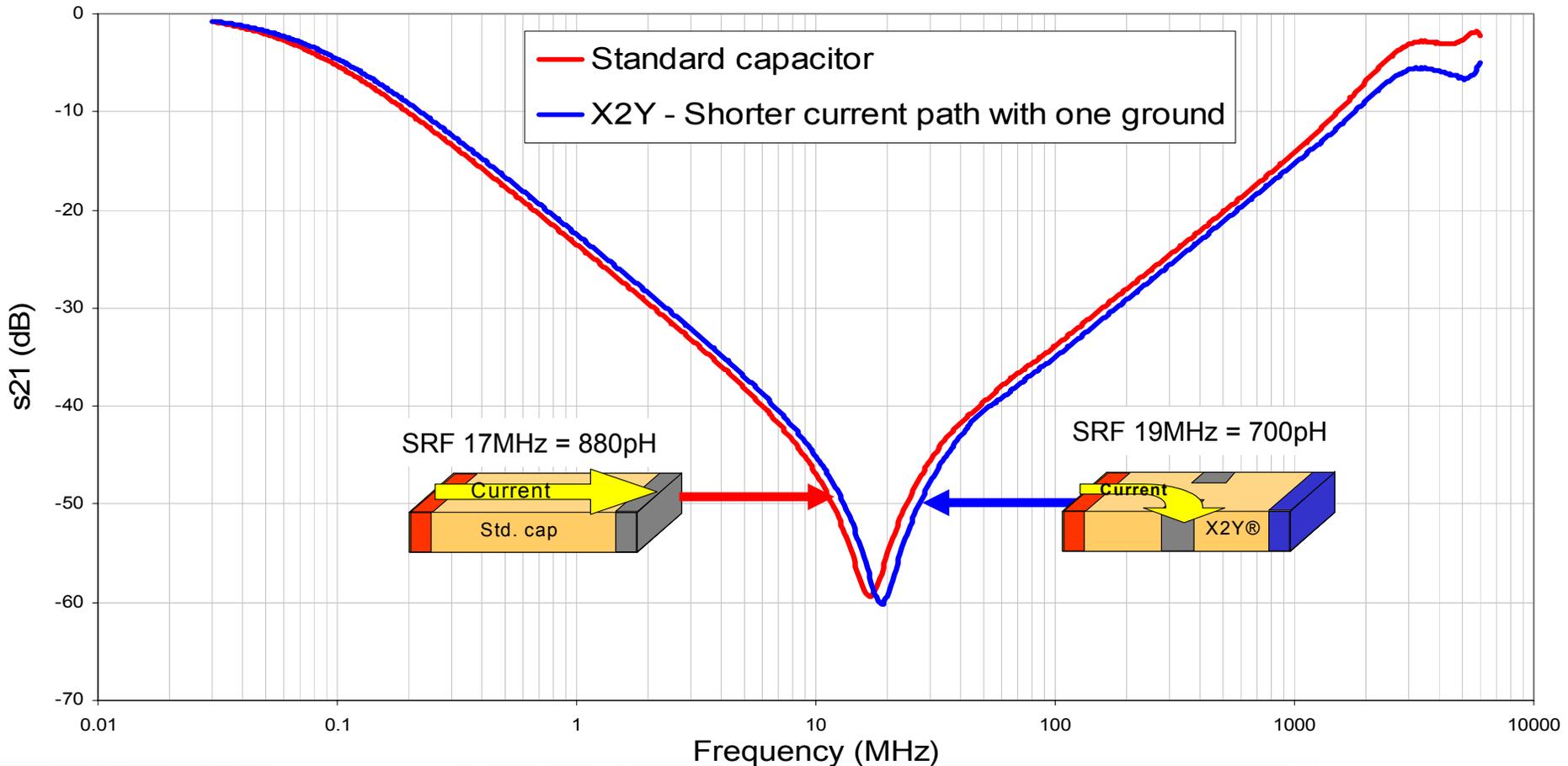
## X2Y® structural features for low-inductance.

- **Shorter** current path to ground, therefore smaller current loops.
- **Dual** current path to ground.
- **Opposing current flow** internal to the device = *cancellation of mutual inductance*.
- The X2Y footprint results in lower mounted inductance.



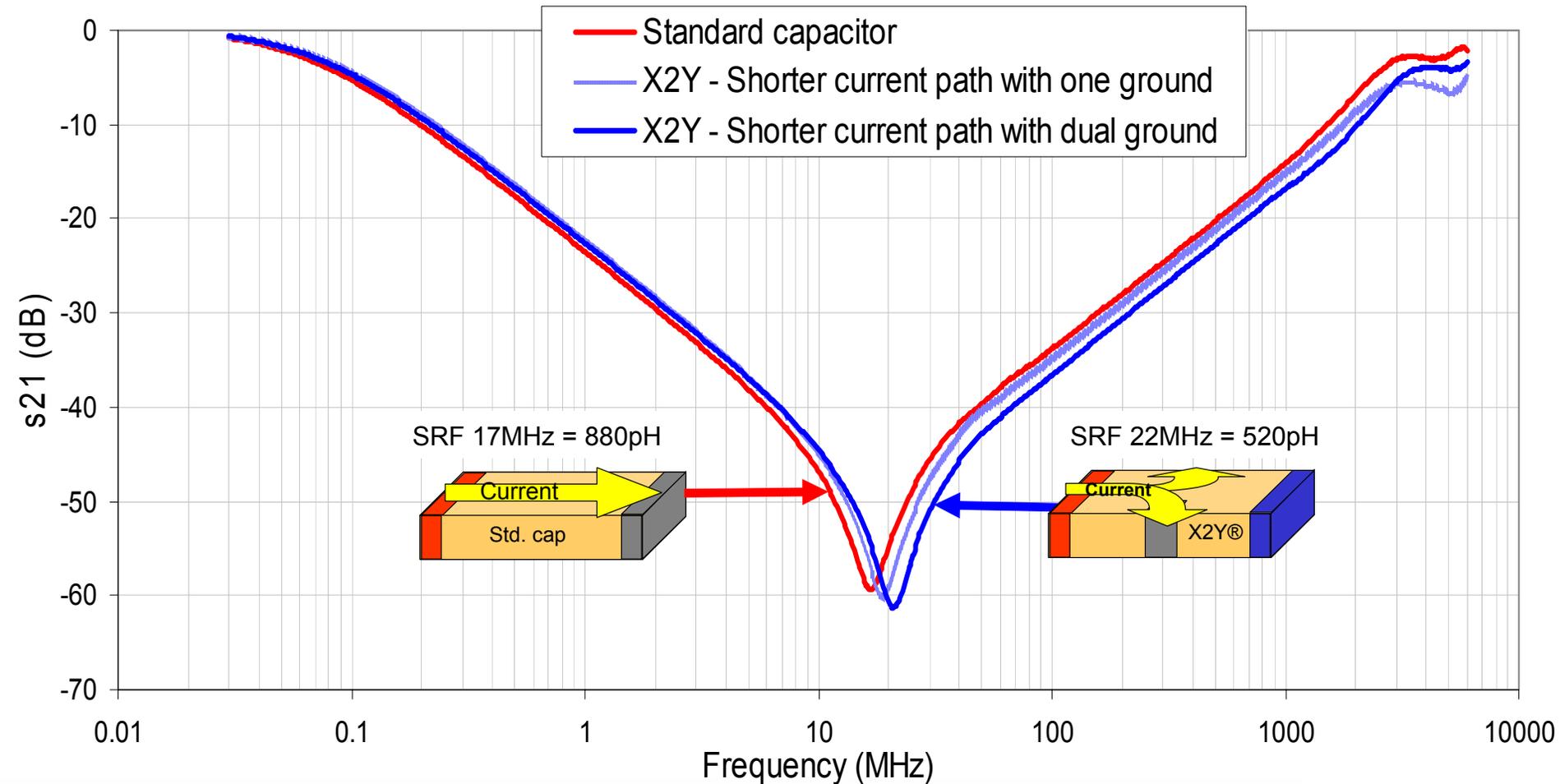
# X2Y<sup>®</sup> Components (Overview)

**X2Y<sup>®</sup> Structural Benefit – shorter path to ground, which creates a smaller current loop when attached to the PCB.**



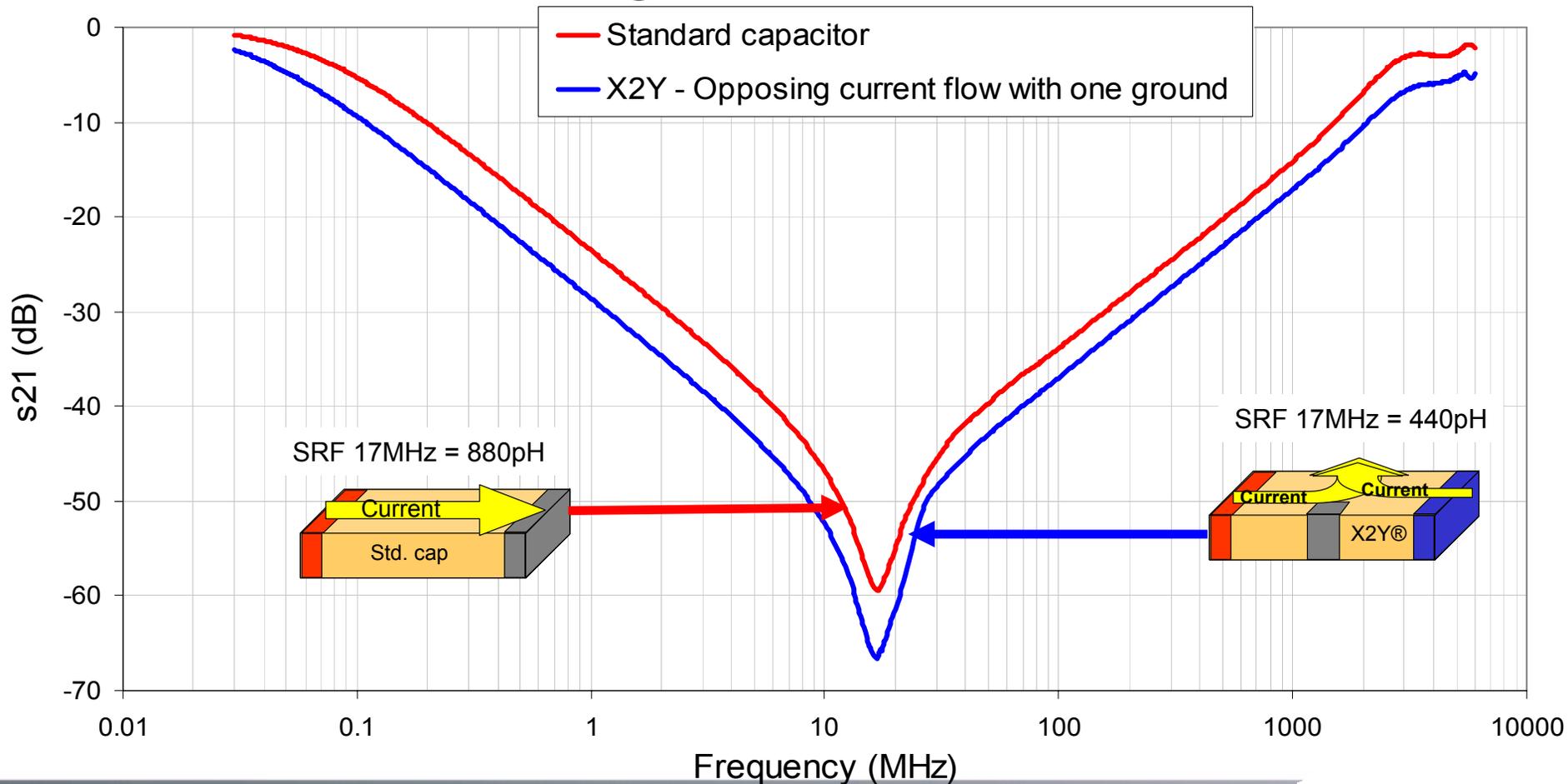
# X2Y<sup>®</sup> Components (Overview)

## X2Y<sup>®</sup> Structural Benefit – dual ground connection to the PCB.



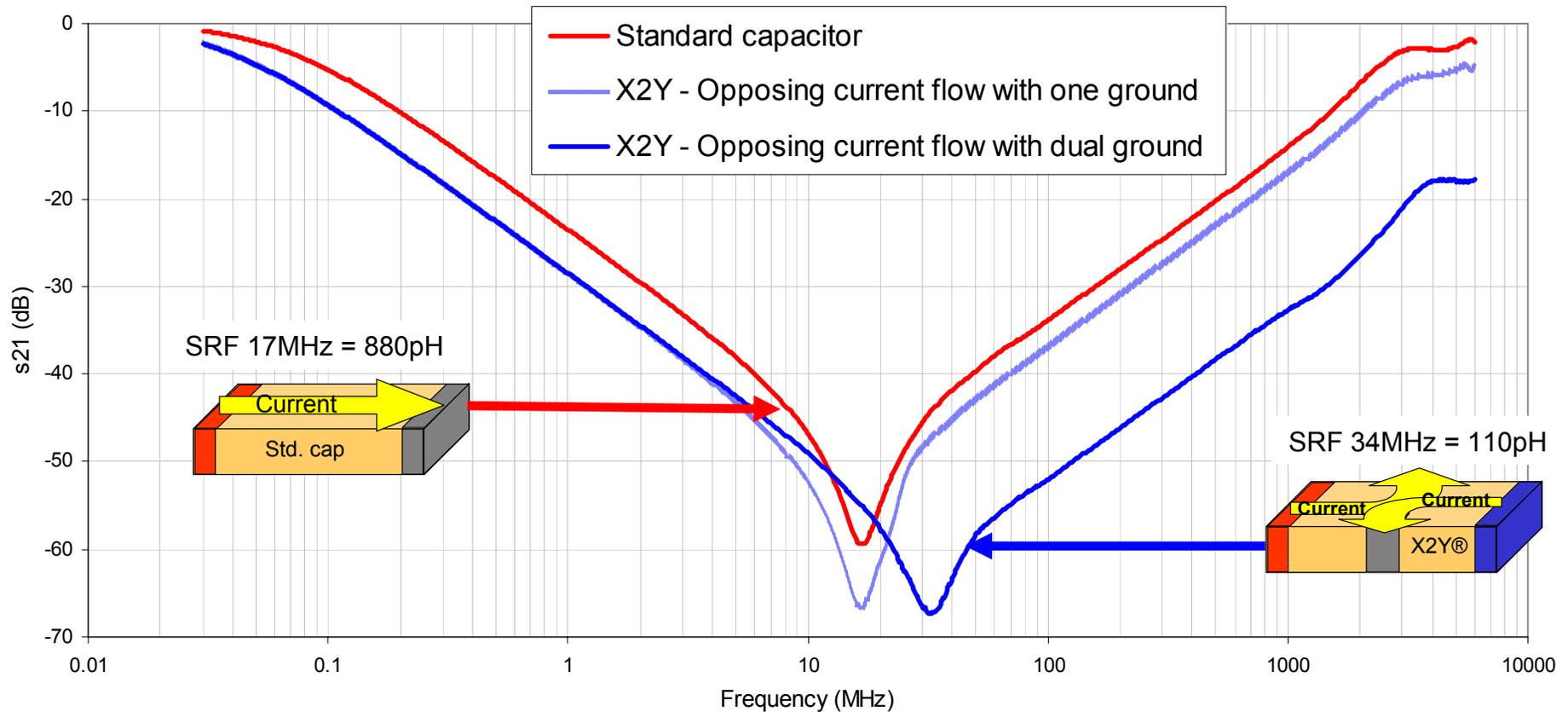
# X2Y<sup>®</sup> Components (Overview)

**X2Y<sup>®</sup> Structural Benefit – opposing current flow to a single ground connection and resulting benefit of flux cancellation.**



# X2Y<sup>®</sup> Components (Overview)

**X2Y<sup>®</sup> Structural Benefit – opposing current flow to a dual ground connection and resulting benefit of flux cancellation.**



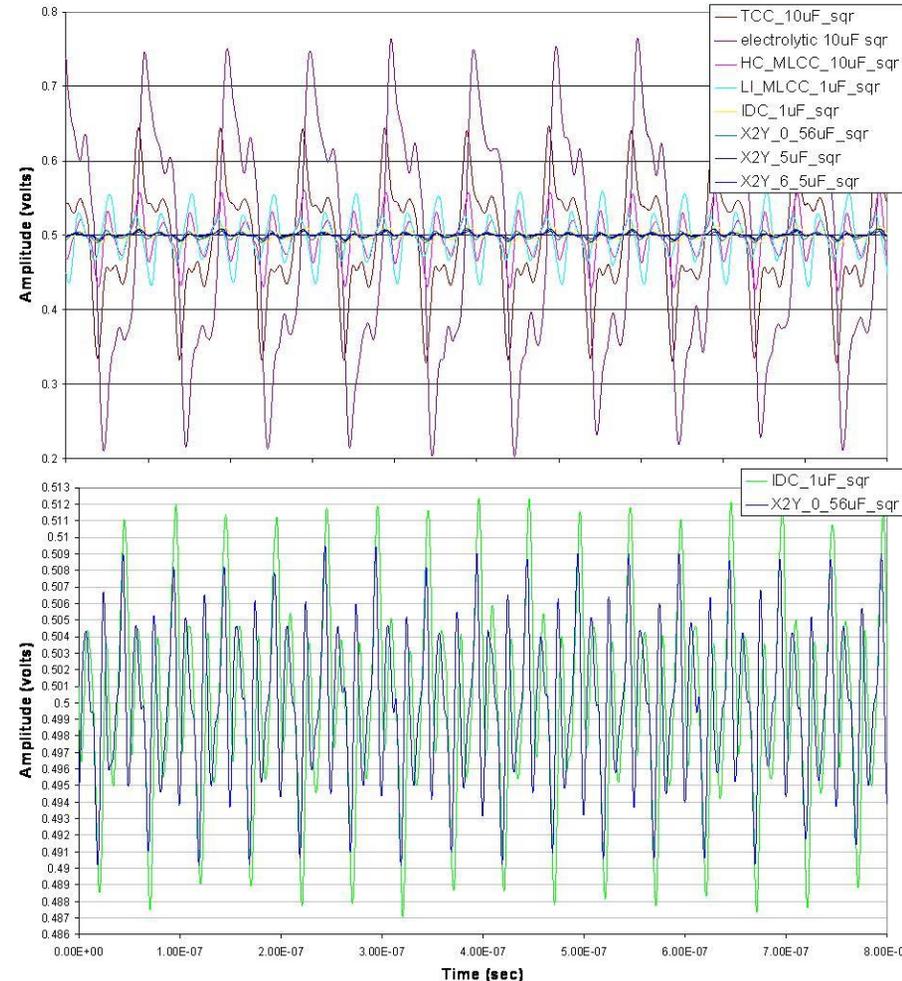
# X2Y® Components (Overview)

## Time-Domain Testing (Clock Cycle)

- 50/50 Duty Cycle
- 70 ps rise/fall time
- 1 GHz Frequency
- 20 GS/s sampling rate

Data courtesy of Kevin Slattery, Intel Corporation.

Component	Square Wave $\Delta$ Peak-to-Peak
Electrolytic 10uF	571 mV
Tantalum 10uF	319 mV
Std. MLCC 10uF	134 mV
LL MLCC 1.0uF	128 mV
<b>IDC™ 1.0uF</b>	<b>25.3 mV</b>
<b>X2Y® 0.56uF (1.12uF total)</b>	<b>19.6 mV</b>
X2Y® 5.0uF (10uF total)	16.7 mV
X2Y® 6.5uF (13uF total)	13.2 mV



Sanders, Muccioli, North, and Slattery, "The Quantitative Measurement of the Effectiveness of Decoupling Capacitors in Controlling Switching Transients from Microprocessors," CARTS 2005 USA, Palm Springs, CA, March 2005.

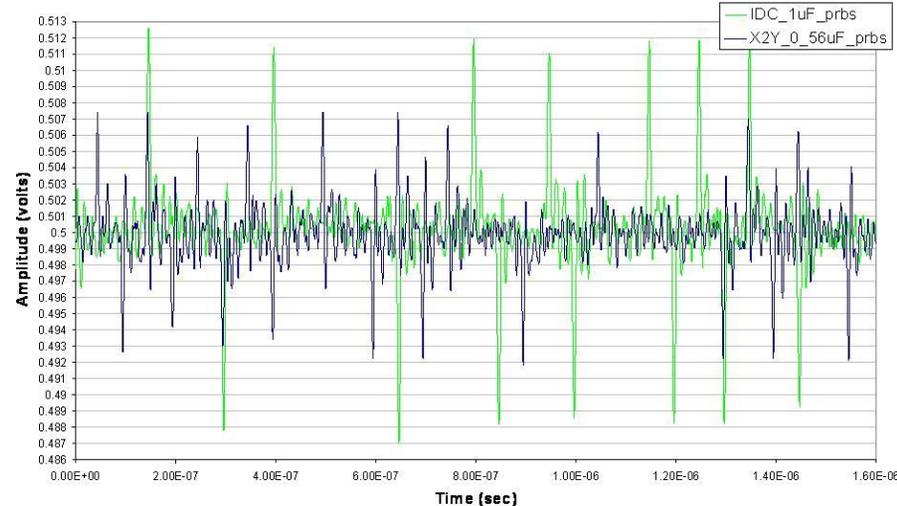
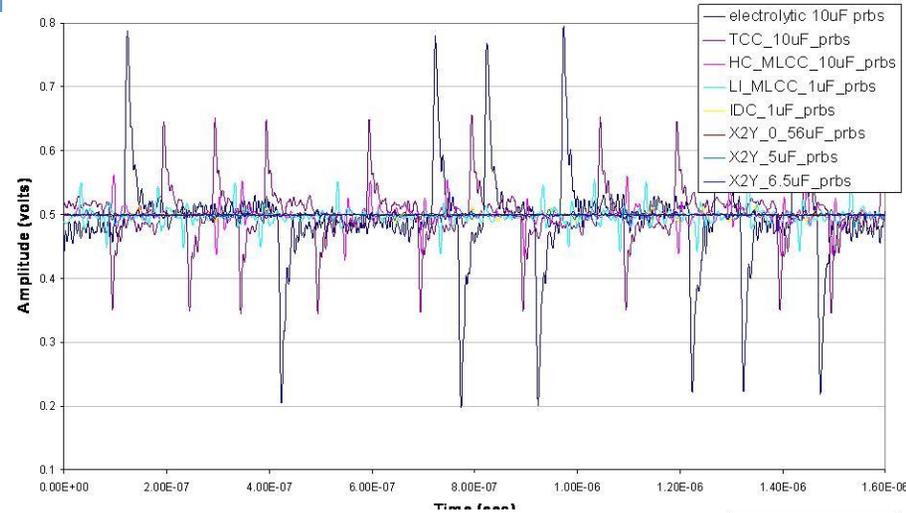
# X2Y® Components (Overview)

## Time-Domain Testing (Random Pattern)

- 70 ps rise/fall time
- 1 GHz Frequency
- 20 GS/s sampling rate

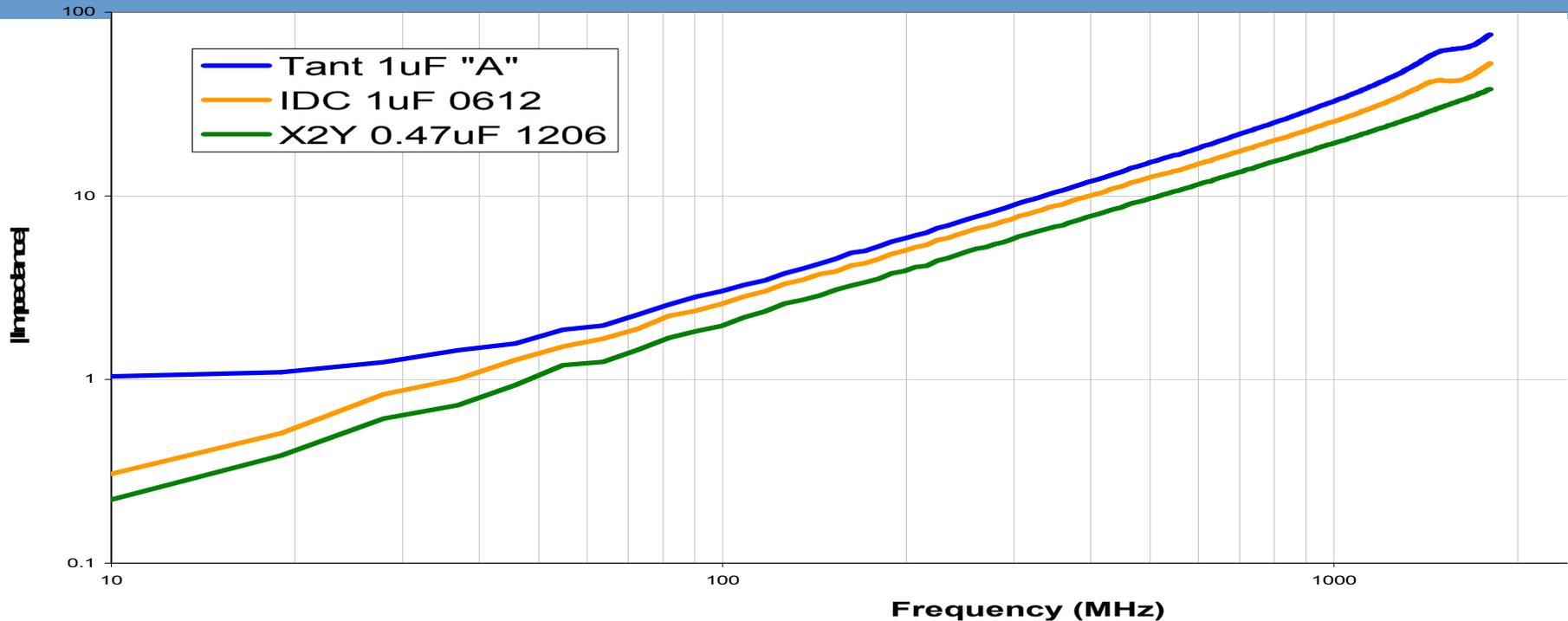
Data courtesy of Kevin Slattery, Intel Corporation.

Component	Random $\Delta$ Peak-to-Peak
Electrolytic 10uF	597 mV
Tantalum 10uF	311 mV
Std. MLCC 10uF	134 mV
LL MLCC 1.0uF	116 mV
<b>IDC™ 1.0uF</b>	<b>25.3 mV</b>
<b>X2Y® 0.56uF (1.12uF total)</b>	<b>15.5 mV</b>
X2Y® 5.0uF (10uF total)	17.2 mV
X2Y® 6.5uF (13uF total)	14.2 mV



Sanders, Muccioli, North, and Slattery, "The Quantitative Measurement of the Effectiveness of Decoupling Capacitors in Controlling Switching Transients from Microprocessors," CARTS 2005 USA, Palm Springs, CA, March 2005.

# X2Y<sup>®</sup> Components (Overview)



## Impedance Analyzer Measurements

- Impedance measurement taken on Agilent 4396B Impedance Analyzer
- Note: X2Y total capacitance value = 0.94uF

Data courtesy of Kevin Slattery, Intel Corporation.

# X2Y<sup>®</sup> Components (Overview)

## X2Y<sup>®</sup> vs. other IPD (Integrated Passive Devices)

- The X2Y<sup>®</sup> Technology Advantage

	X2Y <sup>®</sup> Technology	Other IPD
Package Size	✓ Can be manufactured in any package size and still maintain low-inductive performance.	Limited to 0612 or smaller package size to maintain low-inductive performance.
Capacitance Value	✓ Can be manufactured in any capacitive value current technology allows and still maintain low-inductive performance due to package size advantage.	Limited to smaller package sizes for low-inductive performance, thus limited to the amount of capacitance smaller package sizes will allow.
Number of Terminations	✓ 4	8
Number of Solder Joints	✓ 4	8
Number of Vias	✓ 6	8
Via Size	✓ Any	Small or micro-vias, large vias increase pad inductance.
Low-Inductance	✓ Premier	Good
Sourcing	✓ Multiple Manufactures	Single Sourced
Cost	✓ Good value	Expensive

## Summary

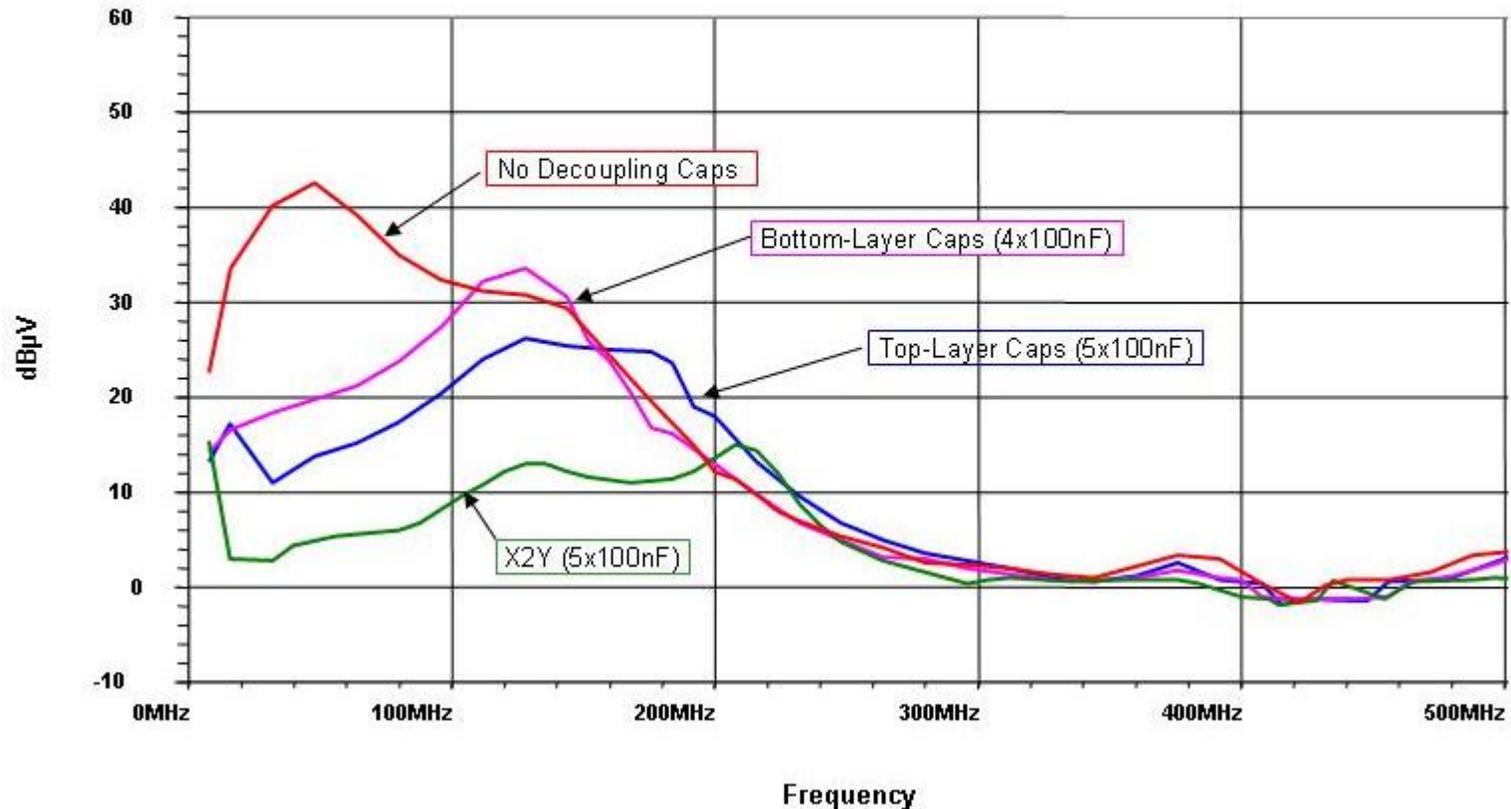
- X2Y<sup>®</sup> is a capacitive circuit capable of different modes of operation (Circuit 1 & Circuit 2).
- X2Y<sup>®</sup> requires connections at all 4 terminals to fully realize the performance benefits.
- X2Y<sup>®</sup> is the premier IPD Technology.
- For more application information on the X2Y<sup>®</sup> Technology go to [www.x2y.com](http://www.x2y.com).

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# IC Conducted/Radiated Emissions (Filtering)

## Comparison Of Decoupling Capacitors Using A 150-ohm Measurement Resistor

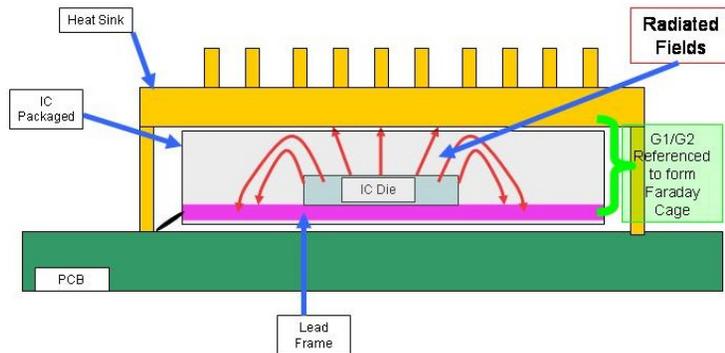
IEC 61967-4 Document 47A/566/CD Measurement of conducted emissions, 1 ohm/150 ohm direct coupling method



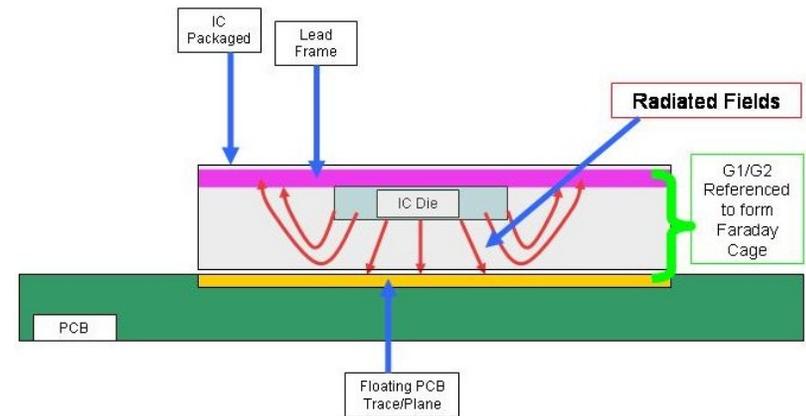
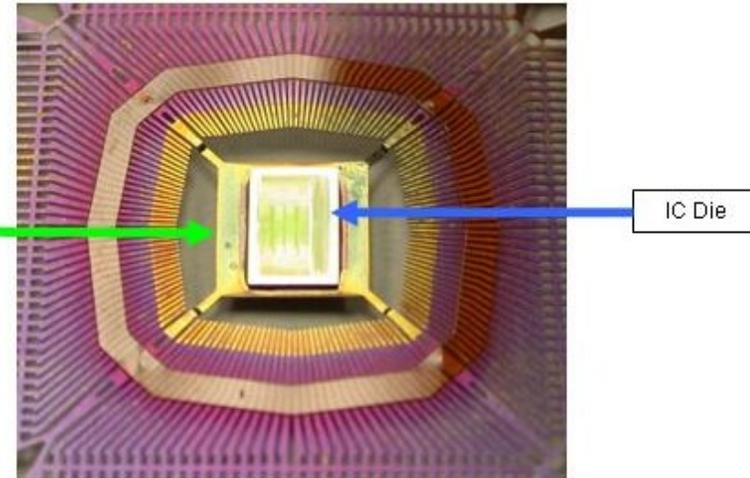
# IC Conducted/Radiated Emissions (Filtering)

## Existing Structures – “quasi” Faraday Cage

- Lead frame
- Heat sinks
- Image planes
- Housings



The Heat Sink and Lead Frame Create a Faraday Cage.



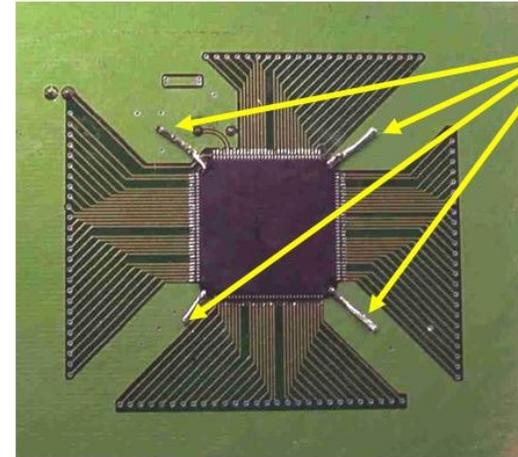
The PCB Trace/Plane and Lead Frame Create a Faraday Cage.

X2Y Application Note #3002 - IC Decoupling and EMI Suppression using X2Y® Technology

# IC Conducted/Radiated Emissions (Filtering)

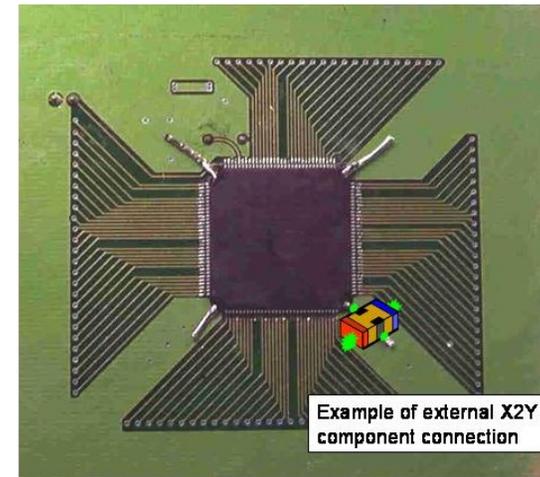
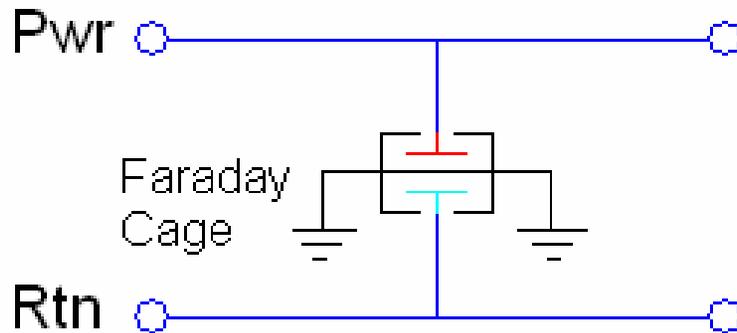
## Applying X2Y<sup>®</sup> to cancel emissions

- “A” and “B” terminal attach to power and ground
- “G1” and “G2” attach to Faraday Cage structure (i.e. image plane, heatsink, lead frame, housing).



RF Image Strip Leads

## Circuit 1



For optimum performance a low-inductance shunting or canceling device should be used between Pwr, GND, and Image Strip. The low-inductive device can be placed internally or externally of the IC package

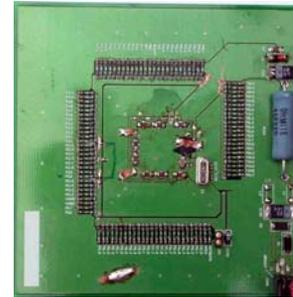
X2Y Application Note #3002 - IC Decoupling and EMI Suppression using X2Y<sup>®</sup> Technology

# IC Radiated Emissions Testing

## IEC 68167: Integrated Circuits, Measurement of radiated emissions - TEM-cell and wideband TEM-cell method



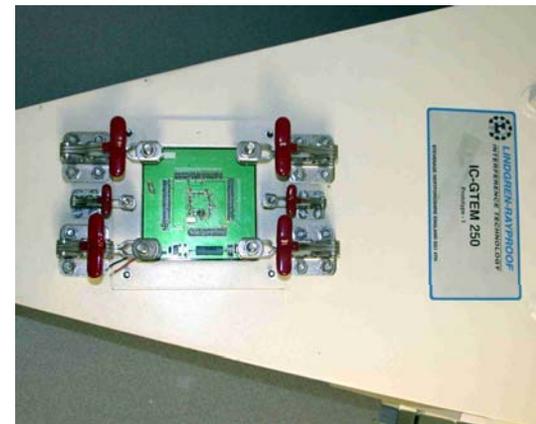
Test Board looking from Inside of TEM-cell



Test Board looking from outside of TEM-cell



ETS-LINDGREN GTEM Model 5402 [www.emctest.com](http://www.emctest.com)



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# Conclusion/Questions

## Questions?

Please Contact:

X2Y Attenuators, LLC

37554 Hills Tech Dr.

Farmington Hills, MI 48331

248-489-0007

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## Additional Resources

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