Technology In Balance

Speeding Edge “Current Source”

Article by John Zasio  Vol. 1, Issue 4
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Article Summary

- Article expresses an obvious negative bias with openly derisive language. Article purports to address:
  - “…information floating around the electronics industry regarding the “magic” of the X2Y® capacitor in terms of its decoupling capabilities.”

- Article claims interest in describing / characterizing X2Y® versus conventional 0402 capacitors.

- Article concludes that X2Y®s only slightly outperform 4 via 0402s, and actually require more vias to do the same job.

- Article was produced without any consultation with X2Y®

- This presentation debunks the article.
  - Article based on disastrously bad footprints for X2Y®
What’s wrong with this picture?

“The footprints shown in Figure 4 were designed for low inductance.”

- John Zasio on the test layouts used by Speeding Edge to compare X2Y® and 0402 capacitors.
Speeding Edge Test Footprints

- X2Y® layout is a very poor design
  - Vias located far from component
  - Vias widely separated from each other

- 0402 layouts very different
  - Vias annular rings directly abut device terminals
  - Vias tightly spaced
Speeding Edge Test Footprints

- Zasio X2Y® layout is **THREE** times the area of recommended X2Y layout.
- Zasio X2Y® layout actually has room for **FIVE** X2Y® caps.

“The footprints shown in Figure 4 were designed for low inductance.”
Impact of Via Locations on Inductance

- Numerous citations are available demonstrating the relation of via placement and geometry to bypass capacitor inductance
  - [www.sigcon.com/Pubs/news/6_09.htm](http://www.sigcon.com/Pubs/news/6_09.htm)
  - [www.sigcon.com/Pubs/edn/ParasiticInductance.htm](http://www.sigcon.com/Pubs/edn/ParasiticInductance.htm)
    - Published EDN July 2000
  - “Right the First Time”, 2003 pp 140 John Zasio
    - “Smaller length conductors and close spacing between the conductors decreases the inductance.” Zasio on bypass capacitor via geometry.

- The high influence of via location and geometry was clearly well known to Zasio when he devised the very poor X2Y® footprint used for his tests
Summary

- Footprint area $3X$ vs recommended.
- Via centers located $3X$ as far from component terminals vs recommended.
  - Capacitor ESL to planes high in the board $\approx 2X$ value with recommended footprint
- Vias spaced $1.8X$ vs recommended.
  - Expected in-cavity inductance $\approx 1.5X$ value with recommended footprint
- Artificially poor layout used for X2Y® capacitors severely skewed obtainable results