

Grounding Requirements for Optimum Performance Results with X2Y[®] Technology on a Printed Circuit Board

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Abstract—With the introduction of the X2Y[®] Technology in decoupling applications, a critical scientific study investigating and documenting the technology’s attachment relationship to a printed circuit board’s power and ground planes is needed. The goal of this paper is to test and document the performance of the X2Y[®] Technology in a Circuit 2 configuration, utilizing different land pad configurations.

Keywords—X2Y[®]; X2Y[®] Technology; filtering; Radiated Emissions; cancellation; passive component; Circuit 2;

I. INTRODUCTION

X2Y[®] Technology is the newest approach in passive component technology for decoupling applications.[1], [2], and [3] have shown benefits of using the X2Y[®] Technology over standard Multi-Layered Ceramic Capacitors (MLCC) and other technologies. MLCCs typically are used to supply energy to suppress transients while applying brute force (shunting) as a low-pass filter to remove unwanted higher frequency common mode and differential mode noise. The X2Y[®] Technology differs from this in that the unique structure is utilized for broadband E- and H-field cancellation of noise while providing the apparent energy. The structure promotes the cancellation of mutual inductance internally which in turn provides a low-impedance for unwanted noise. The structure is similar to a traditional bypass capacitor structure with separately terminated ‘A’ and ‘B’ electrode layers. The difference is additional terminated reference (ground) electrode layers (the terminations are ‘G1’ and ‘G2’) are layered between, above, and below the ‘A’ and ‘B’ electrodes encompassing the E- and H- fields from them. This forms a quasi Faraday Cage and provides a common reference for the ‘A’ and ‘B’ electrodes promoting the cancellation of the internal mutual inductance (Fig. 1) [4]. The result is a 4-terminal device that comes in standard MLCC package sizes, 0603, 0805, 1206, 1210, 1410, 1812, and 2220.

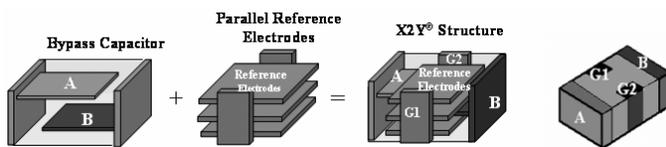


Figure 1. Depiction of X2Y[®] structure.

The connection configuration of the X2Y[®] component to a circuit can have several different orientations, thus modes of operation, with respect to the source and load. Changing the orientation utilizes structure in different ways. Thus, X2Y[®] components are viewed as symmetrically balanced capacitive circuits, not simply as a discrete passive device [5]. (It should be noted that the X2Y[®] chip components are applied to circuits in bypass and therefore should not be confused with chip feedthrough capacitors.)

For the purposes of this paper, the connection configuration utilized will be Circuit 2. (The Circuit 2 configuration has been defined by the inventor and manufacturers of X2Y[®] Technology [5].) Circuit 2 is a single ended application that utilizes two independent conductor connections to the structure. For the purposes of this paper the conductors are power and ground planes on a PCB (Fig. 2).

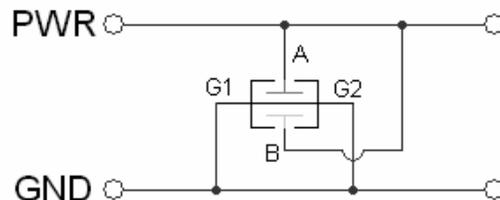


Figure 2. Circuit 2 schematic.

The capacitive rating of X2Y[®] components is a Line-to-ground measurement which divides the structure into two capacitive halves. For example, an X2Y[®] component with a 100nF capacitive rating has 100nF of capacitance between the ‘A’ terminal and the ‘G1’/‘G2’ terminals and 100nF of capacitance between the ‘B’ terminal and the ‘G1’/‘G2’ terminals (C_y in Fig. 3). Therefore in a Circuit 2 configuration, the total capacitance supplied between the power and ground planes is 200nF or twice the capacitive rating ($C_y + C_y$ in Fig. 3). Unsorted X2Y[®] components have a variance of 2.5% or less in X7R dielectric between the capacitive halves due to the shared electrodes and dielectric, which additionally allows capacitive tolerance to be maintained over temperature and time (aging).

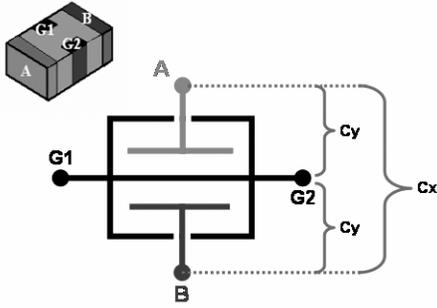


Figure 3. Illustration of X2Y[®] capacitive rating.

II. TEST PROTOCOL

The test protocol consisted of twelve FR4 laminated PCBs with over-all dimensions of length = 1.25", width = 1.2", and thickness = 0.062" each. The PCBs consist of 3 layers with layer spacing as shown in Fig. 4.

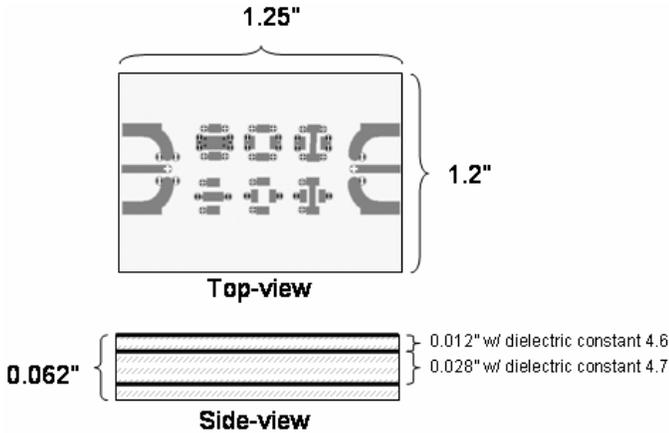


Figure 4. Test PCB's layering structure.

The PCBs were divided into two control groups, Board A and Board B. Board A used the first inner copper plane below the DUT (X2Y[®] component) as power and the second for ground. For Board B, the inner planes were reversed with ground under the DUT followed by power (see Fig. 5).

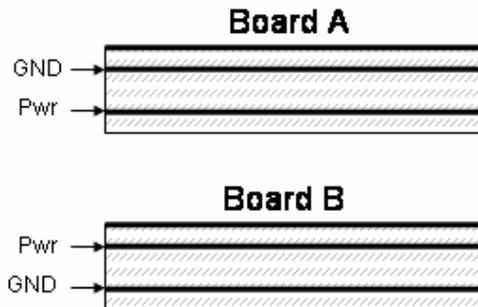


Figure 5. Plane assignment for Board A and Board B.

The top-layer (where DUT is soldered) is identical for the twelve boards as shown in Fig. 6. The layout consisted of SMA footprints located to the left and right of the PCBs using 0.041"

round, 0.020" hole vias to the power and ground planes. Layout footprints for the DUT consisted of three configurations:

- Three landpads where the G1 and G2 pads are connected with a solid trace.
- Four landpads, one for each termination of the DUT (X2Y[®] component).
- Three landpads where the A and B pads are connected with a solid trace.

Each PCB has two sets of these DUT footprints outlined above. They are equally spaced above and below from the direct line of sight of the SMA connections. The upper footprints have two vias per terminal of the DUT and the lower footprints have one via per terminal of the DUT. The vias to the power and ground planes are 0.037" round, 0.020" hole vias.

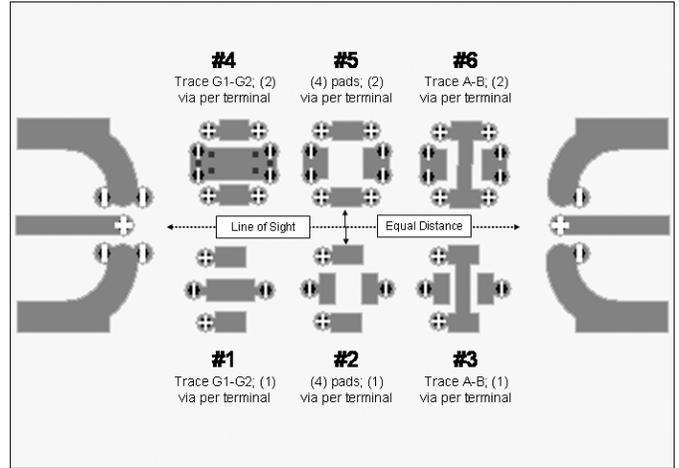


Figure 6. Landpad layout geometry for both Board A and Board B.

To add additional controls to the analysis, s_{21} (insertion loss) measurements of each of the twelve boards were taken without DUTs attached (Fig. 7) using a Vector Network Analyzer (VNA). (For the set-up of the VNA see TABLE 1.) For the DUTs themselves, s_{21} measurements were taken on twelve separate 1206 (100nF) X2Y[®] components with a microwave test fixture verifying uniformity of the DUTs (Fig. 8). (Information on the microwave test fixture can be found in [6].) Note that all measurements in this paper were insertion loss measurements taken with the VNA and converted to impedance using the following formula from [7]:

$$|S_{21}| = 20 \log_{10} \left| \frac{Z_{DUT}}{25\Omega} \right| \quad (1)$$

TABLE I. SET-UP PARAMETERS FOR VNA.

HP8753E		
CHAN	MEAS	FORMAT
1	S21	LOG_MAG
CHAN_START FREQ	CHAN_STOP_ FREQ	
30000	6E+09	
POINTS	POWER	IF_BW
1601	0.00E+00	100

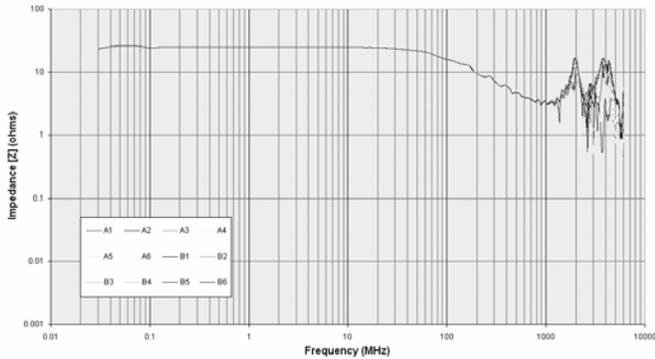


Figure 7. All twelve test PCB's impedance measurements.

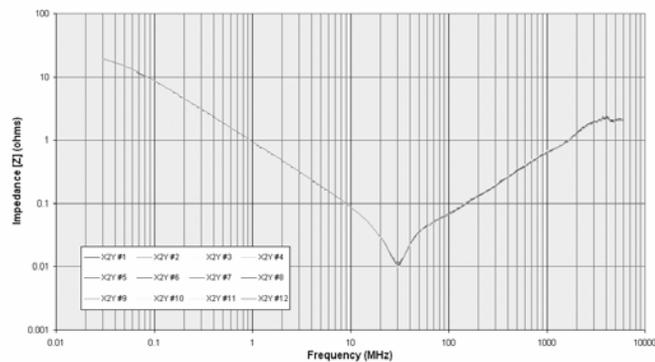


Figure 8. All twelve X2Y[®] components used for testing were measured on a microwave test fixture. The X2Y[®] components used are Phycomp 1206 X7R (100nF) 63v Lot # 225908125749 in a Circuit 2 configuration.

III. ANALYSIS RESULTS

One DUT, 1206 X2Y[®] (100nF), was placed on separate positions on each of the twelve PCBs. The results are shown two different ways. Fig. 9 show the results of the six landpad configurations for Board A. Fig. 10 show the results of the six landpad configurations for Board B. Fig. 11 compare the one via per landpad for Board A versus Board B. Fig. 12 compares the two via per landpad for Board A versus Board B.

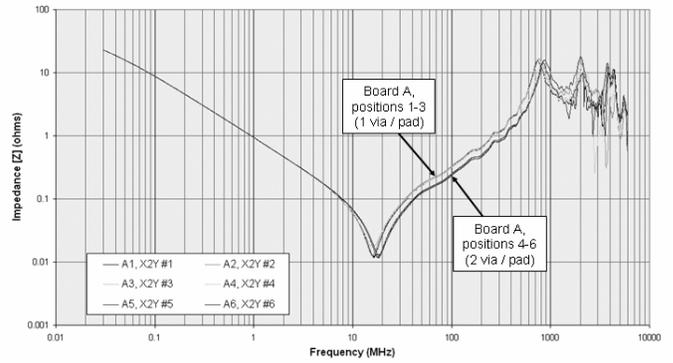


Figure 9. Comparison of the 6 landpad geometries on Board A.

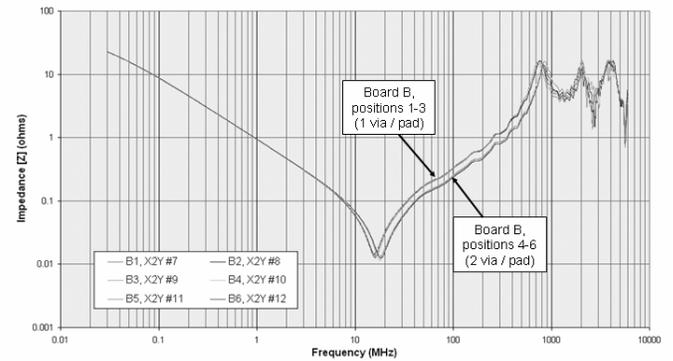


Figure 10. Comparison of the 6 landpad geometries on Board B.

Both Fig. 9 and Fig. 10 show lower impedance for the two via per landpad configurations versus the one via per landpad, but no difference between the layout footprint geometries themselves. This means that impedance is not affected by landpad geometry, but only by the number of vias used.

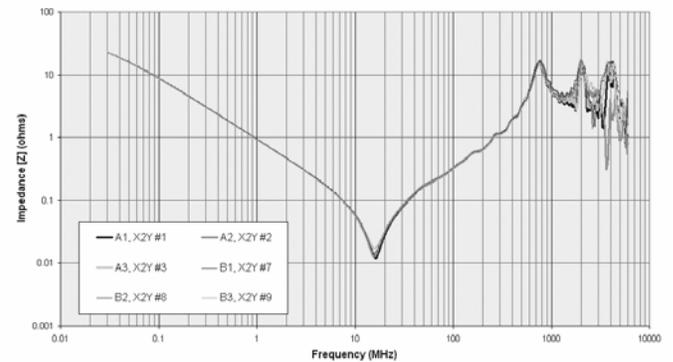


Figure 11. Comparison of landpad positions 1-3 on Board A and Board B.

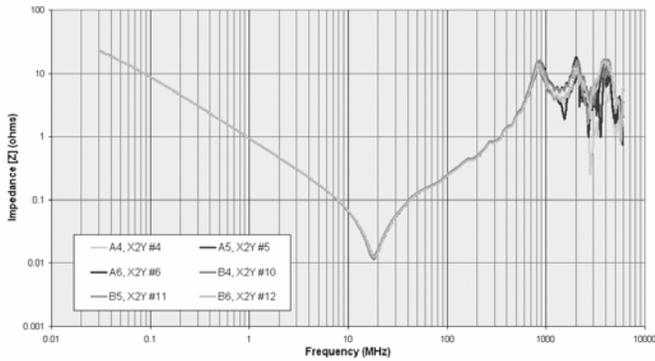


Figure 12. Comparison of landpad positions 4-6 on Board A and Board B.

Fig. 11 and Fig. 12 show that the plane assignment (power or ground) directly below the DUT has no effect on the impedance between Board A and Board B.

IV. CONCLUSIONS

The X2Y[®] Technology has been shown to provide the desired broadband low-impedance for decoupling applications in the previously mentioned work ([1], [2], and [3]). The goal of this paper was to document the parameters between the relationship of the X2Y[®] Technology Circuit 2 configuration and the PCB. The conclusions that can be drawn from this paper are:

1. Power/Ground plane assignment below the X2Y[®] Technology has no effect on impedance.
2. Landpad geometry has no affect on the impedance of the X2Y[®] Technology.
3. To lower the impedance of the X2Y[®] Technology with respect to PCB attachment, multiple vias need to be used.

Recommended future work would be to investigate and document the same parameter using the X2Y[®] Technology in a Circuit 1 configuration.

ACKNOWLEDGMENTS

We would like to thank Dave Anthony, Ken Musil, and William Anthony for their comments and time they took reviewing our paper.

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