X2Y® Technology Used for Decoupling

D L Sanders
X2Y Attenuators, LLC
USA

J P Muccioli
X2Y Attenuators, LLC
USA

A A Anthony
X2Y Attenuators, LLC
USA

D J Anthony
X2Y Attenuators, LLC
USA

***Abstract*—Power distribution systems (PDS) on printed circuit boards (PCB) have ever increasing complexities associated with them. Multiple voltages, lower voltage levels, higher frequency content, increasing supply demands, and parasitics magnify sensitivities to transients and noise voltage/current. Capacitors are typically used as a local source of energy to suppress transients and provide a low-pass filter operation for noise by providing low impedance. This paper investigates the impedance properties of standard multlayer ceramic capacitors (MLCCs) and compares them to the X2Y® Technology Circuit 2 configuration for use in decoupling applications.**

Keywords-X2Y®; X2Y® Technology; decoupling; cancellation; passive component;

I. INTRODUCTION – IMPEDANCE VS. FREQUENCY FOR STANDARD MLCC

[1] states that effective series inductance is only affected by the geometry of the conductive region for bypass capacitors. For MLCCs, this means that parasitic inductance correlates directly with the physical package size and not the capacitance value or dielectric.

Figure 1 – Figure 3 uses a capacitor library to show typical impedance trends of MLCC package size, capacitive value, and dielectric substrates [2].

Figure 1 examines the impedance beyond self-resonant frequency (SRF) of different package size MLCCs. The same capacitive value (0.1uF) and dielectric (X7R) is used to compare a 0603, 0805, 1206, 1812 package size MLCC. One can see that as the package size increases, so does the impedance beyond SRF. Smaller is better!

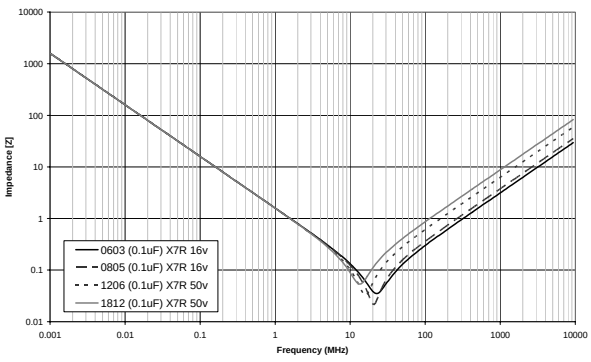

Figure 1. Impedance beyond SRF is lower for smaller packaged MLCCs.

Figure 2 examines the impedance beyond SRF for different capacitive values. The same package size (1812) and dielectric (X7R) is used to compare capacitive values 0.22uF, 0.33uF, 0.47uF, and 1uF. Figure 2 clearly shows that the impedance beyond SRF is not related to the capacitive value.

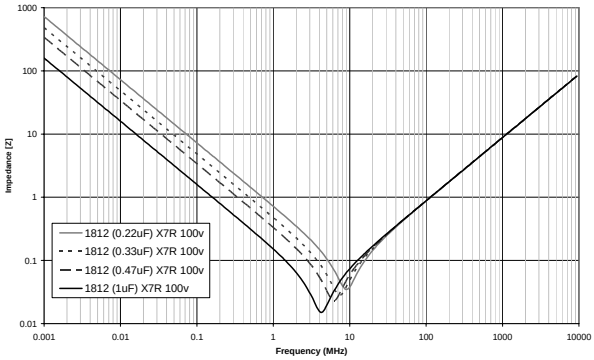

Figure 2. Impedance beyond SRF is independent of capacitive value.

Lastly, Figure 3 examines the impedance beyond SRF for different dielectric MLCCs. The same package size (1812) was used to compare NPO, X7R, and Y5V dielectrics. (Note: different capacitive values were used due to value limitations of the library.) Figure 3 demonstrates that the impedance beyond SRF is independent of dielectric substrate used.

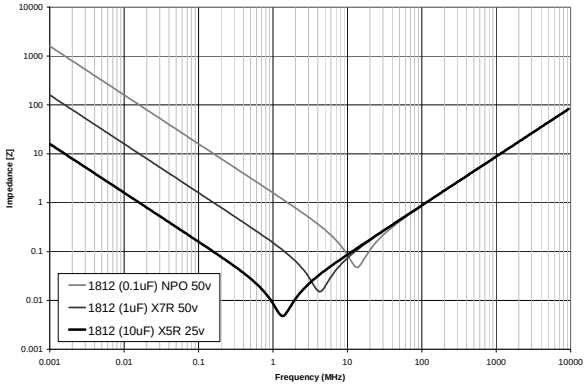

Figure 3. Impedance beyond SRF is independent of dielectric substrate.

II. X2Y® TECHNOLOGY AND TEST PROTOCOL

The X2Y® Chip Technology is a 4-terminal device that comes in standard MLCC package sizes: 0603, 0805, 1206, 1210, 1410, 1812, and 2220.

For the purposes of this paper, the connection configuration utilized will be Circuit 2. (The Circuit 2 configuration has been defined by the inventor and manufacturers of X2Y® Technology [3].) Circuit 2 is a single-ended application that utilizes two independent conductor connections to the structure. In the case of this paper, the conductors are signal and return Figure 4.

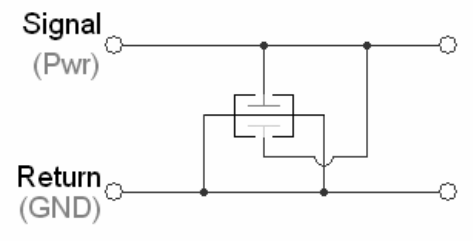

Figure 4. Circuit 2 schematic. (Note: that the connections are parallel to the Signal and Return.)

The capacitive ratings of X2Y® components are a Line-to-ground measurement which divides the structure into two capacitive halves. The orientation of the Circuit 2 configuration (with respect to the source and load) places both capacitive halves in parallel. This means that a X2Y® component in a Circuit 2 orientation supplies twice the rated capacitance value to a circuit (Figure 5) [4].

For example, an X2Y® component with a 100nF capacitive rating has 100nF of capacitance between the 'A' terminal and the 'G1'/'G2' terminals and 100nF of capacitance between the 'B' terminal and the 'G1'/'G2' terminals. Since both the 'A' and 'B' terminals are attached to the signal trace and the 'G1' and 'G2' terminals are attached to the return trace, both capacitive halves are in parallel with the traces (source and load), thus the total capacitance is supplied is 200nF.

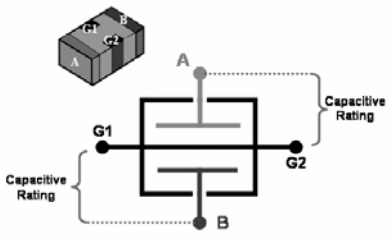

Figure 5. Illistration of X2Y® capacitive rating.

Tolerance between capacitive halves of X2Y® components is typically ±2.5% unsorted which is maintained over temperature and time (aging) due to the shared dielectric and electrodes [5].

Evaluation measurements for this paper utilize a Hewlett Packard 2-port Vector Network Analyzer (VNA) (model HP 8753E) with test set cables (HP 11587D). TABLE I. lists the VNA set-up and parameters.

TABLE I. VNA PARAMETERS

Points:	801
Start/Stop:	30kHz - 6GHz
IF Bandwidth:	100Hz
Span:	30kHz - 6GHz
Format:	Log Mag
Measurement:	S21
Data:	Log Scale

Insertion loss measurements (S21) from the VNA are then converted in a spreadsheet to impedance (Z) using the following equation from [9]:

$$|S_{21}| = 20\log_{10}\frac{|Z_{DUT}|}{25\Omega} \qquad \text{(Equation 1)}$$

Two types of test fixtures are used to measure impedance performance. The first fixture is a microstrip–PCB with an overall dimension of 28mm x 28mm made with an FR-4 substrate. The microstrip–PCB is double layered, 1.0688mm thick, with a relative permittivity of 4.6. The signal trace is 1.345mm and the ground trace widths are 12.9475mm. SMA connectors are soldered at each end of the signal trace (Figure 6).

(Note: in order to use multiple package sizes with one size microstrip–PCB, a modified–Circuit 2 configuration was used. Due to the symmetry of the X2Y® structure, performance difference between Circuit 2 and modified–Circuit 2 is nominal. This is documented in [4]. In addition, to test a 0603 package X2Y®, the signal trace was narrowed under the component. This had nominal effect on the microstrip–PCB impedance/S21 measurements as shown in Figure 9.)

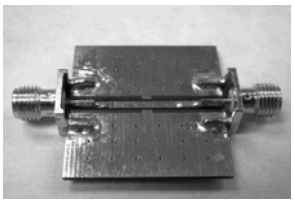

Figure 6. Microstrip-PCB and modified-Circuit 2 schematic.

The second type of test fixture is a series of three via-PCBs which use vias to connect the component to planes. SMA connectors are attached to the left and right sides of the via-PCBs (Figure 7 and 8). The original purpose of the boards was to identify optimal via sizes and layout configurations for X2Y® components along with other devices. The arrows in Figure 7 and 8 identify which component layouts were used for this paper.

The via–PCBs are 4 layer boards with an overall size of 1.2" by 1.2" and 0.062" thick made of FR-4. The planes are solid copper with a weight of 1 ounce located 0.012" and 0.05" from the component's surface. The nominal Er is 4.6 at 1MHz. (For further documentation see [7].)

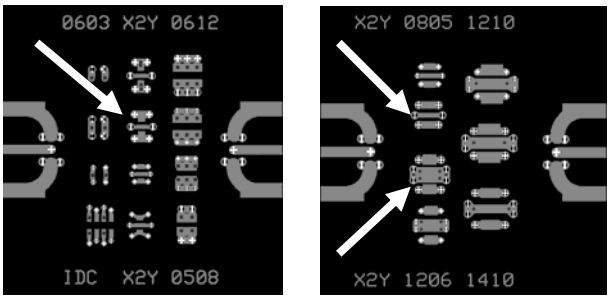

Figure 7. 0603 via-PCB (top-left) & 0805 & 1206 via-PCB (top-right).

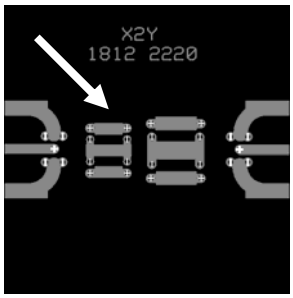

Figure 8. 1812 via-PCB.

Figure 9 provides impedance measurements on all PCB test fixtures used in this paper. The PCBs provide comparable impedance correlation to 300MHz.

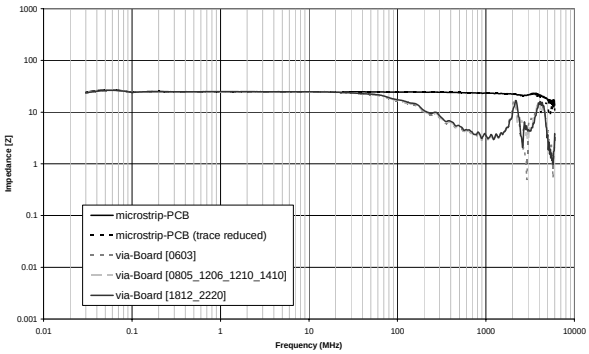

Figure 9. PCB impedance plots.

III. X2Y® PACKAGE SIZE AND INDUCTANCE BEYOND SRF

This section evaluates the correlation between package size and impedance of the X2Y® Technology beyond SRF. The DUTs are:

- X2Y® 0603 (0.1uF) X7R 10v
- X2Y® 0805 (0.1uF) X7R 16v
- X2Y® 1206 (0.1uF) X7R 63v
- X2Y® 1812 (1uF) X7R 25v

(Note: an 1812 (0.1uF) was not available at the time testing was conducted.)

Figure 10 shows the impedance measured on the microstrip-PCB and Figure 11 shows the impedance measured on the via-PCBs.

Both Figure 10 and 11 demonstrate that the impedance/inductance beyond SRF improves with package size. This is contrary to what was demonstrated by standard MLCC in Section I of this paper.

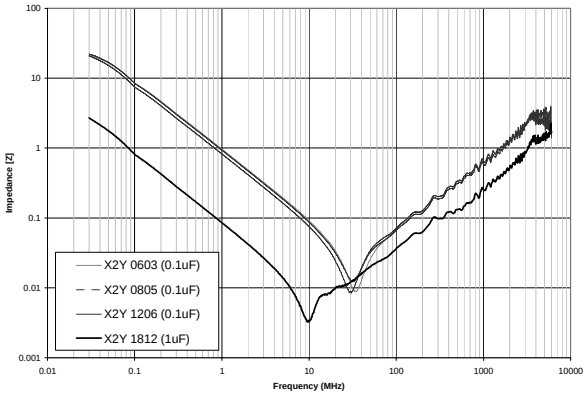

Figure 10. Microstrip-PCB impedance plot comparing different package sizes.

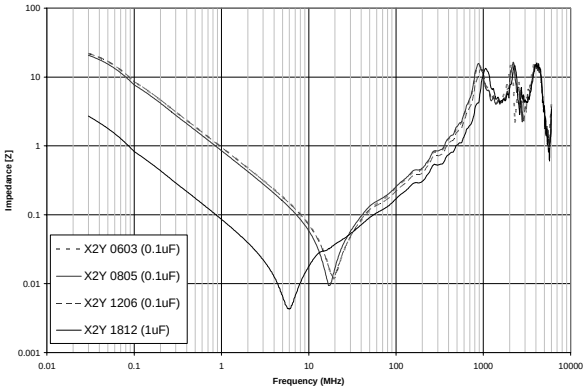

Figure 11. Via-PCB impedance plot comparing different package sizes.

IV. X2Y® CAPACITIVE VALUE AND INDUCTANCE BEYOND SRF

This section evaluates the correlation between capacitance value and impedance of the X2Y® Technology beyond SRF. The package size (1812) and dielectric (X7R) are held constant while the capacitance value is varied. The DUTs are :

- X2Y® 1812 (0.22uF) X7R 100v
- X2Y® 1812 (0.33uF) X7R 100v
- X2Y® 1812 (1uF) X7R 25v

Figure 12 shows the impedance measured on the microstrip-PCB and Figure 13 shows the impedance measured on the via-PCBs.

Both Figure 12 and 13 demonstrate that the impedance/inductance beyond SRF improves with larger capacitive values. Again, this is contrary to what was demonstrated by standard MLCC in Section I of this paper.

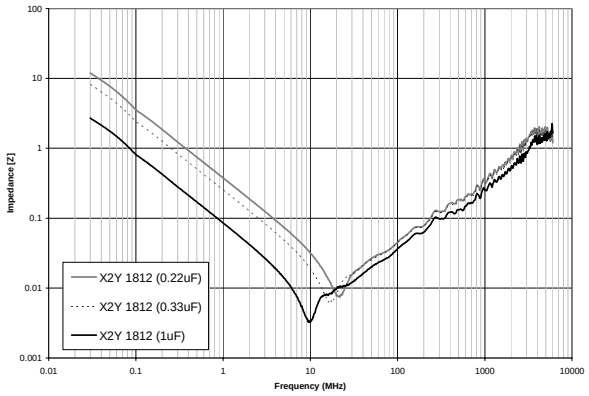

Figure 12. Microstrip-PCB plot comparing different capacitance values.

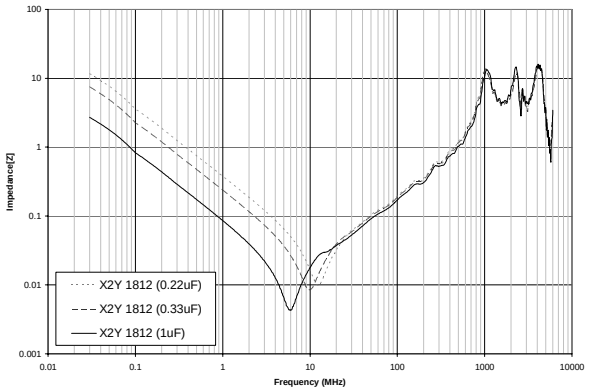

Figure 13. Via-PCB plot comparing different capacitance values.

V. UNDERSTANDING THE X2Y® TECHNOLOGY

The unexpected behavior of the X2Y® Technology is the result of internal structural improvements over standard MLCC. The X2Y® structure is comprised of alternating electrodes ('A' and 'B') encompassed by three connected (top, middle, and bottom) dual terminated ('G1' and 'G2') parallel electrodes that form a quasi Faraday Cage (Figure 14) [5].

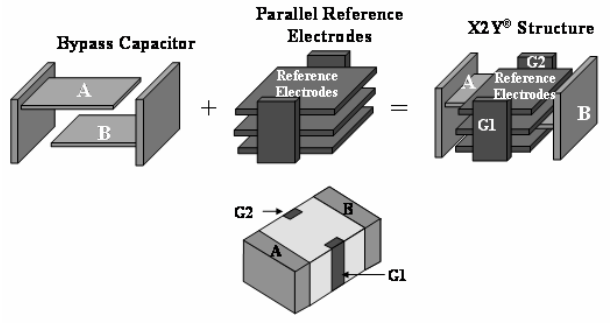

Figure 14. Dipiction of X2Y® structure.

The structure and circuit orientation (Circuit 2 configuration) dictate that the current path on the 'A' and 'B' electrodes are in opposing directions. The reference electrodes provide a common return path for both the 'A' and 'B' electrodes. Opposing currents and resulting H-fields returning on a common reference electrode cancel mutual inductance (right-hand-rule) [8].

In addition, the geometry of the conductive region (which is responsible for the effective series inductance as stated earlier) is no longer the distance from the 'A' to 'B' terminals as with standard MLCCs. The conductive region is now a dual parallel path ('A' to 'G1'/'G2' and 'B' to 'G1'/'G2') approximately half the physical distance of standard MLCCs [9].

Understanding the benefits of the structure is the key to explaining the data presented in Section III & IV. The data shows that the larger package components (Section III) and biggest capacitive values (Section IV) have the lowest impedance.

The electrodes for the larger package X2Y® components further maximize the mutual inductance cancellation by providing a larger surface area for cancellation to occur.

The larger capacitive value components contain more electrodes in the structure. The result is a 'more' parallel structure and reduced dielectric thickness between the electrodes (per given voltage rating and package size), which further promotes cancellation and thus lower impedance.

VI. WHAT CAN X2Y® TECHNOLOGY DO FOR DECOUPLING APPLICATIONS?

Typically in order to meet impedance and energy requirements, multiple smaller packaged MLCCs are configured in parallel on a PCB. Figure 15 and 16 use (5) different value 0805 MLCCs in parallel on the microstrip-PCB and compares their combined impedance to a single 1812 X2Y® component of equivalent total capacitance value (0.47uF). (Note: the dashed lines are the individual 0805 values.) In both examples, the single X2Y® was as good as or better than the (5) 0805 MLCCs in parallel. Additionally, the (5) component configuration had significant unwanted anti-resonances.

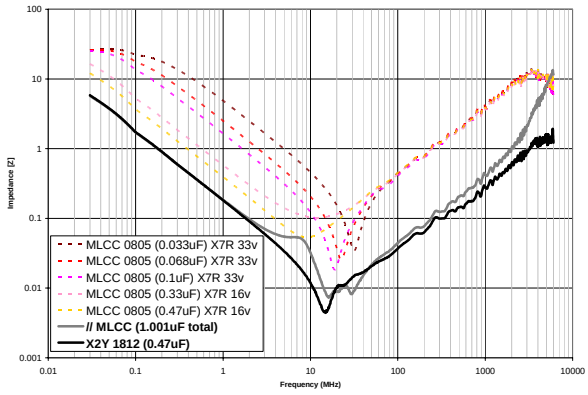

Figure 15. Multiple different value 0805 MLCCs in parallel compared to a single equivalent value 1812 X2Y® component.

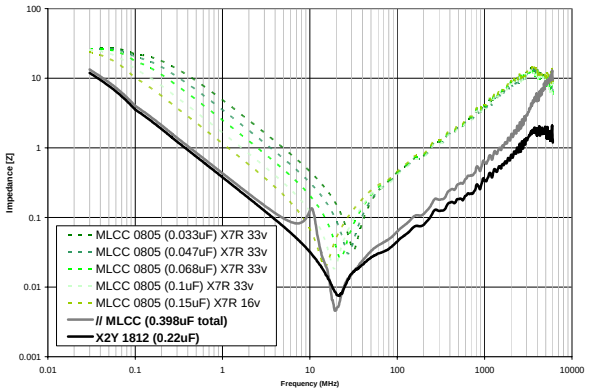

Figure 16. Multiple different value 0805 MLCCs in parallel compared to a single equivalent value 1812 X2Y® component.

In order to minimize the unwanted anti-resonance, Figure 17 uses same value (0.1uF) 0805 MLCC to repeat the impedance measurements [10]. Each capacitor is added one at a time to demonstrate the impedance progression and is then compared against a single 1812 X2Y® component of equivalent total capacitance value (0.22uF). Again the single X2Y® was as good as or better than the (5) 0805 MLCCs in parallel and without any significant anti-resonances.

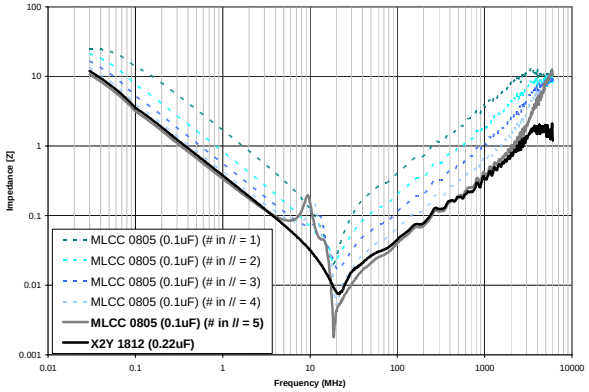

Figure 17. Multiple same value 0805 MLCCs in parallel compared to a single equivalent value 1812 X2Y® component.

VII. Conclusions

Section III and IV demonstrate that larger package and higher capacitance values are desirable for the X2Y® Technology. Bigger is better!

Section VI demonstrates a 5:1 ratio in comparable impedance performance between the X2Y® Technology and standard MLCC on a microstrip-PCB.

Ongoing research and testing that will be presented at the time of this paper will show if this ratio holds true when vias are used.

Preliminary testing and calculations done at the time of publication shows a 4:1 (MLCC:X2Y®) component ratio with a 16:6 (MLCC:X2Y®) via ratio when using vias.

Recommended future work would be a cost analysis study and testing on larger capacitive value (1-100uF) X2Y® components in Y5V and X5R dielectrics.

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