Presented by: Dale L. Sanders

Reducing Switching Transients from ICs in Power Distribution Systems (PDS) on PCBs
Basic PDS Model – Source, Path, Receiver

- **Source** – power supplied to PCB
- **Path** – PCB planes
- **Receiver** – ICs

Ensure “clean” power
- Supply instantaneous current for switching IC
- Filter high frequency transients

- **Capacitors**
  - Large value Caps – supply energy
  - High Freq. Caps – Filter
What are PDS design issues?

- Inductance
  - Caps
  - Vias
  - Component mounting
  - PCB plane
  - Package

- PCB real-estate
  - Number of caps & vias
  - Location/effectiveness
  - Placement cost
  - Multiple power planes

- Signal Integrity (SI)
  - Number of vias (routing)
  - Manufacturing cost (multiple plane PCBs)
  - Functionality
Power Distribution System (PDS) [EXAMPLE]

Smaller is better – 0603 has less inductance than 0805, 1206, 1812.

To meet total capacitance requirements typically small caps increase the number of caps needed. (Package size limits number of layers.)

Larger number of caps require more vias & greater distance from IC. (More PCB space)

**X2Y® Technology**

- Capacitive Circuit
  - Circuit 1 – 3 conductor
  - Circuit 2 – 2 conductor
- 4 terminal device
- Layout attachment is inter-digitated
- Unless noted, X2Y® is Circuit 2 for this presentation

**IDC™**

- 8 terminal device
- Terminals are inter-digitated
Cap-only Performance Test Set-up

- Caps mounted to 50 ohm coplanar PCB.
- Shunt-through measurements
- Input waveform below

<table>
<thead>
<tr>
<th>Duty Cycle</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>50/50</td>
<td>100 kHz</td>
</tr>
<tr>
<td><strong>80/20</strong></td>
<td>1 MHz</td>
</tr>
<tr>
<td></td>
<td><strong>10 MHz</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Rise/Fall time</th>
<th>Amplitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 ns</td>
<td><strong>5 V</strong></td>
</tr>
<tr>
<td>5 ns</td>
<td>2.2 V</td>
</tr>
</tbody>
</table>


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Electrolytic & Tantalum Capacitors

- 80/20 duty cycle, 10 MHz, 1 ns rise/fall time, 5 V amplitude
- 47 uF needed to “smooth” ripple
- Minimal HF transient suppression.

- 80/20 duty cycle, 10 MHz, 1 ns rise/fall time, 5 V amplitude
- 1 uF needed to “smooth” ripple
- X2Y® & IDC™ suppress HF transients.
- Note: X2Y total capacitance value = 0.94uF
- Note: Amplitude scale – order of magnitude smaller than previous slide

Additional High Frequency Test #1 – 50/50 Clock

- 50/50 duty cycle, 1 GHz, 70 ps rise/fall time
- Note: X2Y total capacitance value = 1.12uF
- Note: Amplitude scale – order of magnitude smaller than previous slide

Data courtesy of Kevin Slattery, Intel Corporation.
Additional High Frequency Test #2 - Random

- Random duty cycle, 1 GHz, 70 ps rise/fall time
- Note: X2Y total capacitance value = 1.12uF

Data courtesy of Kevin Slattery, Intel Corporation.
Insertion Loss Measurements

- Insertion Loss (dB) [S21] taken on Agilent ENA 5071A Network Analyzer
- Note: X2Y total capacitance value = 0.94uF & 1.12uF respectively

Impedance Measurements

- Impedance measurement taken on Agilent 4396B Impedance Analyzer
- Note: X2Y total capacitance value = 0.94uF

Data courtesy of Kevin Slattery, Intel Corporation.
What is the Performance benefit of Low-Inductive Caps?

- Each MLCC measured individually
- Total (5) MLCC = 0.398uF
- X2Y total capacitance value = 0.44uF
- MLCC cumulative measured
- Total (5) MLCC = 0.5uF
- X2Y total capacitance value = 0.44uF

- Measurements made on 50ohm Coplanar PCB with Ground Plane.

Power Distribution System (PDS) [EXAMPLE]

How to Take Advantage of Low-Inductance Caps?

- **Lower Via/mounting Inductance**
  - Multiple parallel vias
  - Mutual inductance cancellation between vias
  - Reduce trace length from cap to via

- **Spreading Inductance**
  - Fewer low-inductance caps are required, therefore caps can be located closer to ICs.

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What Does Low-Inductance Caps Do for PDS?

- **Std. MLCC vs. X2Y® on Xilinx FPGA PCB.**

Table 1, Mounted Inductance, Comparative Conventional and X2Y³

<table>
<thead>
<tr>
<th></th>
<th>Capacitors on Component Side</th>
<th>Capacitors on Back side⁴</th>
</tr>
</thead>
<tbody>
<tr>
<td>H1</td>
<td>0.005 0.020 0.005 0.020 0.005 0.012 0.012</td>
<td>0.005 0.005 0.005</td>
</tr>
<tr>
<td>H2</td>
<td>0.014 0.003 0.003 0.001 0.001 0.038 0.038</td>
<td>0.014 0.003 0.001</td>
</tr>
<tr>
<td>S</td>
<td>0.03 0.03 0.03 0.03 0.03 0.032 0.044</td>
<td>0.03 0.03 0.03</td>
</tr>
<tr>
<td>D</td>
<td>0.01 0.01 0.01 0.01 0.01 0.02 0.02</td>
<td>0.01 0.01 0.01</td>
</tr>
<tr>
<td>K1 D/S</td>
<td>0.33 0.33 0.33 0.33 0.33 0.63 0.45</td>
<td>0.33 0.33 0.33</td>
</tr>
<tr>
<td>L / via pH</td>
<td>318 393 76 217 40 590 629</td>
<td>1580 1530 1540</td>
</tr>
<tr>
<td>L 0603</td>
<td>1052 1290 662 935 579 1500³ 1760</td>
<td>3670 3560 3590</td>
</tr>
<tr>
<td>L 0402</td>
<td>952 1190 552 835 479 1400 1660</td>
<td>3570 3460 3490</td>
</tr>
<tr>
<td>L X2Y</td>
<td>267 355 117 223 90 435 531⁶</td>
<td>1250 1210 1220</td>
</tr>
<tr>
<td>Caps req’d 0603</td>
<td>3.9 3.6 5.6 4.2 6.5 3.4 3.3</td>
<td>2.9 2.9 2.9</td>
</tr>
<tr>
<td>Caps req’d 0402</td>
<td>3.6 3.3 4.7 3.7 5.3 3.2 3.1</td>
<td>2.9 2.9 2.9</td>
</tr>
<tr>
<td>Caps req’d X2Y</td>
<td>1.0 1.0 1.0 1.0 1.0 1.0 1.0</td>
<td>1.0 1.0 1.0</td>
</tr>
</tbody>
</table>

Decoupling multiple power planes on PCB increases the number of standard caps needed.
Multi-Plane Test Fixture Insertion Loss

Circuit 1

Pwr 1

GND

Pwr 2

PCB Fixture

X2Y 0603 100nF

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X2Y® Circuit 1 --- Multi-Plane Decoupling

Ch 1 Input
Ch 2 Input

Ch 1 X2Y
Ch 2 X2Y
X2Y® Circuit 1 - Multi-Plane Decoupling (crosstalk)

Ch 1 X2Y
- Ch 2 X2Y
- Crosstalk Board
- Crosstalk X2Y
IPDs are the foremost capacitor technology that can supply the instantaneous current needs and HF transient filtering for ICs.

NEMI Roadmap shows IPDs offer cost advantages to OEMs by 2005.

BOM considerations for IPDs
- Fewer vias
- Fewer solder joints
- Saves PCB space
  - Allows for smaller, more dense designs
  - More room for signal routing
  - Functionality – plane integrity

IPDs are the future for decoupling
Resources


