Precision Analog Designs Demand Good PCB Layouts

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Outline

• Enemies of Precision:
  • “Hidden” components
  • Noise
    • Crosstalk
      • Analog-to-Analog
      • Digital-to-Analog
    • EMI/RFI
  • Poor Grounds
  • Thermal Instability
  • Leakage Currents
• Optimize the Signal Chain at the PCB
What is Precise?

• Signal Range Is Critical
  • ±10V Is A 20V Range
    • 16 Bits: 20V/65536 = 305μV Per LSB
    • 24 Bits: 20V/16777216 = 1192nV Per LSB
  • ±2.5V Is A 5V Range
    • 16 Bits: 5V/65536 = 76.3μV Per LSB
    • 24 Bits: 5V/16777216 = 298nV Per LSB
  • ±0.020V Is A 0.040V Range
    • 16 Bits: 0.040V/65536 = 0.610μV Per LSB
    • 24 Bits: 0.040V/16777216 = 2nV Per LSB
Enemy #1: “Hidden” Components

- Resistance
- Inductance
- Capacitance
All Materials have a Finite Resistance

For PCB Trace

\[ R = \frac{\rho Z}{XY} \]

For 1 oz. Copper:

\[ \rho = 1.724 \times 10^{-6} \ \text{\AA} \cdot \text{cm} \quad \text{for} \ Y = 0.0038 \text{cm} \]

\[ R = 0.45 \frac{Z}{X} \ \text{m\AA} = \text{number of “squares”} \]

R = sheet resistance for 1 “square”

\( (Z = X) = 0.45 \text{m\AA}/\text{square} \)

For Wire

\[ R = \frac{0.0219L}{d^2} \]

L in meters

\( d \) in mm
PCB Trace Resistance

- 1 inch (7 mil) trace of 1/2 oz copper with 10μA of current => voltage drop of 1.3μV
- 4 LSBs (298nV) at 24 bits!
PCB Inductance

PCB:

Inductance = 0.0002L \left[ \ln \left( \frac{2L}{W+H} \right) + 0.2235 \left( \frac{W+H}{L} \right) + 0.5 \right] H

Example:

\begin{align*}
L &= 10\text{cm} \\
W &= 0.25\text{mm} \\
H &= 0.038\text{mm}
\end{align*}

This PC track has 141nH of inductance

Wire:

Inductance = 0.0002L \left[ \ln \left( \frac{2L}{2R} \right) - 0.75 \right] H

Example:

\begin{align*}
L &= 10\text{cm} \\
2R &= 0.5\text{mm}
\end{align*}

This wire has 105nH of inductance
PCB Capacitance

- Two Cu plates with PCB material dielectric
  - Two 10 mil traces on a multi layer PCB, 10 mil between layers

\[ A = 0.25 \text{ mm} \times 0.25 \text{ mm} \]

Permittivity of FR4 \( \approx 4.7 \)
\( \Sigma_0 = 8.84 \times 10^{-12} \)

\[
C = \frac{\varepsilon_R \times \varepsilon_O \times A}{t}
\]

\[
C = \frac{(41.9 \times 10^{-12}) A}{t}
\]

\[
C = \frac{(41.9 \times 10^{-12})(0.25 \times 10^{-3})}{0.25 \times 10^{-3}}
\]

\[ C = 0.01 \text{ pF} \]
PCB Vias

Component: Vias

Purpose: Interconnect traces on different layers

Problem: Inductance and Capacitance

\[
L(nH) \approx \frac{h}{5} \left[ 1 + \ln \left( \frac{4h}{d} \right) \right]
\]

\[
C(pF) \approx \frac{0.0555 \varepsilon_r \cdot h \cdot d_1}{d_2 - d_1}
\]

0.4mm (0.0157”) via with 1.6mm (0.063”) thick PCB has \( \approx 1.2 \text{nH} \)

1.6mm (0.063”) Clearance hole around 0.8mm (0.031”) pad on FR-4 has \( \approx 0.4 \text{pF} \)

\( \varepsilon_r = \) PCB material permeability (FR-4 \( \approx 4.5 \))
Bypass Capacitors

- Used in all analog applications
- Used for bypassing (cleaning up) power supplies
- Most op amp applications use two types for the two roles they must fill
Bypass Capacitors

- **DO NOT** have vias between bypass caps and active device – Visualize the high frequency current flow !!!

- Ensure Bypass caps are on same layer as active component for best results.

- Route vias into the bypass caps and then into the active component.

- The more vias the better.

- The wider the traces the better.

- The closer the better
Enemy #2: Noise and Crosstalk

- Noise = anything in your signal that is **not** your signal
- May couple from signals on your board, or
- From signals external to your board
Source of Electromagnetic Energy

RF generating sources

Intentional radiators
- cell phones
- transmitters & transceivers
- wireless routers, peripherals

Unintentional radiators
- System clocks & oscillators
- Processors & logic circuits
- Switching power supplies
- Switching amplifiers (class D)
- Electromechanical devices
- Electrical power line services

Electromagnetic wave representation

\[ f = \frac{1}{t} \text{ (per cycle)} \]
How radio frequency energy comes about in circuitry

\[ |X(f)| = \sqrt{\text{Re}(f)^2 + \text{Im}(f)^2} \]

Complex frequency domain in Polar form

\[ \sin x \quad x \]

Voltage (V) vs. Time (s) graph showing a 20ns pulse.

Amplitude [V/Hz] vs. Frequency (Hz) graph showing peaks at \(1/T_0, 2/T_0, 3/T_0, 4/T_0\).
Coupling Medium: Conducted Emissions
Coupling Medium: Radiated Emissions
Radiated Noise: Long Traces

• Trace going into 10-bit or 12-bit ADC input is longer than a few inches
Analog receptors: electromagnetic energy

Op-amps
Low-speed: offset shift, RF noise
High-speed: linear and non-linear amplification

Converters
EMI aliased into passband
offset shift

Regulators
offset shift in output voltage

EMI Source

load

A/D

REG

101010111...

load
Loops

- Introduces unintended inductance in the current path where: \( V_L = L \frac{di}{dt} \)
- May result in multiple AC signals sharing a current path
- May become a loop antenna that couples EMI/RFI

The common-mode return loop may be difficult to predict
Traces That Form a Loop

- Signal Path
- Ground
Loop Area Influences Inductance

Figure 1 Each loop of wire is the same length, yet they each have inductances, from left to right, of 730, 530, 330, and 190 nH.

Figure 2 Magnetic fields from the outgoing current (red) nearly cancel the equal-but-opposite magnetic fields from the returning signal current.

EDN, May 24, 2007. Howard Johnson, PhD
The ground return environment may be very complex

Current paths must be carefully considered to avoid long loops
PCB Capacitance: E-Field

\[ C = \frac{w \cdot L \cdot e_0 \cdot e_r}{d} \text{ pF} \]

\[ I = C \frac{dV}{dt} \text{ amps} \]

\( w = \text{thickness of PCB trace} \)
\( L = \text{length of PCB trace} \)
\( d = \text{distance between the two PCB traces} \)
\( e_0 = \text{dielectric constant of air} = 8.85 \times 10^{-12} \text{ F/m} \)
\( e_r = \text{dielectric constant of substrate coating relative to air} \)
PCB Capacitive Coupling

$\text{Voltage IN}$

$\text{PCB Trace}$

$\text{Coupled Current}$

$I = C \frac{dV}{dt} \text{ (amps)}$
Capacitive Cross-Talk Coupling by electric fields

- Coupling looks like high pass filter
- Cross-talk increases with increasing $Z$
- Voltages responsible for coupling
- Signals are in phase
PCB Coupling Noise Reduction

- Decrease “L” or Increase “d”
- Put Ground Guard Between Traces

\[ C = \frac{w \cdot L \cdot e_0 \cdot e_r}{d} \text{ pF} \]

\[ I = C \frac{dV}{dt} \text{ (amps)} \]
Inductive Cross-Talk
Coupling by magnetic fields

- Coupling looks like high pass filter
- Cross-talk increases with decreasing $Z$
- Changes in current are responsible for the coupling
- Signals are out of phase
Decrease Inductive Cross-Talk

- Increase the distance ($R_X$) between two circuits
- Twist the wires of the two circuits to counteract their fields
Balance helps limit CM EMI response

Balance helps prevent common-mode EMI from being converted to differential-mode EMI

Differential or odd mode

Common or even mode

Balanced Line

PC board

Zcm1 = Zcm2
Balanced analog and digital circuit
(common-mode signals not welcome!)

Balanced digital logic: LVDS, PECL, HSTL

Balanced differential analog circuitry

Balanced traces over GND

Balanced traces over GND

Balanced traces over GND

Balanced traces over GND
Circuit techniques to minimize EMI

- Strive for a zero impedance ground
- Design for a differential signal environment, both logic and analog
- Minimize PCB loops that act as EMI antennas
- Use X2Y capacitors for filtering and decoupling
- Make use of common-mode transformers
- Use balanced lines and traces
Enemy #3: Poor Grounds

• A good grounding scheme helps reduce the values of the “hidden” components.
• The key to good ground plane design is managing return currents
• Requires good floorplanning first.
Component Placement
Single Point Grounding

Series

- Simple wiring
- Common impedance causes different potentials
- High impedance at high frequency (>10 kHz)

Parallel

- Complicated wiring
- Low differential potentials at low frequencies
- High impedance at high frequency (>10 kHz)
Multi Point Grounding

- Ground plane provides low impedance between circuits to minimize potential differences
- Also, reduces inductance of circuit traces
- Goal is to contain high frequency currents in individual circuits and keep out of ground plane
Current Density

\[ i(A/cm) = \frac{I_o}{\pi h} \times \frac{1}{1 + \left( \frac{D}{h} \right)^2} \]

- \( I_o \) = total signal current (A)
- \( h \) = height of trace (cm)
- \( D \) = distance from trace (cm)

- Illustrates Return Current Flow is directly below the signal trace. This creates the path of least impedance.
- Must have Solid return path (i.e. Solid Ground Plane) under the signal trace to maintain homogeneous nature of current density.
Slots in Ground Plane
Return Current Paths
Taking a Look at Vias

- Must have Return Path Vias next to Signal Path Vias.
- Notice Large Current Density Area flow in return path.
- Will have a change in impedance with this configuration.

2-Layer PCB showing Current Density of PCB trace and Single Return Path Via.
Controlled Impedance Vias

- Better Solution is to add Multiple Return Path Vias.
- Notice minimal Current Density Area Flow at vias.
- Improved impedance – reduces reflections.

2-Layer PCB showing Current Density of PCB trace and Multiple Return Path Vias.
Split Grounds

Analog Ground

A/D

AGND DGND

Digital Ground

Power Supply
Split Ground Connected Under ADC
Connecting Both to Analog Ground
Ground Plane overlap
ADS1232REF Layout: Bottom
Enemy #4: Thermal Instability

• Component placement
• Parasitic Thermocouples
In-circuit Thermocouples
Thermal Considerations

• A temperature differential with any two metals will create a thermocouple
• This includes PCB feedthroughs
  • A different number of feedthroughs for both sides of a differential signal will create an offset that varies with temperature.
Enemy #5: Leakage Paths

• Most critical when measuring small currents
  • Photodiode sensors
  • High-impedance sensors (pH, etc).
• Come from layout as well as contamination of the board or IC packaging
Guard Rings-Circuit

(A) Non-Inverting

(B) Buffer

(C) Inverting

Guard top and bottom of board.
Guard Rings - PCB

Connect to proper circuit node, depending on circuit configuration (see Figure 2).

(A) DIP package

Connect to proper circuit node, depending on circuit configuration (see Figure 2).

OPA129
Summary

- Optimize the Signal Chain at the PCB
- Take steps to minimize:
  - “Hidden” components
  - Noise
    - Crosstalk
      - Analog-to-Analog
      - Digital-to-Analog
    - EMI/RFI
  - Poor Grounds
  - Thermal Instability
  - Leakage Currents
References

- Kuehl, T., “Tackling EMI and RFI at the Board and System Level”, Texas Instruments