DesignCon 2009
PCB Power Delivery Optimizations for the Cost Driven Era

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The Power Deliver Problem

- Support DC current requirements of each IC
- Support AC current requirements of each IC
- Sufficiently suppress AC noise between separate IC power nodes and ICs
- Support I/O return path impedance requirements
- Meet emissions and susceptibility requirements
Divide and Conquer

• Divide the problem between what is on the PCB and the requirements and parasitics of each IC
• Results in impedance budget for each IC at the PCB attach
What We Can Control On the PCB

- PCB stack-up
- PCB laminate selection
- Bypass capacitor selection
- Bypass network design
- Choices interact
Power Plane Behavior

- Power plane cavities exhibit two distinct behaviors:
  - Distributed impedance
    - How the cavity appears to many loads distributed over the cavity X-Y extents
    - Very low inductance, modest value capacitor
    - Thin cavities increase capacitance
  - Local impedance
    - How the cavity appears to any given load
    - Series R-L out to bypass caps & VRM
    - Thin cavities decrease inductance
Plane Cavity R / L

• In the X-Y plane, spreading resistance and inductance both scale identically
  – Simulation computations can be greatly reduced by solving first as just an R-mesh, and then reducing the result to a matrix or RLCs between IC and capacitor attachment nodes and then solving complex Z vs Freq

• Changing the size / shape of a polygon changes |Z| but not phase
Cavity Height and Complex Z

- R/L behavior depends on:
  - Conductor bulk resistance,
  - Skin effect,
  - Conductor relative permeability, 1.0 for copper
  - Cavity dielectric height
- Reflected as phase response of interconnect alone
Cavity Height and Complex Z

- Thick cavities exhibit almost no local skin effect
- Local power connections inductive from 73kHz 2oz, 138kHz 1oz
- Z phase 2oz crosses 45 deg 0.53F of 1oz
  - W/o skin effect w/b 0.50F
Cavity Height and Complex Z

- Cavity transition to inductive response occurs:
  - <150kHz for 48mil 1oz
  - <3MHz for 4mil 1oz
  - <15MHz for 1mil 1oz
  - Skin effect apparent

- Three key parameters are:
  - INDUCTANCE, and INDUCTANCE, and INDUCTANCE
PDN as Collection of Local PDNs

- Good approximation that handles worst case-
  - All ICs draw $I_{\text{AC,MAX}}$ in phase
- Approximation becomes increasingly accurate for thick cavities
  - Spreading $|Z|$ isolates non-local bypass
- Effective divide and conquer
  - Second pass optimization *may* reduce final requirements
PDN as Collection of Local PDNs

- Solve PDN for each IC first
- Adjust for full optimization second
  - Useful tools: Optimize PI™, Hyperlinx™, SI-Wave™
- Adjust for resonances and EMI hot-spots third
2 Routing Layer Constructions

- 4 layer, thick power cavity traditional
  - Very high impedance cavity
    - Typical 300pH $L_{\text{SPREAD}}$ to IC power
  - Peripheral bypass caps below 300pH little effect
  - < 300pH Relies on enough power / gnd pairs directly under IC to bottom of PCB and caps to match
2 Routing Layer Constructions

• Add thin power cavity to center?
  – IC Z axis L improves 2:1
  – Caps can go top or bottom
• Total Z axis still very high for caps and IC
2 Routing Layer Constructions

- Add thin power cavities to outside
  - IC Z axis very low
  - Cap attach very low
  - L/R spreading very low

- Bottom cavity natural puddle, or add’l route (4mil), or combination
4 Routing Layer Constructions

- Traditional 6 layer same as 4 layer
  - For Tx line return purposes 2 PCBs, top and bottom
- 8 layer constructions very different than 6 layer
  - IC Z axis drops
  - 2 power cavities
    - Can puddle bottom

4 Signal Layer Constructions

- 6 Layer: One FR406 Power Cavity
- 8 Layer: Two FR406 Power Cavities
- 8 Layer: Two HK04 Cavities
Caps Req’d Versus L

- Caps peripheral to IC using thick cavities:
  - Poor effectiveness
- Caps under IC
  - Works adequately if IC mfg provides enough pwr/gnd via pairs
  - If not 4 layer design won’t work
Caps Req’d Versus L

- Caps peripheral to IC using thin cavities:
  - Can eliminate many caps
  - How many depends on target L, cavity thickness
  - Only works down to $L_{\text{SAT}}$

![Inductance Bypass Network to IC Power Cavity Attach](image)

<table>
<thead>
<tr>
<th>Capacitor Type</th>
<th>$L_{\text{SAT}}$</th>
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</thead>
<tbody>
<tr>
<td>0402 X2Y</td>
<td>6</td>
</tr>
<tr>
<td>4 layer, 50 mil center</td>
<td>625pH</td>
</tr>
<tr>
<td>6 layer, 4 mil center</td>
<td>50pH</td>
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<tr>
<td>6 layer, 4 mil top</td>
<td>50pH</td>
</tr>
<tr>
<td>6 layer, 1 mil top</td>
<td>13pH</td>
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</tbody>
</table>

Figure 1, Inductance Saturation Capacitor Counts, Typical
## Caps Req'd vs \( L_{\text{TGT}} \)

### 2 / 4 Routing Layer PCBs

<table>
<thead>
<tr>
<th>Target Inductance</th>
<th>0402</th>
<th></th>
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<th></th>
<th>X2Y™</th>
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<tbody>
<tr>
<td></td>
<td>4/6 Layer</td>
<td>6/8 Layer</td>
<td>6/8 Layer</td>
<td>6/8 Layer</td>
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<tr>
<td></td>
<td>Bottom Caps</td>
<td>4mil</td>
<td>1mil</td>
<td>4mil</td>
<td>1mil</td>
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<tr>
<td>5pH</td>
<td>363</td>
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<td>No Solution</td>
<td>No Solution</td>
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<tr>
<td>10pH</td>
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<td>No Solution</td>
<td>136</td>
<td>No Solution</td>
<td>37</td>
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<tr>
<td>20pH</td>
<td>91</td>
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<td>37</td>
<td>No Solution</td>
<td>10</td>
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<td>102</td>
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<tr>
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<tr>
<td>60pH</td>
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<td>4</td>
<td>3</td>
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<td>70pH</td>
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<td>11</td>
<td>8</td>
<td>3</td>
<td>2</td>
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<tr>
<td>80pH</td>
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<td>2</td>
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<tr>
<td>100pH</td>
<td>19</td>
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<td>5</td>
<td>2</td>
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<tr>
<td>120pH</td>
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<td>1</td>
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<td>220pH</td>
<td>9</td>
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<td>2</td>
<td>1</td>
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</tbody>
</table>

### Capacitor Counts vs. Inductance to IC Attach 0.062" PCB

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Caps Req’d vs $L_{TGT}$

2 / 4 Routing Layer PCBs

- At modest $L_{TGT}$:
  - $90\,\text{pH} < L_{TGT} < 300\,\text{pH}$
  - 4mil, 1mil drops caps $\approx 3:1, 4:1$ versus 50/42mil
- More demanding $L_{TGT}$ more advantage to 1mil versus 4mil cavities
- Combination of 1mil and X2Y® 10:1 cap reduction from 200pH down to 20pH $L_{TGT}$
  - 200pH 63mOhms @ 50MHz
  - 20pH 6.3mOhms @ 50MHz

<table>
<thead>
<tr>
<th>Target Inductance</th>
<th>0402</th>
<th>6/8 Layer</th>
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<tbody>
<tr>
<td></td>
<td>4/6 Layer</td>
<td>6/8 Layer</td>
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<tr>
<td></td>
<td>Bottom Caps</td>
<td>4mil</td>
</tr>
<tr>
<td>5pH</td>
<td>363</td>
<td>No Solution</td>
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<tr>
<td>10pH</td>
<td>182</td>
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<td>200pH</td>
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</tr>
<tr>
<td>220pH</td>
<td>9</td>
<td>3</td>
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Evaluating Costs

• Evaluation comes down to the big three:
  – PCB material cost
  – Bypass caps, BOM cost
  – Bypass caps, placement cost

• Conventional bypass caps are almost free
  – $0.001 typical in high volume

• Assembly placement cost is the critical parameter for both more and/or better PCB materials and/or better caps
Evaluating Costs

- At current prices, break-even on 4/6 layer alternatives occurs near $0.01 / comp placement
  - Why?
    - **Adding 1 layer of FR406 adds $2.00/sq ft / $0.014 / sq”**
      - Save 1.3 caps / sq” pays back - $2.00 / (144 * $0.011)
    - **Changing 2 layers of FR406 to HK04 adds $6.00/sq ft**
      - Save 3.8 caps / sq” pays back - $6.00 / (144 * $0.011)
    - **X2Y™ replaces caps ≈ 4:1**
      - $0.03 comp + $0.01 place ≈ $0.004 comp + $0.04 place

- Key drivers:
  - Performance targets and
  - Assembly cost
Example Cases

- 4” x 8” PCB
- Ten IC’s 70pH $L_{TGT}$
  - 22mOhms @ 50MHz
- 2 routing layers
- $2.00/sq ft FR406 / layer pair
- $5.00/sq ft HK04™ / layer pair
- $0.001 / cap 0402
- $0.03 / cap X2Y™
- $0.015 / cap assy

<table>
<thead>
<tr>
<th>Costs</th>
<th>0402</th>
<th>X2Y</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>4 lyr</td>
<td>6 lyr</td>
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<td></td>
<td>Bottom</td>
<td>4 mil top</td>
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<td>PCB</td>
<td>$0.89</td>
<td>$1.33</td>
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<tr>
<td>Capacitors req’d</td>
<td>260</td>
<td>110</td>
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<tr>
<td>Cap. mat’l</td>
<td>$0.26</td>
<td>$1.10</td>
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<tr>
<td>Cap. assy</td>
<td>$3.45</td>
<td>$1.65</td>
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<tr>
<td>Total</td>
<td>$4.57</td>
<td>$4.07</td>
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</table>

Table 1, Example Two Signal Routing Layer Costs
Example Cases

- 4” x 8” PCB
- 4 routing layers
- 12 ICs 50pH $L_{TGT}$
  - 15mOhms @ 50MHz
- $2.00/sq ft FR406 / layer pair
- $5.00/sq ft HK04™ / layer pair
- $0.001 / cap 0402
- $0.03 / cap X2Y™
- $0.015 / cap assy

<table>
<thead>
<tr>
<th>Costs</th>
<th>0402</th>
<th>X2Y</th>
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</thead>
<tbody>
<tr>
<td></td>
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<td>8 lyr</td>
</tr>
<tr>
<td></td>
<td>6 lyr</td>
<td>4 mil top</td>
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<td>PCB</td>
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<td>Cap. mat’l</td>
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<td>Cap. assy</td>
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<tr>
<td>Total</td>
<td>$8.44</td>
<td>$5.62</td>
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</table>

Table 1, Example Four Signal Routing Layer Costs
Conclusions

- Power distribution focus is managing inductance
- PCBs are locally inductive from low frequencies
  - Transition frequency independent of plane shape
  - Inductance proportional to thickness
- Thinner dielectric allows more inductance in bypass cap network, IE fewer caps
- In many low-cost constructions, total manufactured cost can be minimized through use of:
  - More material – take 4 to 6 layer, or 6 to 8 layer w/ glass / resin cavities
  - More expensive raw materials – using 1 mil polyimide (DuPont Interra HK04®), or epoxy (Oak/Mitsui BC24®) dielectric in place of 4 mil glass / resin
  - Lower inductance capacitors such as X2Y™
- Thinner cavities offer other performance benefits, but here we are concerned only with cost and presume function can be realized w/thick cavities
- Actual results depend on IC L_{TGT} and assembly cost per capacitor
  - Know your requirements!
  - Know your costs!
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