Understanding Capacitor Inductance and Measurement in Power Bypass Applications

Summary

Power supply bypass is a critical function in all electronics. High frequency capacitor performance depends on the mounted inductance of the bypass capacitor network. The number of capacitors needed to reach a given performance target is directly proportional to the mounted inductance of each individual capacitor. The total number of vias needed is proportional to device inductance multiplied the number of vias that attach each part.

When mounted with well-designed attachment vias, X2Y® capacitors often replace four or five times as many conventional capacitors. Because X2Y® capacitors utilize vias more efficiently than conventional capacitors; X2Y® capacitors often reduce the total bypass capacitor via count anywhere from 30-60%.

This paper explains the elements of capacitor inductance, and how to accurately characterize bypass capacitors for power supply bypass applications.

Introduction

Bypass capacitors[1] support power supply voltage at medium to high frequencies: from a low-frequency cut-off with the voltage regulator module (100kHz to 1MHz typical), to a high frequency cut-off with the PCB planes, (several hundred MHz typical).

Within their range of operation, ceramic capacitors exhibit a well-known "V" shaped response curve. Capacitance dominates impedance at frequencies below the series resonance of the **mounted** part. Around series resonance, the capacitor ESR sets the minimum impedance, while above the series resonance, the **mounted inductance** sets device impedance.

The mounted capacitor inductance sets both the SRF, and the device performance above the SRF. The mounted inductance of a single capacitor sets the number of capacitors needed to hit a given impedance target up to the high frequency transition to the PCB planes. Similarly, the mounted inductance multiplied by the number of vias used by each capacitor determines the total number of vias in the bypass network. X2Y® capacitors excel both in mounted inductance and superior (lower) mounted ESL * via count products. These facts are born out through carefully designed and verified device and application characterization fixtures.

Simply put, proper application of X2Y® capacitors results in a bypass network with both the fewest total capacitors, and fewest vias compared to any other capacitor in the market today.

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[1] Bypass capacitors are so named as over the frequency range that they are effective, most load current diverts through the capacitors, bypassing the rest of the power system.

Bypass Capacitor Behavior

To a reasonable approximation, bypass capacitors may be modeled as three significant elements all in series: device capacitance, effective series resistance, ESR, and **mounted** effective series inductance, ESL. At all frequencies we are concerned with the parameter that limits the capacitors' ability to shunt current. At high frequency, barring very small capacitance values, it is the ESL that defines (limits) bypass performance. This can be readily understood by first modeling capacitors with zero ESL, as shown by the blue RC Response curve in Figure 1.
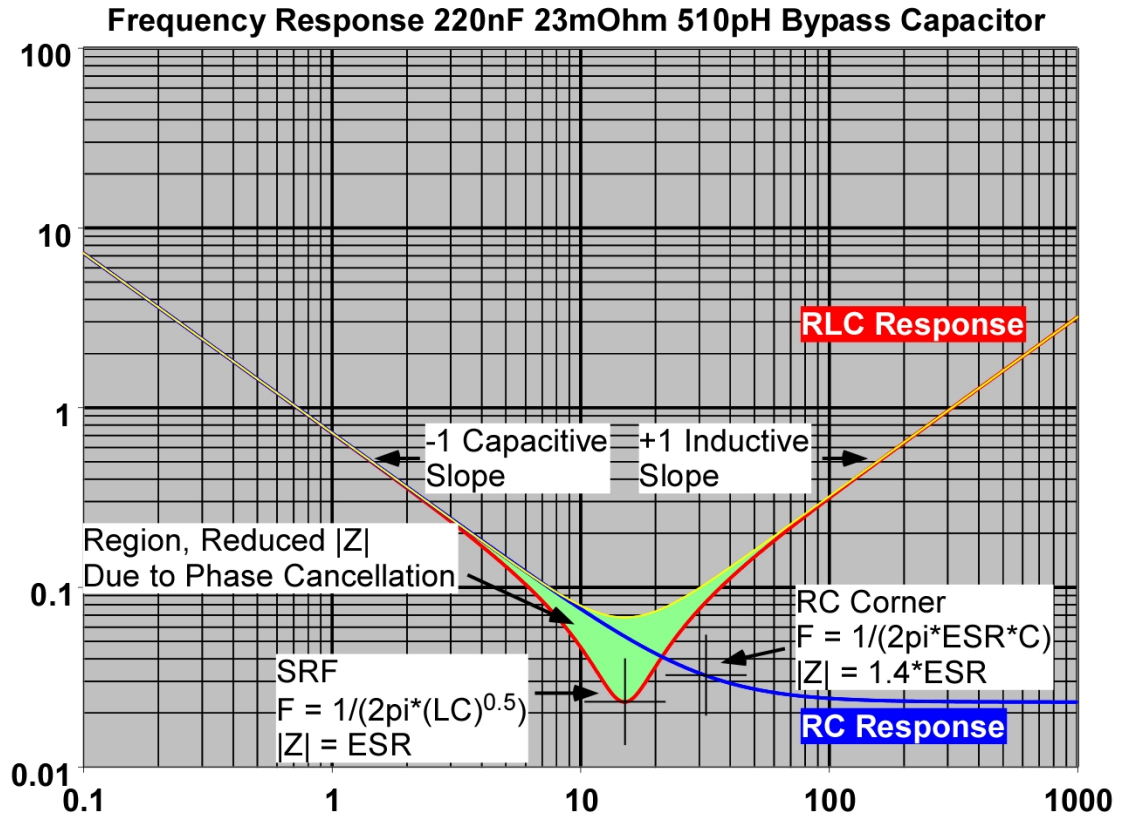
Frequency Response 220nF 23mOhm 510pH Bypass Capacitor

Figure 1, Bypass Capacitor Impedance vs. Frequency, MHz

As Figure 1 shows, capacitance dominates impedance below the RC corner, as 1/jwC, while the ESR sets the impedance above the corner. More capacitance shifts the corner frequency down. It does not reduce impedance beyond the corner. We can scale impedance above the corner down only by paralleling more components, or finding components with a lower ESR.

Now, let's turn our attention to the effects of ESL. Changes in current induce counter EMFs that oppose the respective current change. For a given peak-to-peak current, the rate of change, and therefore the opposition to current flow, is proportional to frequency. Whereas capacitive reactance decreases with frequency, inductive reactance increases.

Capacitive current leads signal voltage by 90 degrees, while inductive current lags by 90 degrees. When the magnitudes are similar, the net reactance falls quickly. The point where the magnitudes match and completely cancel is the capacitor series resonant frequency, SRF.   At the SRF, capacitor impedance is its minimum, equal to the device ESR, also shown in Figure 1. Above the SRF, the capacitive reactance continues to fall, and the inductive reactance continues to rise. Phase cancellation quickly diminishes until the capacitor impedance appears almost completely inductive.

Even though the capacitor behavior is inductive above the SRF, the capacitor still presents a shunt across the power system, lowering impedance by diverting current away from the rest of the power system. Because the impedance is inductive, the amount of current each capacitor diverts diminishes with rising frequency.

To illustrate, we show the same capacitor from Figure 1, but raise the ESR to 1.6 Ohms as shown in Figure 2. We may parallel some number of these high capacitors in order to hit desired system impedance over the broad frequency range 500kHz to 500MHz.

The green trace plots capacitor response from Figure 1. The low ESR capacitor impedance remains everywhere equal or below that of the high ESR capacitor. Since, the high ESR capacitor remains effective diverting current over this broad frequency range, we must similarly conclude that the low ESR capacitor is at least as effective over the same frequency range. **Bypass capacitors remain effective even in the inductive region above the SRF.**

What limits the frequency range at which the capacitors remain **significant** is the amount of plane capacitance in the plane cavity to which the capacitors attach, the inductance of each attached capacitor, and the spatial density of the capacitors. At a sufficiently high frequency, the inductive reactance of the bypass capacitor network crosses the magnitude of the capacitive reactance of the power / ground plane cavity the network attaches to. Beyond the discrete bypass network to power cavity crossover frequency, load currents divert mostly through the plane cavity impedance.[2]

The crossover frequency is a function of the plane cavity height, dielectric, mounted inductance of each bypass capacitor, and the average density of bypass capacitors attached to the PWB.

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[2] This simplistic model ignores the impedance loading effects of ICs with substantial die and/or in-package capacitors.

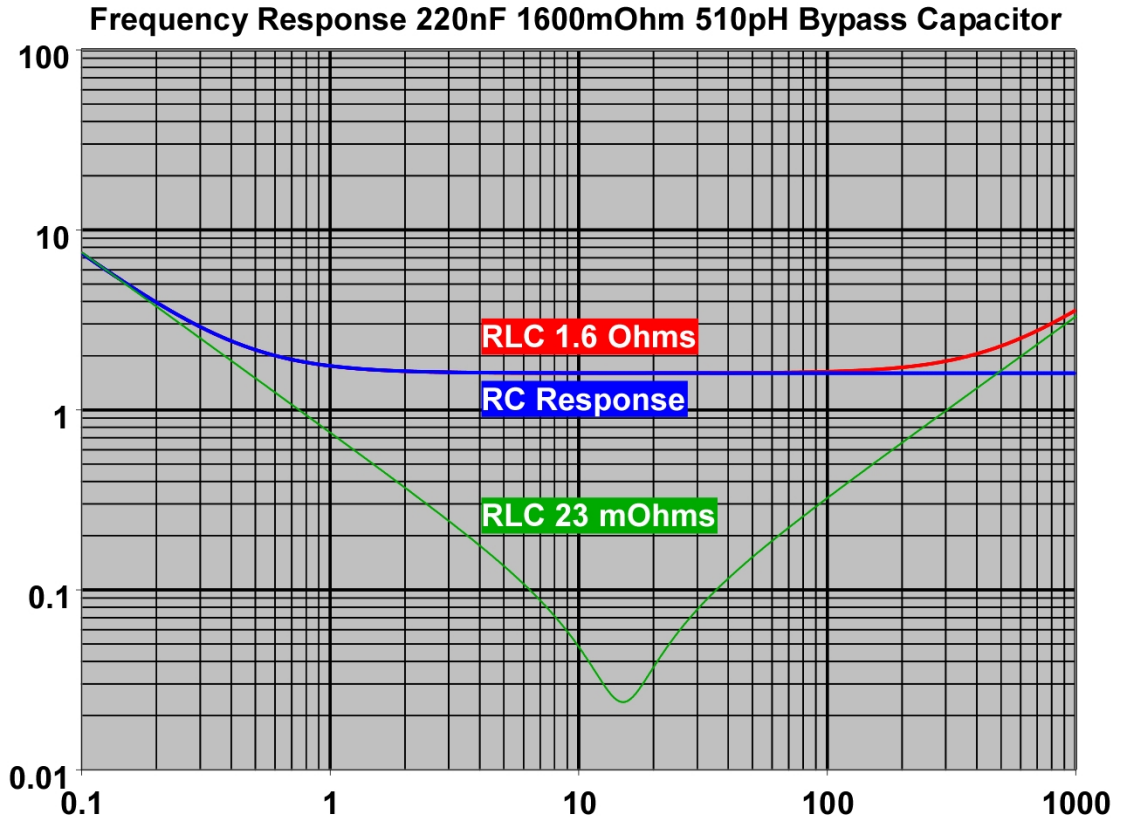**Frequency Response 220nF 1600mOhm 510pH Bypass Capacitor**

Figure 2, Bypass Capacitor Impedance vs. Frequency, MHz, High ESR

Mounted Inductance

Inductance always evaluates around a loop. Bypass capacitor mounted inductance is a function of the **entire physical path(s)** from the IC load(s) attached to the power planes, through the power / ground plane cavity to the bypass capacitor attachment vias, through those vias to the PCB surface, through the PCB surface features and through the bypass capacitor. Complicating this behavior is the fact that skin effect causes bypass capacitor height to effectively shrink at high frequencies.[1] While this characteristic is desirable from a performance perspective, it complicates modeling.
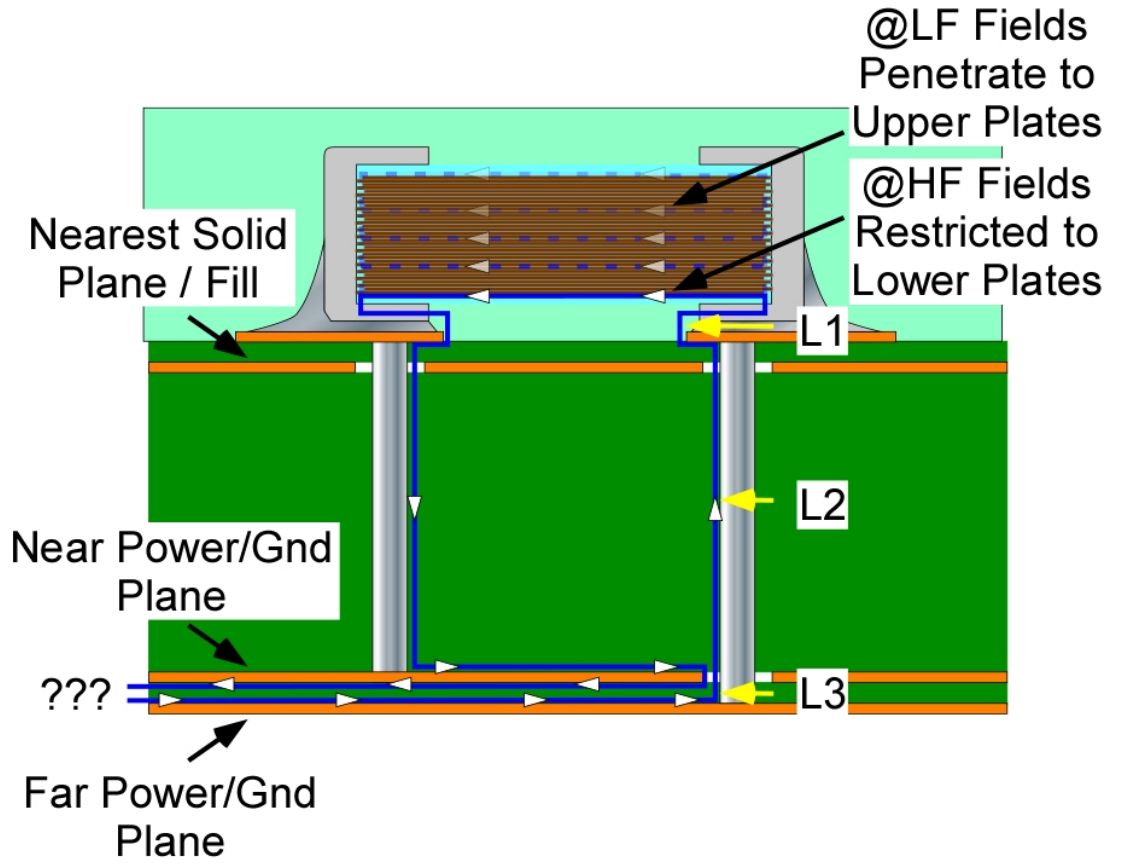
Mounted Bypass Capacitor Induction Loop

Figure 3, Bypass Capacitor Induction Loop

As should be apparent from Figure 3, the complete loop is indefinite until we define the location of the IC power / ground pins and the IC(s) itself. In order to analyze performance, we short the planes shown dividing the entire loop into three distinct induction loops in series by shorting the vias to the near power / ground plane, and the near surface plane / fill area:
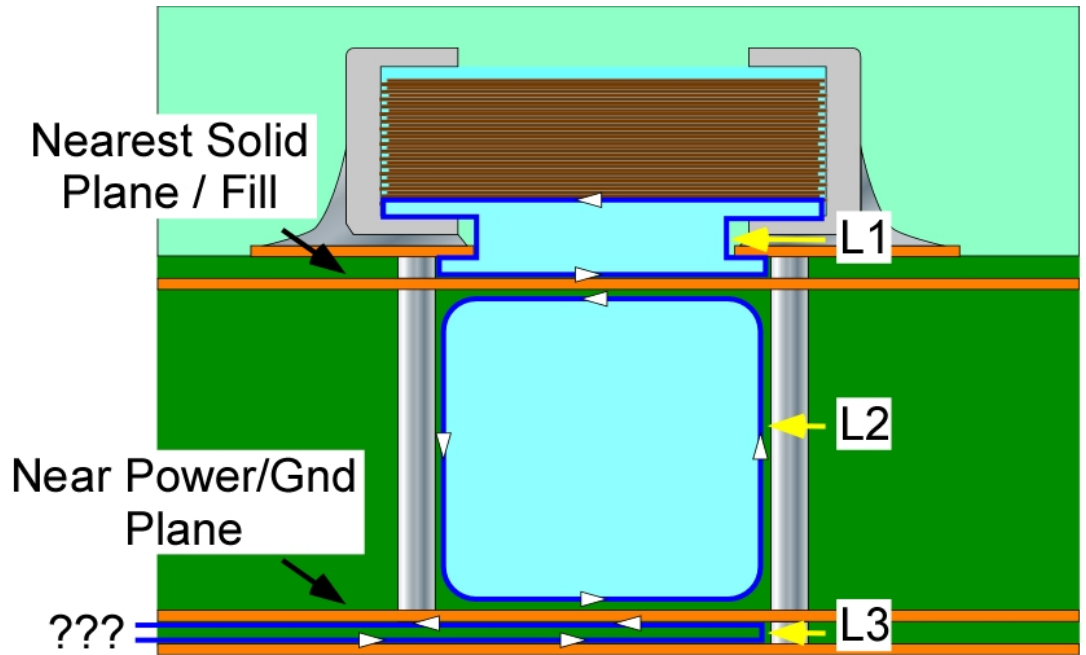
Bypass Capacitor Induction Loop Components

Figure 4, Bypass Capacitor Induction Loop As Three Series Loops

The nearest solid plane / fill, and the near power / gnd plane, act as the top and bottom surfaces of a Faraday cage. Above the skin cut-off frequency, (about 4MHz for 1oz planes, 16MHz for 1/2oz planes), these planes block field penetration, and therefore coupling, between the sections marked L1, L2, and L3. The DC potential on these planes has nothing to do with their shielding properties. Only plane thickness and perforation determine shielding properties.

The three distinct regions are:

- Loop above the nearest plane, L1

- Loop from the nearest plane to the near attached pwr / gnd plane, L2

- Loop(s) within the power / ground cavity to the serviced ICs, L3

L2 only appears on many layer boards where the bypass capacitor supports a power plane cavity buried further into the stack than the plane / fill area nearest the capacitor surface.

Loop Above the Top Cavity, L1

Above the uppermost plane or fill area is geometrically complex and inductance depends on a myriad of factors. Some of these factors are under the capacitor manufacturer's control and others are under the board engineer's control. Variables that affect the total inductance of this loop include[2]:

- Capacitor geometry

- Capacitor Terminal configuration

- Capacitor land pattern design

- Attachment via locations

- Attachment via geometry

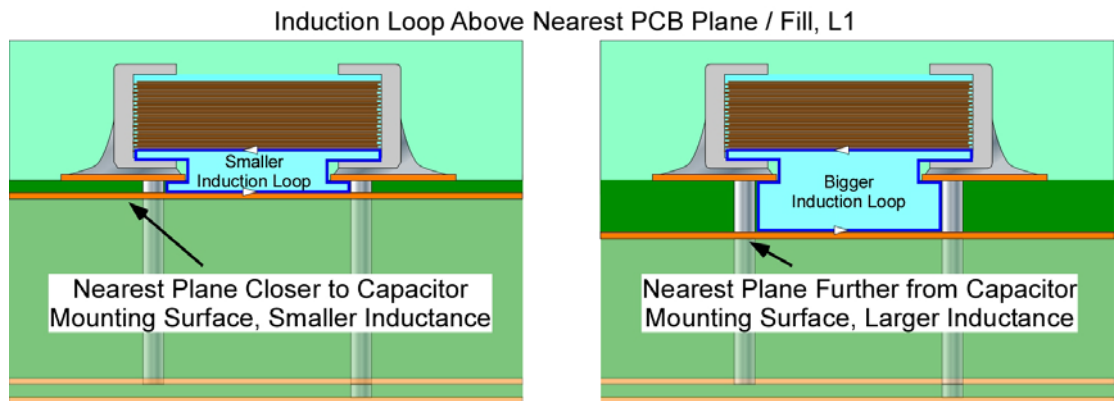- Dielectric height to nearest solid plane / fill area

Induction Loop Above Nearest PCB Plane / Fill, L1

Figure 5, Bypass Capacitor Induction Path Above Uppermost Plane

Given so many variables that are application dependent, how do capacitor manufacturers obtain data sheet ESL values? The answer is that they first measure a reference value on a fixture with a shorting plate in place of the DUT[3]. Then, they measure with a DUT, typically held to the surface under compression. Manufacturers report the measured difference as data sheet ESL.

It should be apparent that this measurement reports only the incremental inductance of the capacitor body over a shorted plate. It does not report the inductance of a capacitor in any application. As such, these values are useful primarily for qualitative comparison between like geometry and terminal configuration capacitors. In order to predict bypass capacitor performance in actual applications, we need to determine the inductance of the entire loop depicted in Figure 5.

In-Cavity Loop, L2

The loop formed between the plane nearest the capacitor mounting surface, and the actual power plane **cavity** that the capacitor supports has an inductance that is almost completely controlled by the vias that traverse it. In situations where the power planes are located far from the capacitor surface, the in-cavity loop accounts for most of the mounted capacitor inductance.
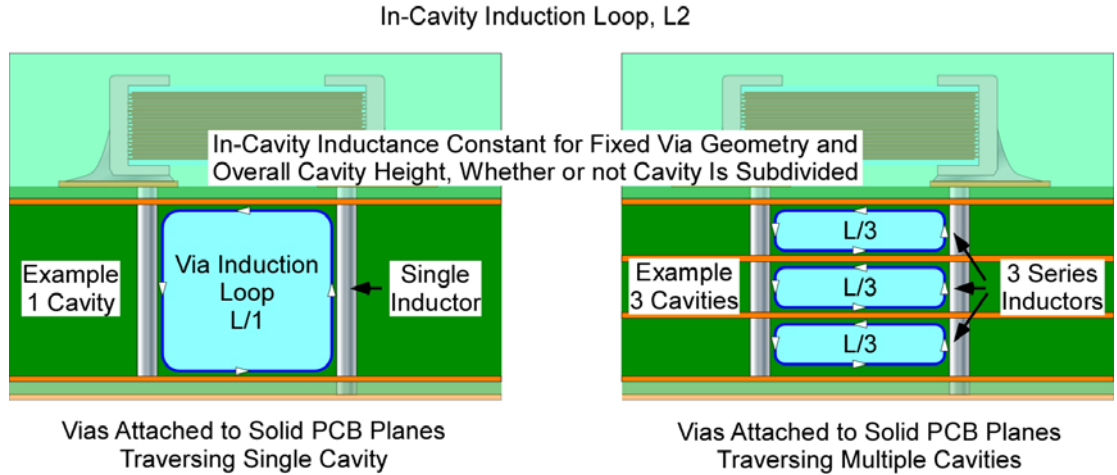
In-Cavity Induction Loop, L2

In-Cavity Inductance Constant for Fixed Via Geometry and Overall Cavity Height, Whether or not Cavity Is Subdivided

Example 1 Cavity

Via Induction Loop L/1

Single Inductor

Vias Attached to Solid PCB Planes Traversing Single Cavity

Example 3 Cavities

L/3
L/3
L/3

3 Series Inductors

Vias Attached to Solid PCB Planes Traversing Multiple Cavities

Figure 6, In-Cavity Induction Loop, L2

This second induction path is defined entirely by via geometry and overall cavity height. Whether vias traverse a single or multiple cavities, the total inductance in this region is fixed by the via geometry and total cavity height. When intervening planes divide the area, each smaller cavity composes a correspondingly smaller inductor that adds in series with the inductances of the remaining cavities to essentially the same total value as the single cavity case.

Since via array geometry determines loop in-cavity inductance, one might believe that the capacitor design does not influence this inductance. This is a fallacy. The capacitor terminal configuration determines where the board designer can readily place vias and therefore the **achievable in-cavity inductance**.

X2Y® capacitors are unique in that the orthogonal terminations facilitate vias arranged on a nearly perfect circle. This geometry enables nearly optimum via utilization, and in-cavity inductance for a given number of vias.
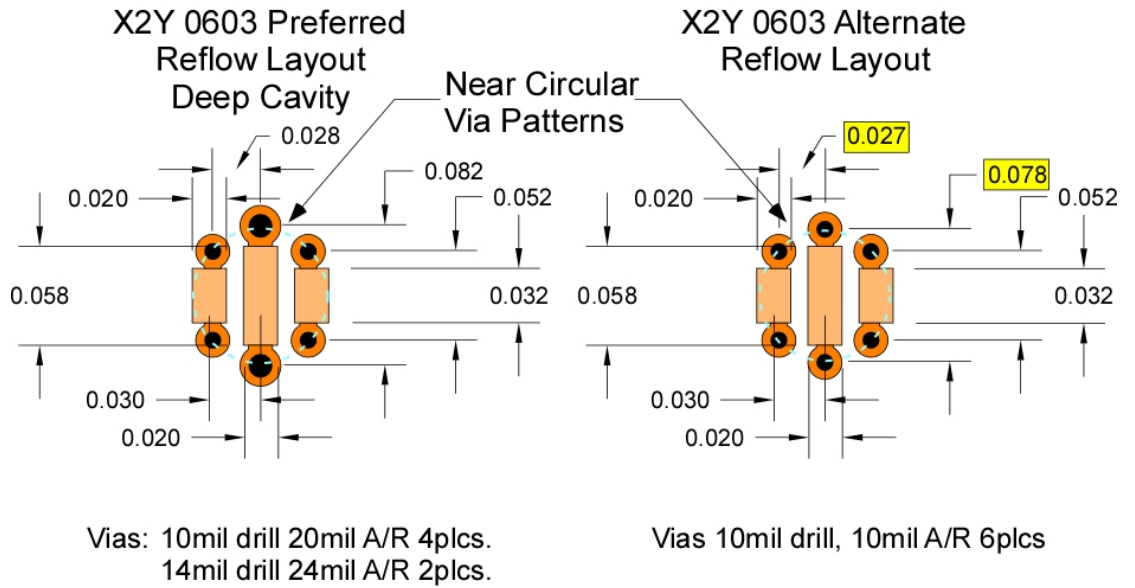
Figure 7, X2Y® 0603 Recommended Reflow Layouts

A good PCB layout optimizes via placements for the capacitor used and realizes superior performance. X2Y® recommended layouts have been designed for high performance and good manufacturability. Poor PCB layouts squander performance, requiring more capacitors, and more vias to do the same job. Figure 8, compares the X2Y® recommended alternate layout against a poor layout. Because of its long extents from device terminals to vias, and the wide via separation, the poor layout shown performs badly. It exhibits approximately 200% L1 inductance, and 150% L2 inductance compared to recommended X2Y® layouts.
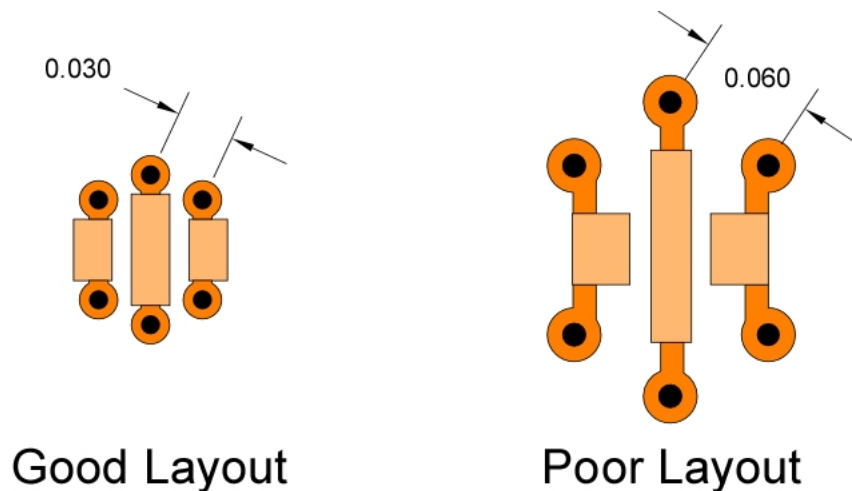

Figure 8, Comparative Layouts, X2Y 0603

Plane Cavity Loop, L3

The last induction path occurs in the power cavity that the capacitor supports. **Cavity height and via geometry define only part of the total loop.** The planar path to IC power connections defines the remainder of the loop. Note that in the model, only the vias from the far plane short the cavity.

Only Via(s) From Far Plane Short Cavity
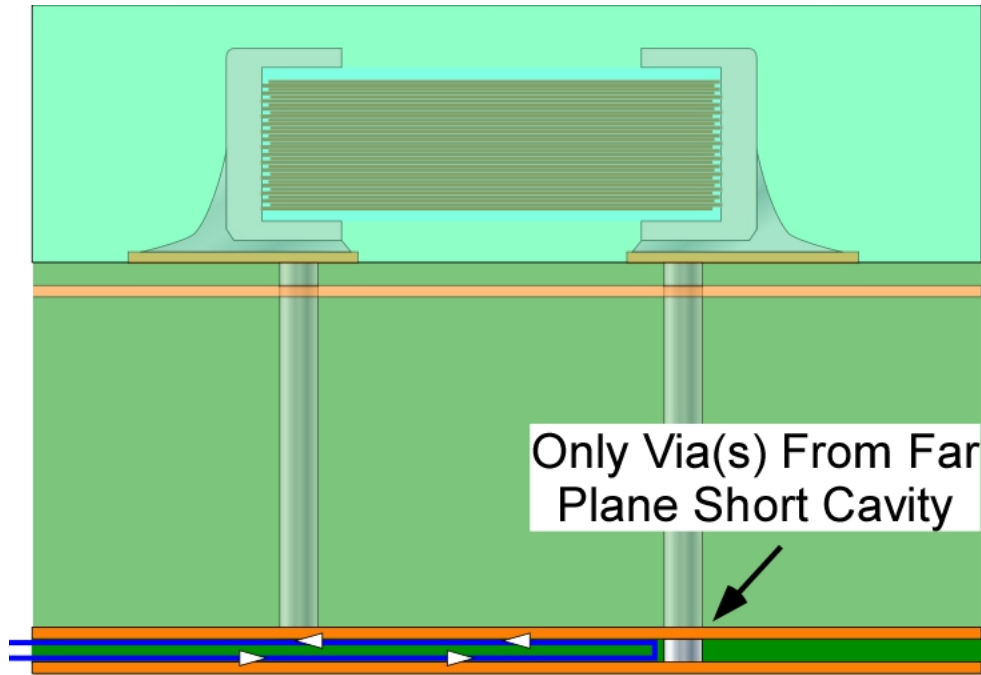
Vias Attached to Solid PCB Planes
Forming Power Cavity

Figure 9, Power Cavity Induction Loop, Single Bypass Capacitor

Measuring L1 Inductance, X2Y® Capacitor Characterization Test Fixture

In order to obtain the highest accuracy results for bypass applications, X2Y® commissioned Teraspeed® Consulting, and Dr. Howard Johnson of Signal Consulting to jointly develop a state of the art bypass capacitor test fixture. This fixture is featured in "Bypass Capacitor Inductance, Data Sheet Simplicity to Practical Reality", Weir TF7, DesignCon East 2005, as well as the Signal Consulting video "Low Inductance Capacitor Packages".

The fixture is designed to accurately characterize bypass capacitors from 10nF and 0201 case sizes up to many uF's in 1812 cases.
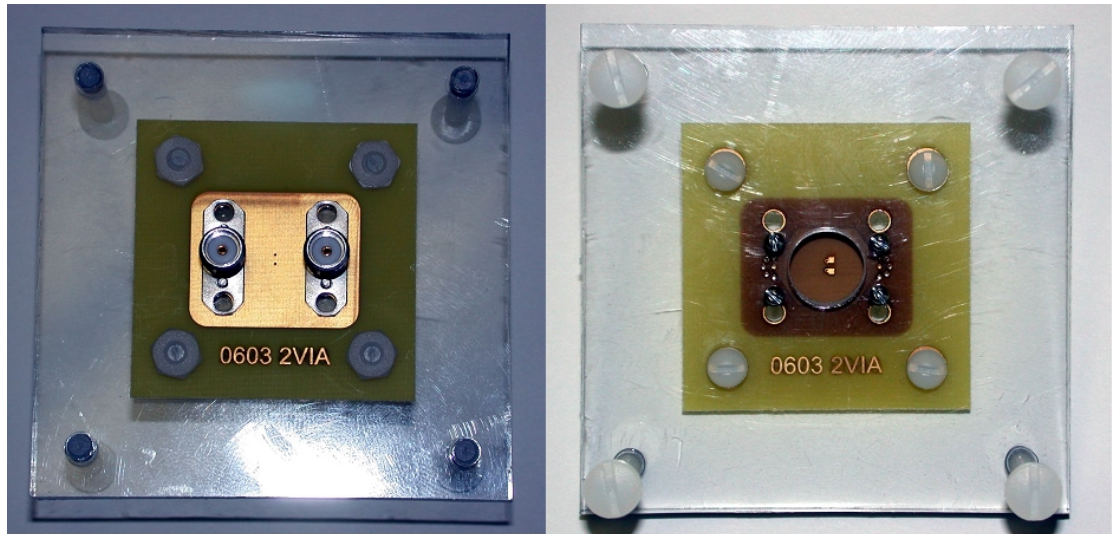
Figure 10, Teraspeed® / SigCon Capacitor Test Fixture

The fixture utilizes three layer PCBs to characterize mounted capacitor performance for various depths of the first PCB plane as shown in Figure 11:
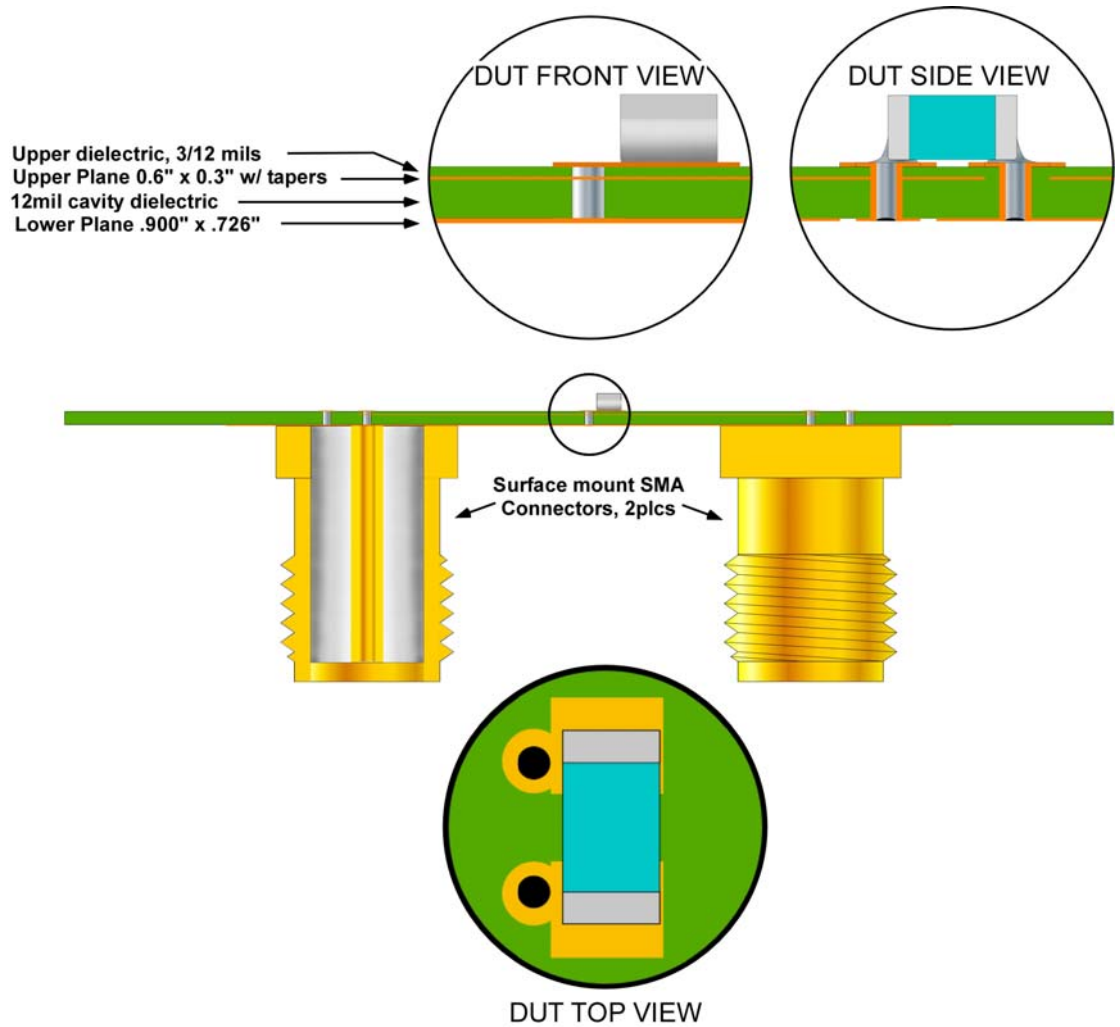
Upper dielectric, 3/12 mils
Upper Plane 0.6" x 0.3" w/ tapers
12mil cavity dielectric
Lower Plane .900" x .726"

DUT FRONT VIEW

DUT SIDE VIEW

Surface mount SMA
Connectors, 2plcs

DUT TOP VIEW

Figure 11, Detail View Inductance Characterization Fixture

The bottom layer of the board carries the bottom shield plane. Two surface mount SMA connectors bolt to the assembly, compressing against pads on the bottom layer. Twelve mils nominal dielectric separates the bottom and inner plane layers. A Teraspeed® designed launch transitions the 50ohm SMAs into the plane cavity. The inner plane etch fans from etch SMA center connection to a 300mil x 300mil region in the center.

The upper dielectric layer is selected to match a given board construction of interest. X2Y® has tested with both 3mil upper dielectric, typical of well-designed high layer count mechanically drilled PCBs, and 12 mil upper dielectric typical of low-cost 4/6 layer construction.

DUT Fixture Parasitics

In order to extract accurate measurements, the test fixture must have parasitics that are either small enough to neglect, or which can be measured with sufficient accuracy to make the residual error negligible. On the X2Y® fixture, the parasitics that most concern us are:

- Fixture parasitic plane capacitance.

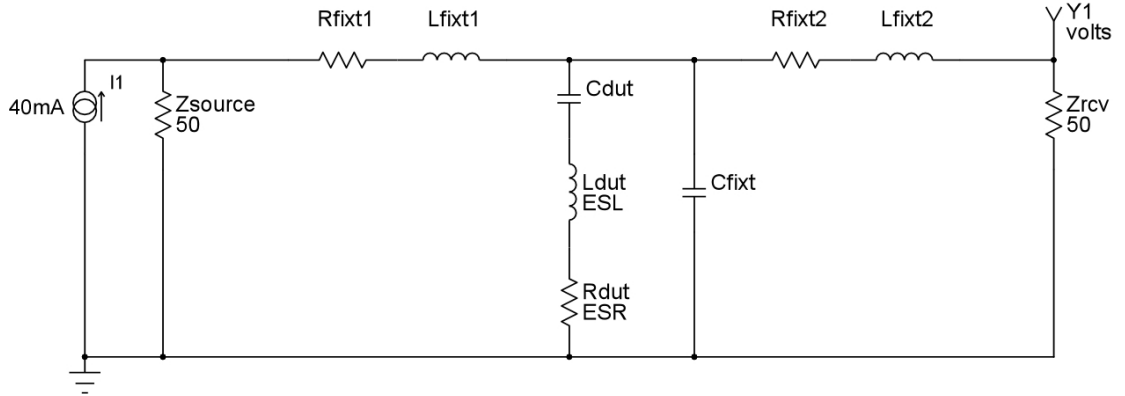- Fixture plane spreading inductance from SMA launches to the capacitor via attachments.

Figure 12, Model, Simplified 1D, Capacitor Test Fixture

Fixture Calibration

On any test fixture, the parasitic capacitance acts in parallel with the DUT capacitance, and also resonates with the DUT ESL.

Resonances occur at:

Equation 1. $F_{SRF} \approx 1/(2\Pi * \sqrt{ESL_{DUT}} * \sqrt{C_{DUT}})$

Equation 2. $F_{PRF} \approx \sqrt{(C_{DUT}+C_{PLANE})}/(2\Pi* \sqrt{ESL_{DUT}} * \sqrt{(C_{DUT}*C_{PLANE})})$

Equation 3. $F_{PRF} \approx F_{SRF} * \sqrt{(C_{DUT}/C_{PLANE} +1)}$

For ceramic capacitors with their relatively low ESRs, the SRF is relatively insensitive to fixture series parasitics, while the PRF is quite sensitive. Wide separation between fixture SRF and PRF facilitates accurate DUT inductance extraction. From Equation 3 we see that PRF and SRF are related by approximately the square root of DUT to fixture capacitance. Consequently, fixtures with very low capacitance facilitate good inductance measurements, while fixtures with high capacitance complicate measurements.

X2Y® employs two dimensional fixture models developed by Teraspeed®. These models discretize the test fixture into a matrix of ten element RLC bedspring subcircuits. For this test fixture, each element models a 0.025″ x 0.025″ square,

equivalent to about 4 picoseconds resolution. The element models account for both skin effect and dielectric absorption.

Fixture calibration begins by determining the material Er and plane cavity height by curve fitting a fixture with a shorted via(s) and no DUT. Shorting just the via(s) that connect from the far plane essentially reduces the test fixture to L3.
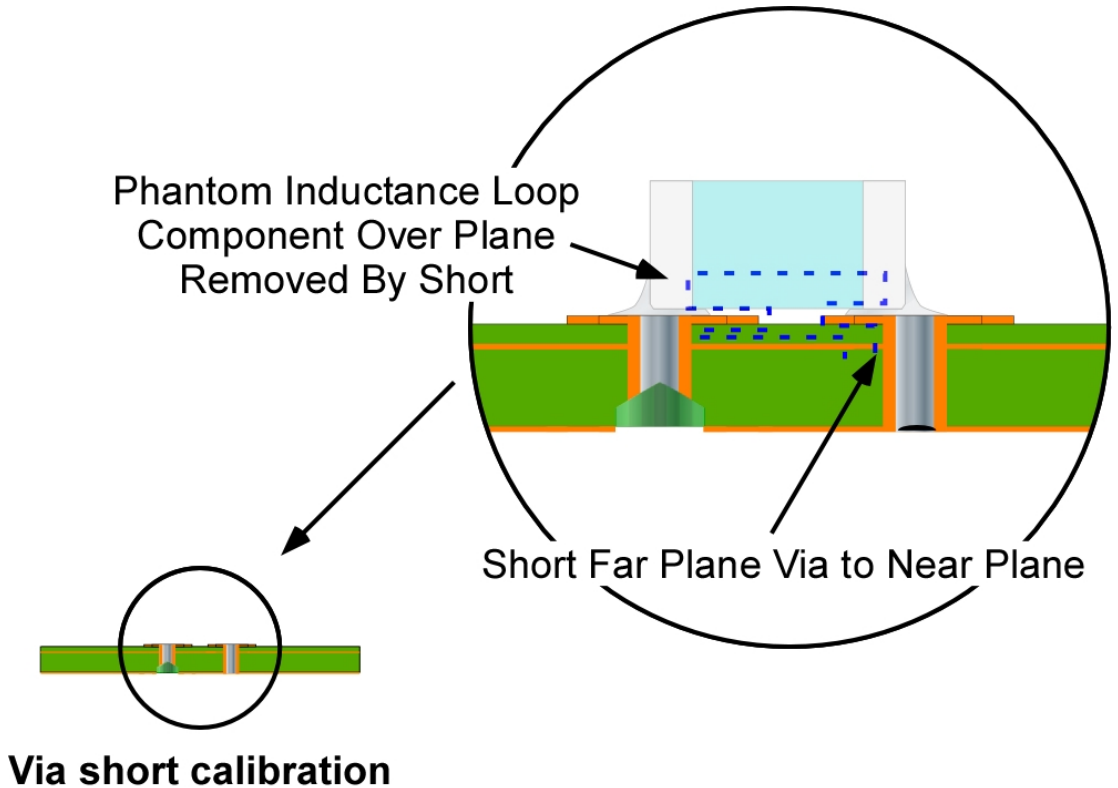

Figure 13, Test Fixture, Via Short Calibration

Figure 14, illustrates model to measurement match within a small fraction of a dB over more than three frequency decades, and more than 80dB magnitude span.
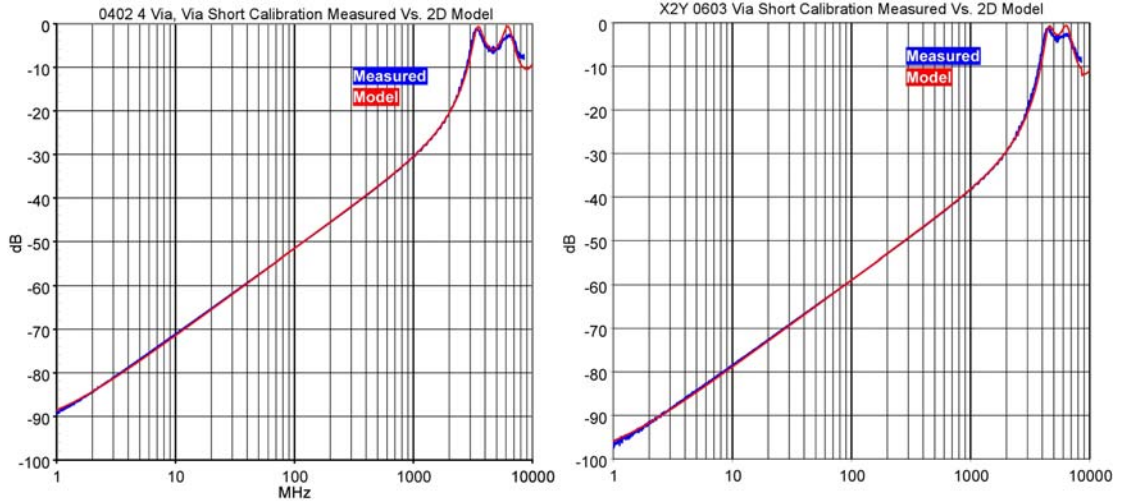
Figure 14, X2Y L1 Test Fixture Calibrations

As in Figure 9, the calibration fixture shorts only the vias extending from the plane furthest from the DUT. The inductance of the X2Y® alternate via pattern is everywhere less than one half that of the four via 0402.

Equation 4. $L_{FIXTURE} \approx 25 * 10^{DB\_100MHz/20}/6.28E8$

Capacitor Parameter Extraction

The single RLC model of a bypass capacitor is only an approximation. As shown in Figure 3, the working height of a bypass capacitor shrinks at rising frequencies. Low frequency fields easily penetrate through the many very thin, 1um to 5um metallization layers of MLCC capacitors. At higher frequencies, eddy currents in the metal layers impede field penetration, concentrating the average field lower and lower in the capacitor. In the limit, fields are constrained to only the bottom-most plates. This reduces the average height of the L1 induction loop, and therefore its apparent inductance.

The closer the uppermost plane is to the capacitor, the greater the proportional difference between the low and high frequency capacitor inductance. For typical capacitors attached to planes in the very top of the stack-up the variation can be more than 40%. The X2Y® L1 characterization fixture exposes both low and high frequency inductance to straightforward extraction.

Low Frequency Extraction

Low frequency parameter extraction may be accurately performed by the method described in: "Accurate Capacitor Inductance Extraction from S21 Measurements", Weir 2004. This method uses measurements at the SRF (maximum insertion loss), and at a second lower frequency F_1.

Selecting a low frequency measurement point $F_1 << F_{SRF}$, we get:

Equation 5. $ESR_{DUT} = 25 * 10^{dB\_SRF/20}/(1 - 10^{dB\_SRF/20})$

Equation 6. $C_{DUT} \approx \sqrt{(10^{-dB\_F1/10} - 1)}/(50 * \Pi * F_1)$

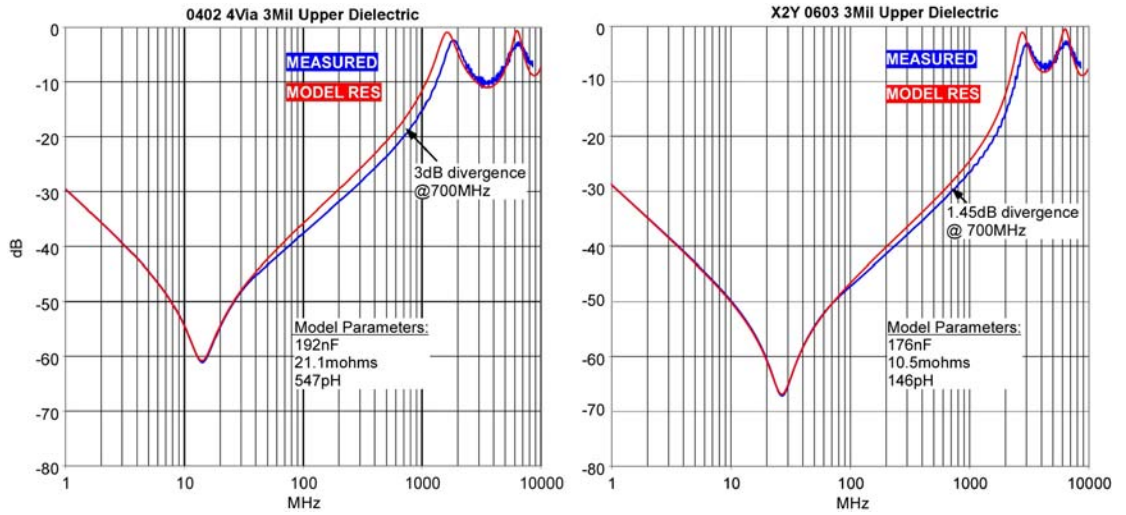**Equation 7.** $ESL_{DUT} \approx 1/((2*\Pi*F_{SRF})^2*C_{DUT}) - L_{FIXTURE}$

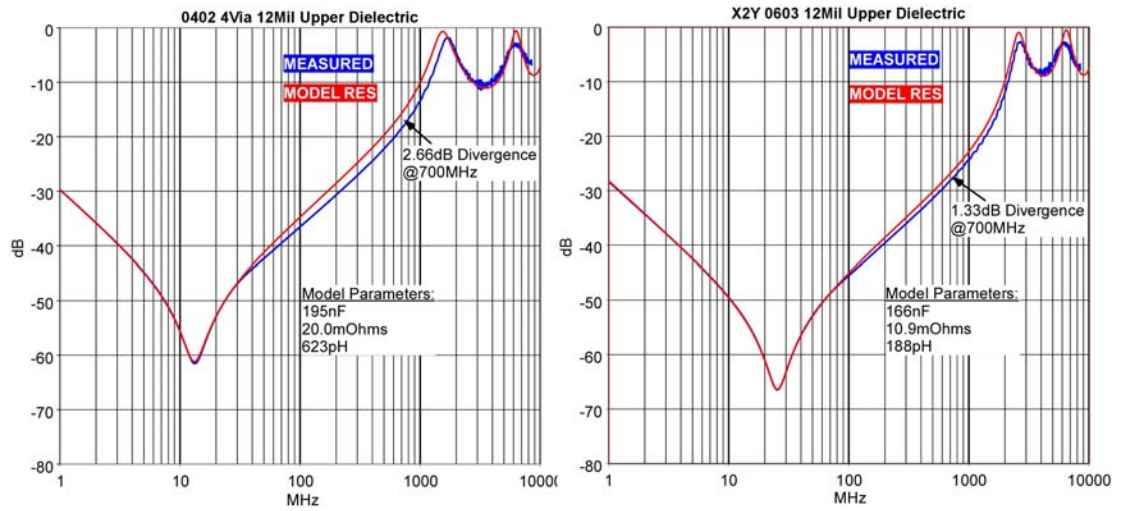**Figure 15, Low Frequency Inductance Extraction 3mil Upper Dielectric**

Figure 16, Low Frequency Inductance Extraction 12mil Upper Dielectric

The resonant method proves very accurate through capacitor SRF. The capacitor construction details, and the height above the nearest plane determine how much the model diverges from actual performance at high frequencies. Figure 15 and Figure 16, illustrate the dependence of divergence on the distance from the capacitor to the uppermost plane.

High Frequency Inductance Extraction

High frequency inductance well away from the SRF may be corrected by adjusting for the total divergence measured at a high frequency point:

Equation 8. $L_{DUT\_HF} \approx L_{DUT\_LF} - 10^{DIVERGE/20}*(L_{DUT\_LF} + L_{FIXTURE})$

This adjustment forces the modeled inductance to track actual behavior, but introduces error near the SRF as shown in Figure 17, and Figure 18.
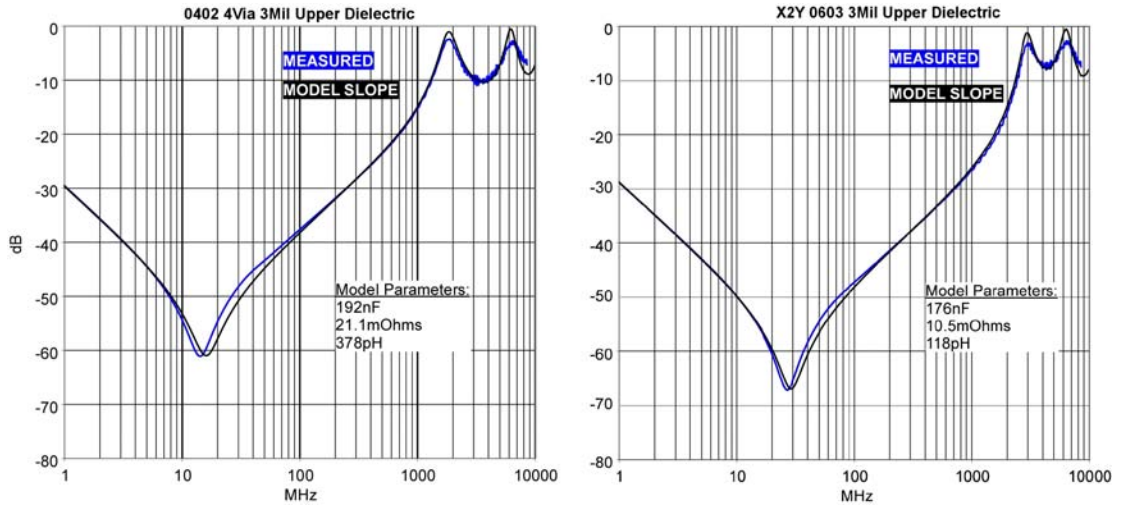

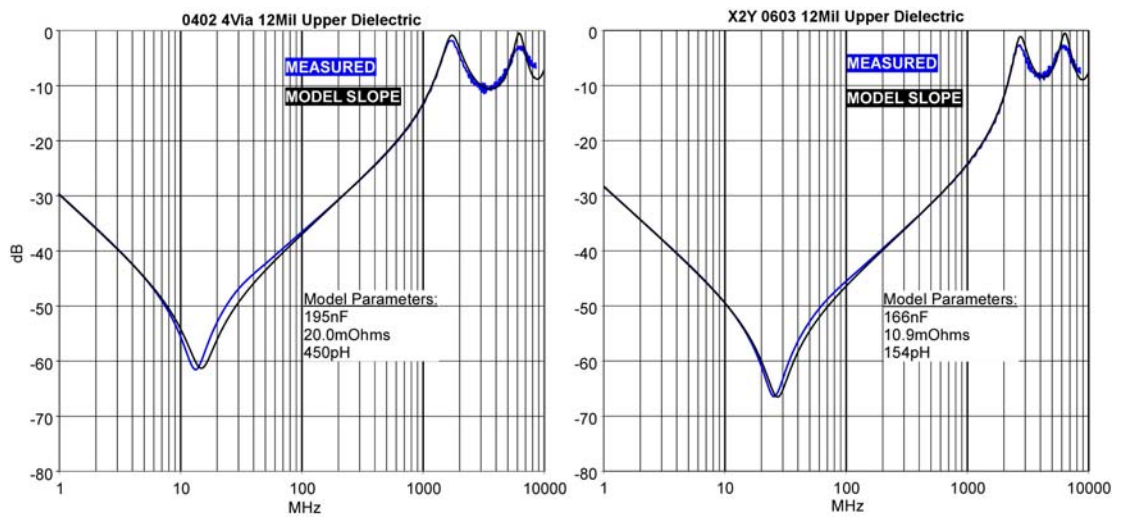**Figure 17, HF Frequency Inductance Extraction 3mil Upper Dielectric**

Figure 18, HF Frequency Inductance Extraction 12mil Upper Dielectric

De-embedded Test Results X2Y® versus Two and Four Via 0402s

The following table represents test results using the X2Y® fixture and the more conservative alternate X2Y® recommended layout:

Upper Dielectric Height	Capacitor	C	ESR	ESL			
				LF		HF	
				Value	%	Value	%
3 mils	X2Y® 0603	176nF	10.5mΩ	146pH	1.00	118pH	1.00
	0402 4 Via	193nF	22.1mΩ	547pH	3.75	378pH	3.20
	0402 2 Via	188nF	23.0mΩ	658pH	4.51	452pH	3.83
12 mils	X2Y® 0603	166nF	10.9mΩ	188pH	1.00	154pH	1.00
	0402 4 Via	199nF	20.2mΩ	643pH	3.42	450pH	2.92
	0402 2 Via	201nF	19.6mΩ	807pH	4.29	626pH	4.07

Table 1.   Capacitor Test Results

Live FPGA Board Test Results

X2Y® configured a test vehicle consisting of a Xilinx Virtex 4, XC4VLX25-FF668. 60 I/Os from each of six I/O groups connect via 50 ohm traces to Thevenin terminators. The scope photographs in xx compare I/O plane noise with 360 simultaneously switching outputs configured for SSTL2 Class II. Test boards were populated with various numbers of conventional 0402 capacitors using four vias each, and X2Y capacitors.

Sixteen of the 0402 capacitors, and sixteen X2Y capacitors share the inner of two capacitor rings. The remaining forty-eight conventional capacitors occupy an outer ring placed as close as practical to the inner ring.
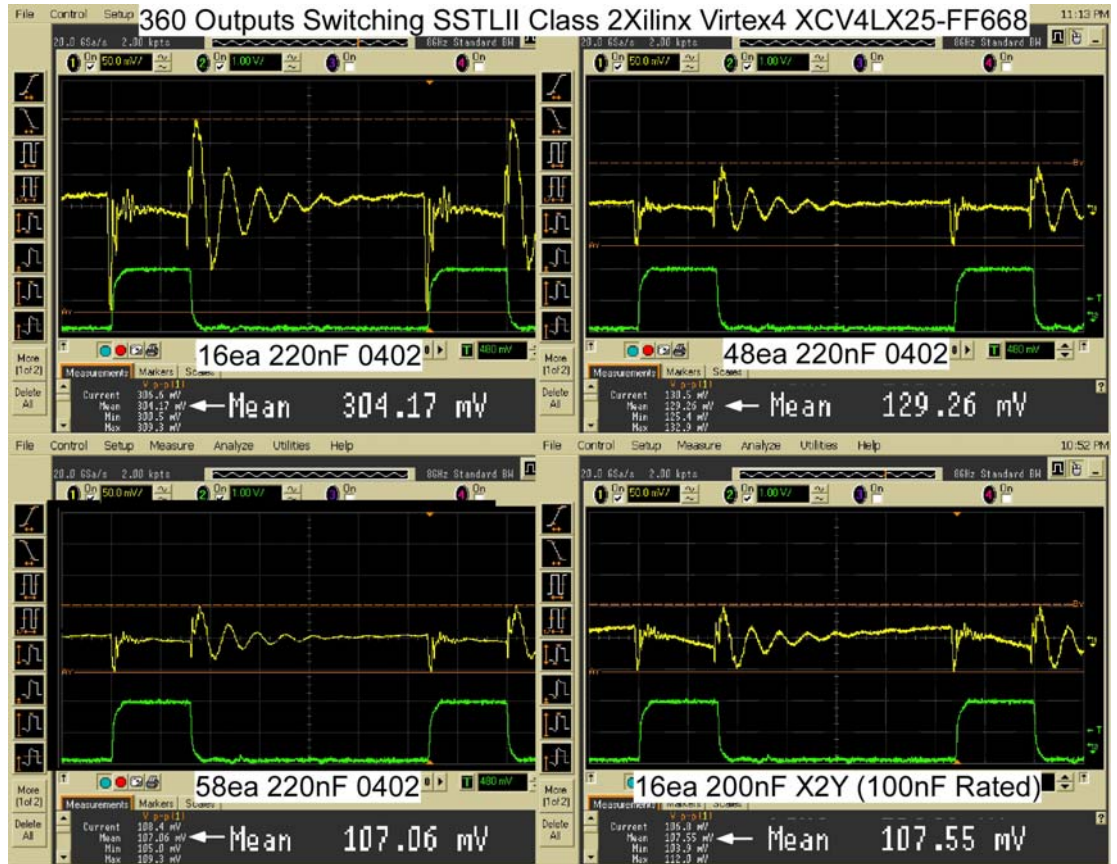
Figure 19, Live FPGA Card, Noise Comparisons

The 16 X2Y® capacitor configuration reduces p-p noise by nearly 3:1 compared to 16 0402s using four vias each. In order to reach noise parity, a total of 58 0402s, consuming 232 vias were needed. By comparison, the X2Y® array required only 96 vias total, less than 42% as many as the conventional capacitors.

X2Y's used to bypass the Thevenin terminator networks demonstrate similar performance advantages with 126mV p-p on the X2Y network, compared to 320mV p-p on the 0402 four via network. See Figure 20.

These real-life test vehicles demonstrate performance very consistent with the X2Y® characterization test fixture results.
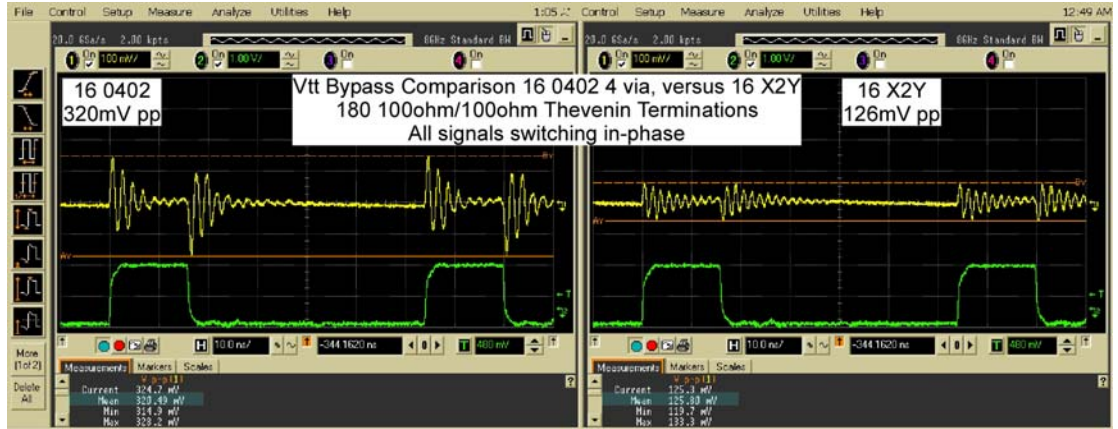
Figure 20, Vtt Noise Comparison

Conclusion

At high frequencies bypass capacitor performance is dictated by **mounted device inductance.** Accurate characterization of bypass capacitor parasitics particularly with low inductance capacitors requires great care in test fixture design to insure visibility of real device performance. X2Y® works closely with leading consultants to design and conduct accurate characterization tests that represent the state of the art.

X2Y® capacitors not only exhibit very low "device only" inductance, but also facilitate high performance via layouts that result in better via utilization than conventional capacitors. Test after test by industry experts confirm the superior performance of X2Y® capacitors.

Example application boards demonstrate 16 X2Y® capacitors with 96 vias total delivering the same bypass performance as 58 0402s attached with best practice four via connections each, 232 vias total: a more than 58% total via count reduction. Compared to typically mounted capacitors, X2Y replacement ratios in the range of 4:1 to 5:1 are common.[4]

Contact Information

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Author Acknowledgement

X2Y Attenuators, LLC would like to thank Steve Weir, Consultant with Teraspeed® Consulting Group LLC and X2Y Attenuators, LLC.

Mr. Weir has more than 20 years of industry experience and holds 17 U.S. patents. He has architected a number of packet and TDM switching products. Mr. Weir is a recognized expert in power delivery and a frequent contributor to the SI-list signal-integrity reflector.

References

[1] "TF-MP2 Inductance of Bypass Capacitors, How to Define, How to Measure, How to Simulate" "On the Uniqueness of Inductance of Bypass Capacitors" DesignCon East 2005, Istvan Novak

[2] "TF-MP2 Inductance of Bypass Capacitors, How to Define, How to Measure, How to Simulate" "Bypass Capacitor Inductance, Data Sheet Simplicity to Practical Reality" DesignCon East 2005, Steve Weir

[3] "TF-MP2 Inductance of Bypass Capacitors, How to Define, How to Measure, How to Simulate" "A Measurement Technique for High Frequency Low-Inductance Decoupling Capacitors", DesignCon East 2005, Joe Hock

[4] Note: performance results reported in this application note were achieved using patented X2Y® components sourced from licensed manufacturers, or their authorized distribution channels. Proper reference of the technology in circuit schematics, technical literature, or product sourcing documents requires use of registered trademark "X2Y®".