X2Y® G1/G2 Attachment

Summary

X2Y® components can be attached in several configurations depending on the application requirements and use. The goal of this application note is to provide a broad concept of attaching G1/G2 in applications to maximize performance. To explain the rationale for these attachment requirements, a brief discussion on the structure of standard capacitors, the structure of X2Y® components, and insertion loss is included. To emphasize the performance improvements of proper G1/G2 attachment, insertion loss measurements of an X2Y® component are included.

Standard Capacitors

Standard capacitor technology has been utilized for years. The internal design consists of alternating electrode plates. The plates are attached to opposing end terminations shown in Figure 1. Proper attachment using this component is intuitive, one terminal to each trace or via in a circuit.

Figure 1. *Standard capacitor construction is made up of alternating electrode plates. To increase capacitance value, multiple alternating plates are added.*

X2Y® Architecture

X2Y® components have a unique internal design. A parallel reference electrode structure is inserted between the alternating electrodes of a standard capacitor as shown in Figure 2. The reference electrode structure is terminated to two additional side terminations called G1 and G2. (Note: the X2Y® component's package is similar to a feedthrough capacitor's package, but the internal structures are entirely different.) The reference electrodes create two symmetrically balanced capacitive halves which create a capacitive circuit with matching tolerances (typically 1-2.5%) in a line-to-ground measured from either end terminal (A/B) to either side termination (G1/G2).

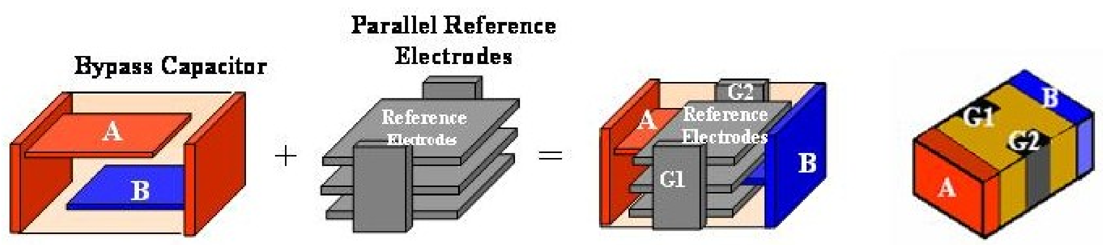

Figure 2. *Internal structure of an X2Y® component.*

Insertion Loss

Insertion Loss is the ratio of measured power resulting from the introduction of an electrical device in a transmission system to before the device was introduced[1]. Insertion loss is typically frequency and impedance dependant. (Typically, insertion loss measurements are taken in a 50Ω system.)

Insertion loss is usually expressed in decibel (dB). The equation to express insertion loss is:

$$\mathrm{dB} = 10\,\mathrm{Log}\left(\frac{\text{Power After}}{\text{Power Before}}\right)$$

X2Y® Testing, Results, and Explanation

To emphasize the importance of connecting G1 and G2, insertion loss measurements were taken on a microwave test fixture from Inter-Continental Microwave (ICM), shown in Figure 3. The fixture is used in combination with an HP8753E Vector Network Analyzer (VNA) to measure the components from 30KHz-6GHz. The VNA and test fixture is calibrated to 50Ω impedance.

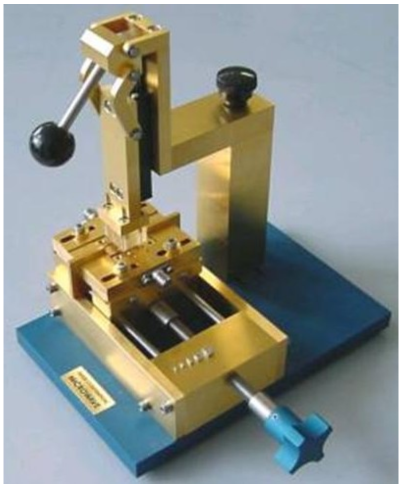

Figure 3. *Microwave test fixture used to measure insertion loss. Photo courtesy of Yageo-Phycomp.*

For the first measurement, illustrated in Figure 4, a Mylar sheet is inserted between G2 and one of the test fixture ground connections while G1 is allowed to make contact with the other test fixture ground connection.

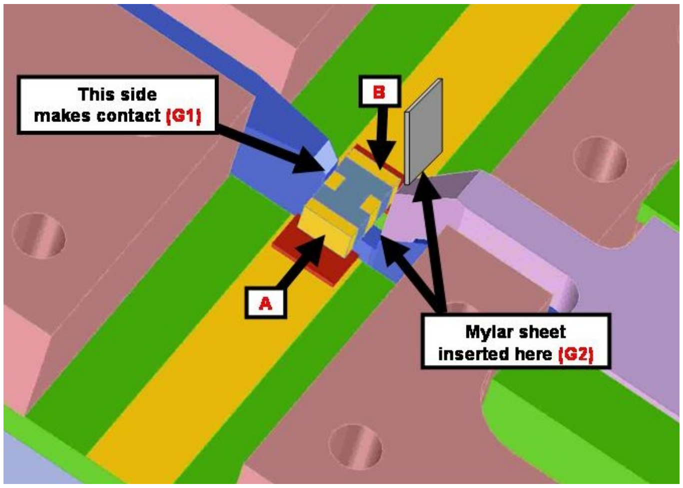

Figure 4. *Test fixture setup to measure the insertion loss with only one side termination grounded. Picture courtesy of Inter-Continental Microwave.*

The VNA applies a signal at the A terminal and records the series-thru results from terminal B with reference to ground. The resulting insertion loss measurement is shown in Figure 5.

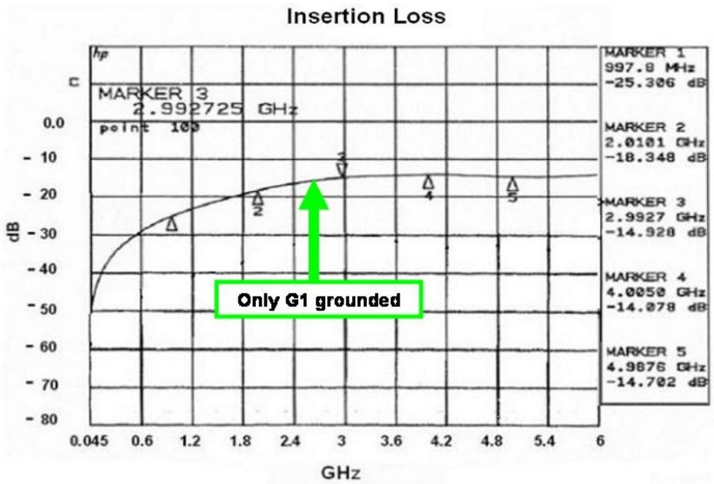

Figure 5. *Insertion loss measurement with only G1 terminated to ground.*

For the second measurement, the Mylar sheet is removed so that both side terminations of the component, G1 and G2, are allowed to make contact with the test fixture ground connections (Figure 6). Figure 7 is the results of insertion loss measurements. For reference, the first measurement (only G1 allowed to make contact with the fixture) is included.

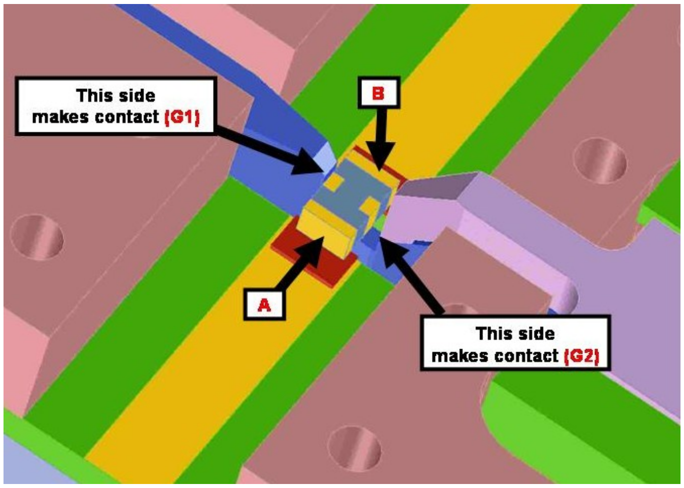

Figure 6. *Test fixture setup to measure the insertion loss with both side terminations grounded. Picture courtesy of Inter-Continental Microwave*

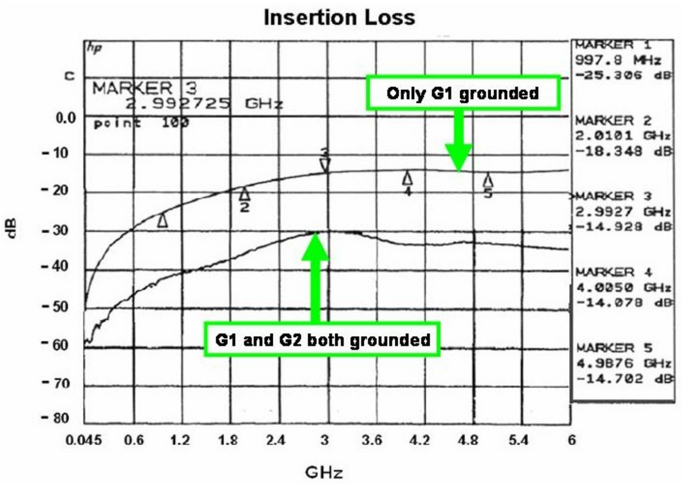

Figure 7. *Insertion loss measurements comparing G1 grounded versus both G1 and G2 grounded.*

A 15dB improvement across the entire bandwidth is observed when both G1 and G2 make contact with the both test fixture ground connections. To explain the improvement, an understanding of mounting parasitics is required. Mounting parasitics can be modeled as resistance and inductance in series with the X2Y® component terminals as shown in Figure 8. (Note Figure 8 is the external mounting parasitics only, NOT the internal model of an X2Y® component.)

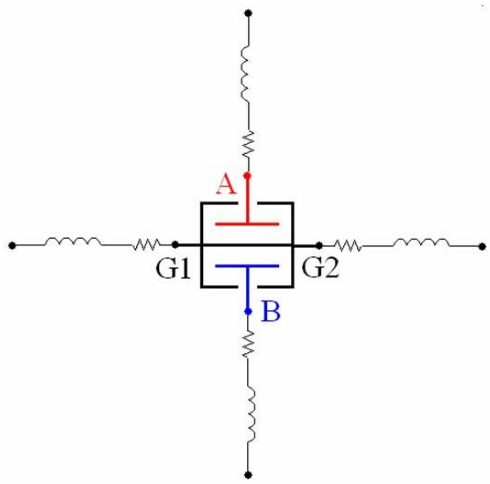

Figure 8. *Mounting parasitics of an X2Y® component*.

Since G1 and G2 terminations are internally connected in parallel (Figure 2), an important subtlety can be missed. When only one termination is connected, the connection from the component to the pad/trace is a series connection; whereas when both G1 and G2 are connected, the connection is parallel (Figure 9). By having a parallel connection, the mounting impedance is reduced by half (assuming that the mounting parasitics are equal for G1 and G2).

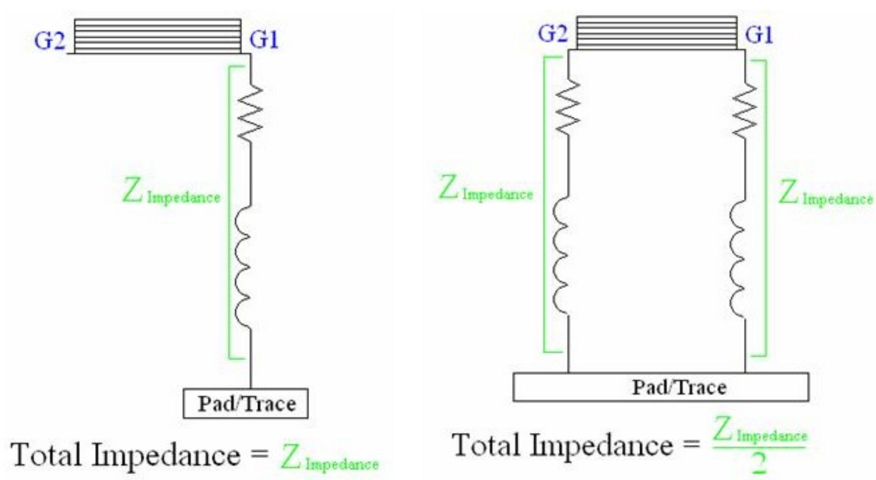

Figure 9. *When both G1 and G2 are attached, the total impedance seen by the component is reduced by one-half*.

PCB Layout for X2Y® Components

When laying out a PCB for an X2Y® component, there are two considerations. First is the number of pads/traces and their configuration. X2Y® is a four terminal component. It might seam intuitive when using an X2Y® component to use four individual pads/traces shown in Figure 10. A four pad/trace configuration would NOT be the optimum choice for performance.

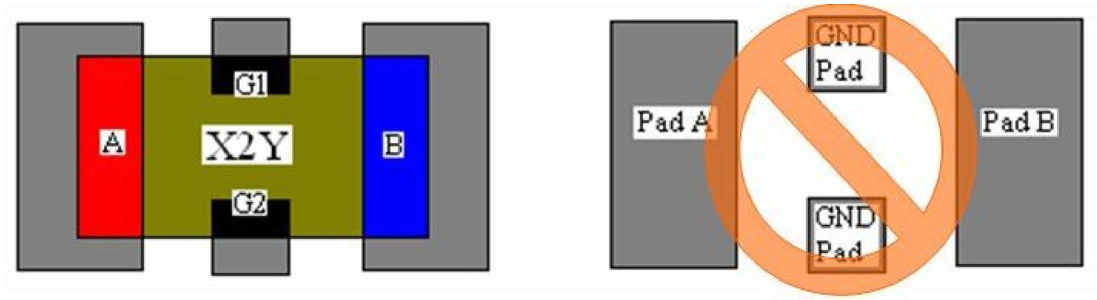

Figure 10. *Top-view of four pad PCB layout.*

To ensure that G1 and G2 are at the same potential and provide the minimum impedance between them externally, a three pad/trace configuration is advised (Figure 11). (Note: Depending on the circuit configuration, the A and B pads/traces may differ than what is shown. The concept here is the solid pad/trace for G1 and G2.)

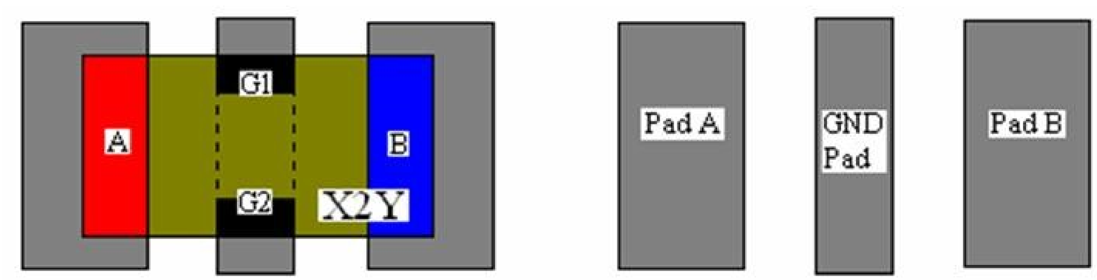

Figure 11. *Top-view of three pad PCB layout*

The second consideration is the number of layers a PCB has. When planes are used for power and ground instead of traces, vias are used to make connections to the pads. The parasitics associated with vias must be considered in attachment of an X2Y® component. Generally via inductance is larger than trace inductance and therefore needs to be minimized. In order to minimize via inductance multiple vias in parallel should be used.

For example, assume that a via's impedance between a pad and a ground plane is equal to Z_{via}. If two separate pads are used for G1 and G2, then the impedance seen by G1 and G2 would equal Z_{via} (left Figure 12). Now consider if the two vias are attached by a solid pad/trace (middle Figure 12). The impedance seen by G1 and G2 is now reduced to one-half Z_{via}. Generally three vias can be placed in the solid G1/G2 pad/trace and reduce the impedance to one-third Z_{via} (right Figure 12).

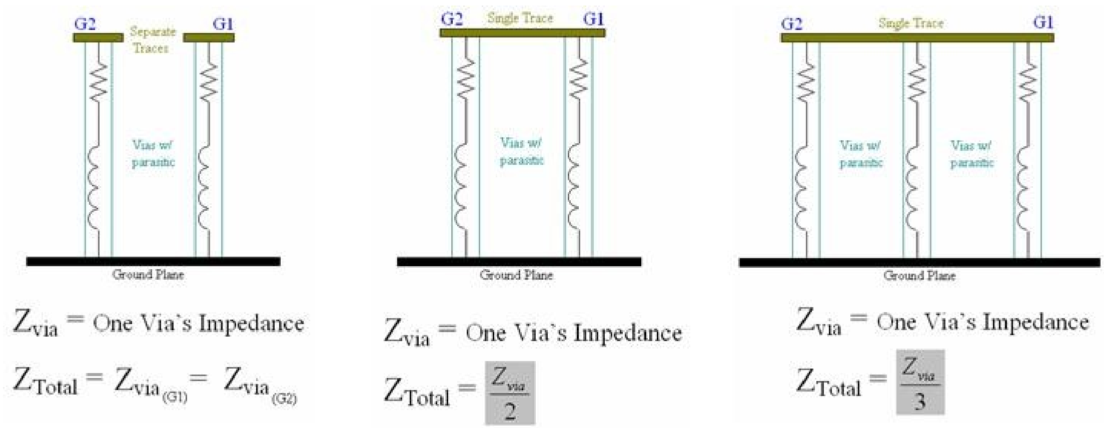

Figure 12. *Multiple vias attached in parallel reduce vias' impedance*.

The minimum recommended number of vias is 2, but 3 is preferred for optimum performance. (Note: vias are not required to be located directly below the component, but are advised for best possible performance.)

Conclusion

Attachment of X2Y® components is a straightforward and simple process when the proper attachment requirements for G1 and G2 are defined. The key for optimum performance is to minimize mounting parasitics. To accomplish this, a parallel ground structure should be built from the component to the ground plane.

Note: Performance results reported in this and other application notes can only be achieved with patented X2Y® components sourced from X2Y® licensed manufacturers or their authorized distribution channels.

References

[1] "The IEEE Standard Dictionary of Electrical and Electronics Terms." IEEE Std 100-1996.

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