High Speed Decoupling Strategies with fewer Capacitors

By James Muccioli & Dale Sanders
X2Y Attenuators, LLC © 24 July, 2006

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CTO X2Y Attenuators, LLC

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The Goal of Decoupling

- Supply DC power to IC for proper functionality.
- Minimize switching noise generated by IC.

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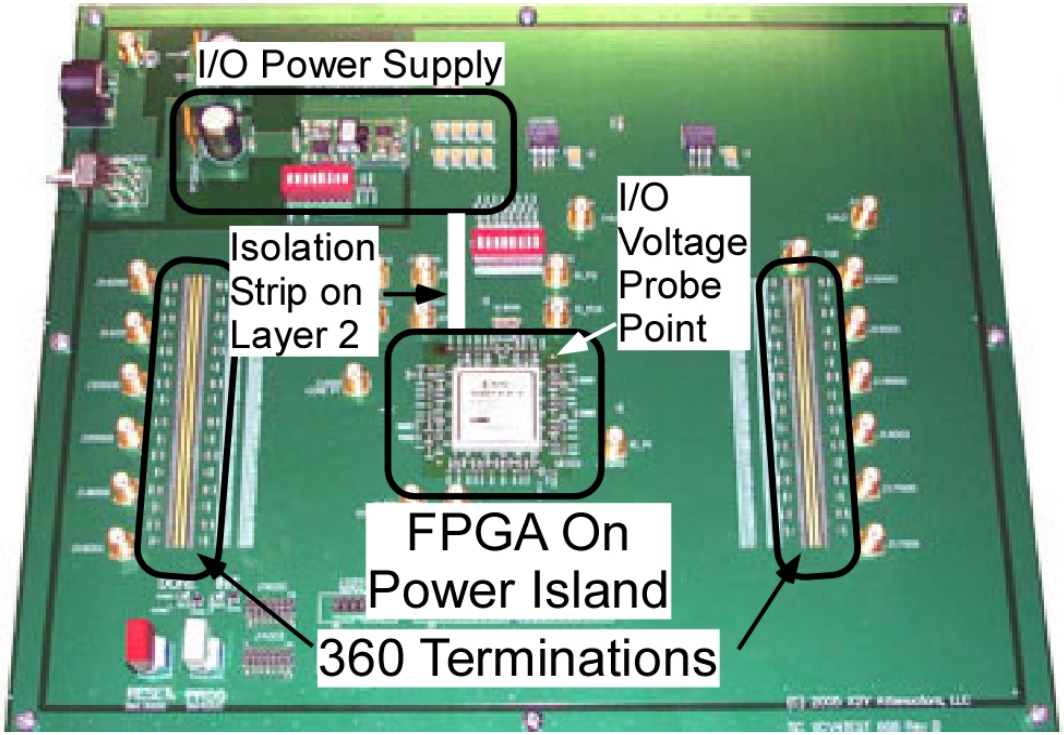
The Goal of Decoupling



Layer	Function
1	Component / ground fill
2	**I/O power**
3	**Ground**
4	Signal
5	Signal
6	Ground
7	Ground
8	Signal
9	Signal
10	**Ground**
11	**Core Power, I/O power**
12	Solder side comp / ground fill

The Goal of Decoupling

Power Distribution System (PDS)

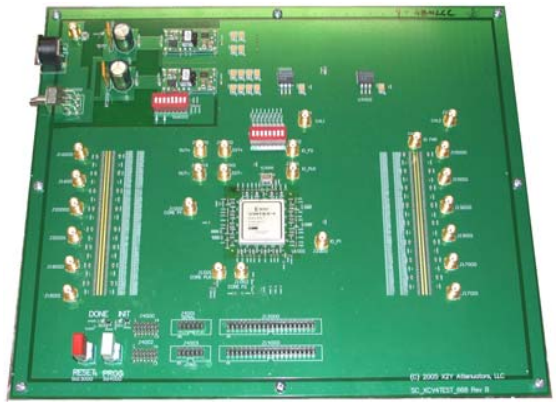
- Is not a perfect DC supply due to parasitics.
- PDS needs defined voltage levels that include max & min values to ensure IC and other circuits functionality.
- Voltage levels require the PDS to have a target impedance.
- Capacitors are used to meet target impedances to prevent:
  - Current Ripples – supply instantaneous current (energy).
  - Bypass transients – filter high frequency switching noise.

What are the PDS design issues?

- Inductance
  - Caps
  - Vias
  - Component mounting
  - PCB plane location/stack-up
  - Package
- PCB real-estate
  - Number of caps & vias
  - Location/effectiveness
  - Placement cost
  - Multiple power planes

Signal Integrity (SI)

- Number of vias (routing)
- Manufacturing cost (multiple plane PCBs)
- Functionality



The Goal of Decoupling

What Does the Bypass Network Do?

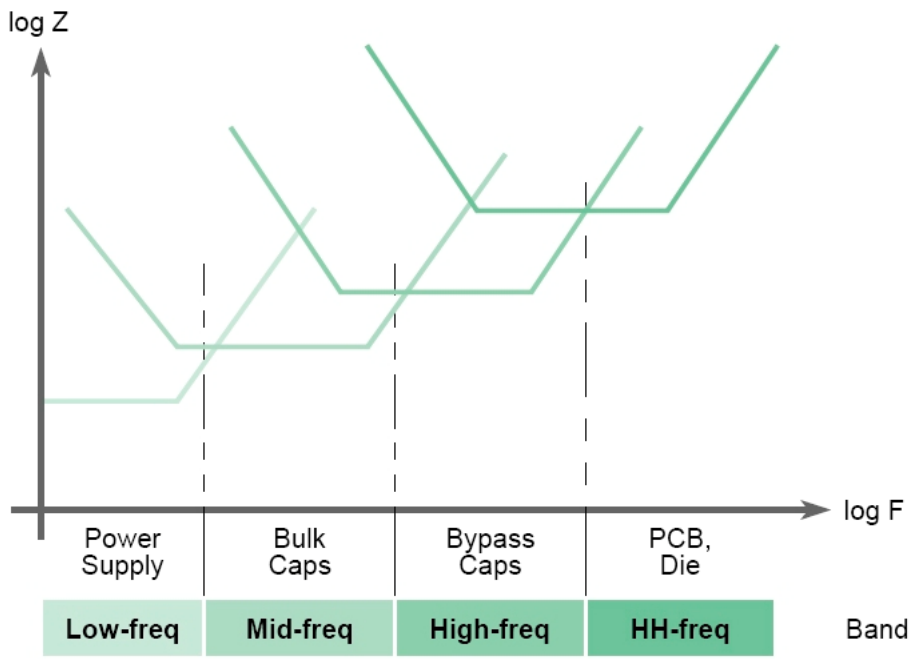
A bypass filter network applies a shunt across the power rails of sufficiently low impedance to maintain rail voltage in the presence of switching currents. In a modern system, we are concerned with switching currents that range:

- One time surge as the power rails initial charge. Large spikes can occur for a few uS to a millisecond or more as the rails transition through a range that biases CMOS FETs in their linear regions.
- Repetitive surges as power-managed devices enable or disable large functional blocks.
- Pulsating core currents associated with large state machine or memory block operations.
- Pulsating I/O currents associated with signaling.
- Where Vdd planes are used as signal return image planes, bridges signal switching currents

DesignCon East 2005; "Bypass Filter Design Considerations for Modern Digital Systems, A Comparative Evaluation of the Big "V", Multi-pole, and Many Pole Bypass Strategies" ;Steve Weir, Teraspeed Consulting Group

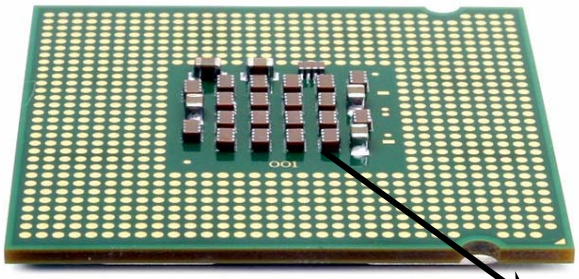
The Goal of Decoupling

- Decoupling capacitors consist of:
  - Large value caps – bulk caps (mid-freq).
  - Small value caps – bypass/H.F. caps (high-freq).

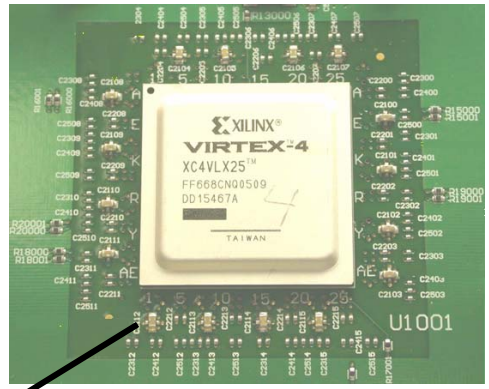


Milliorn, Gary, "Power Supply Design for PowerPCTM Processors," Freescale Semiconductor Application Note AN2447, Rev. 1.1, Sept 2004.

The Goal of Decoupling



On package caps



Topside caps

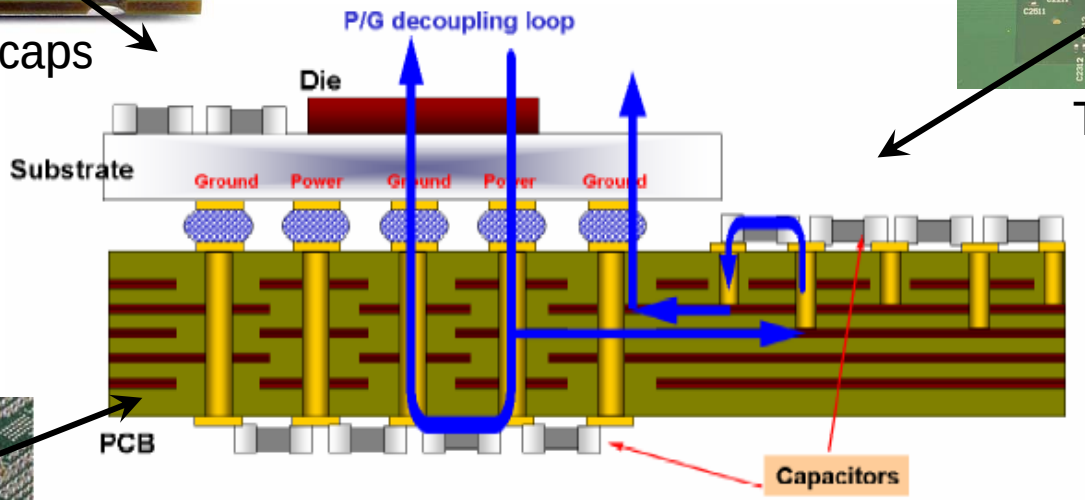
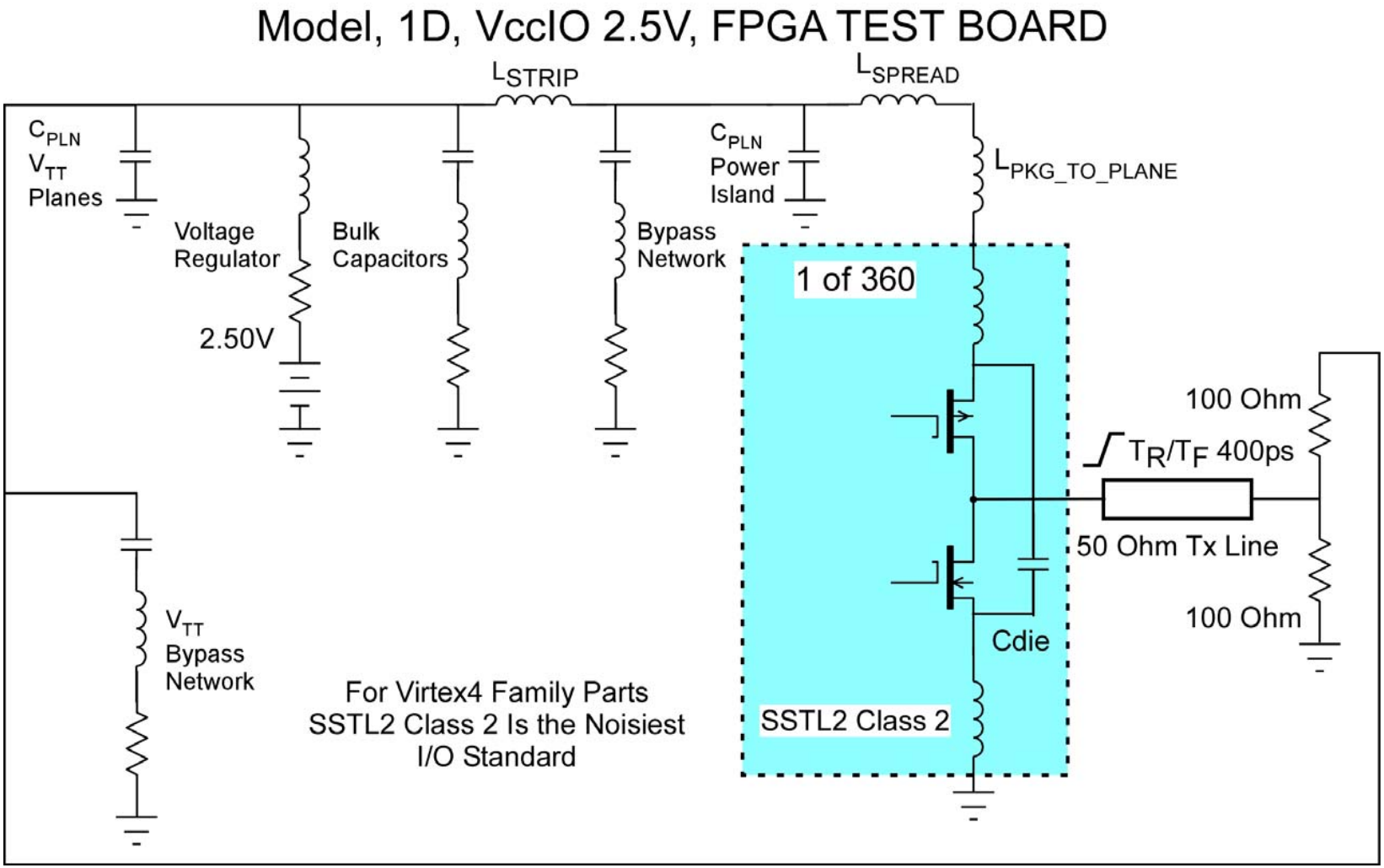


Fig. 1. System decoupling loops for PCB-mounted decoupling capacitors.

Backside caps

"Decoupling Capacitance Platform for Substrates, Sockets, and Interposers", DesignCon 2005

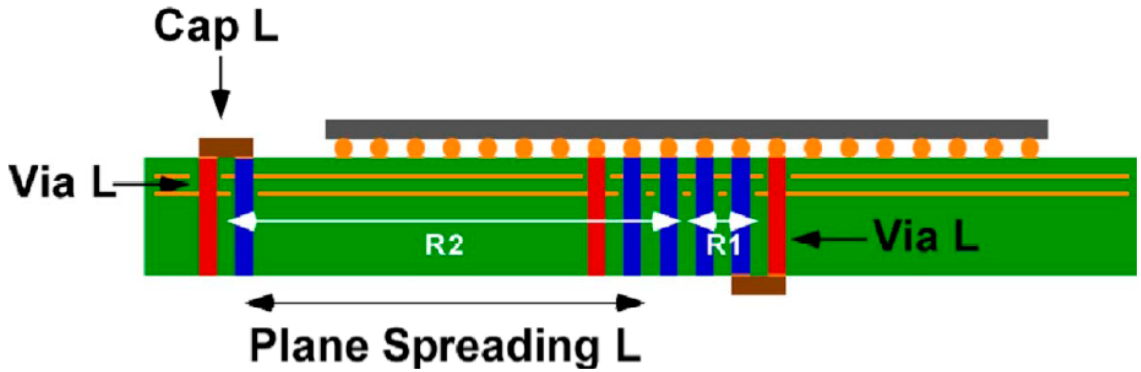
The Goal of Decoupling

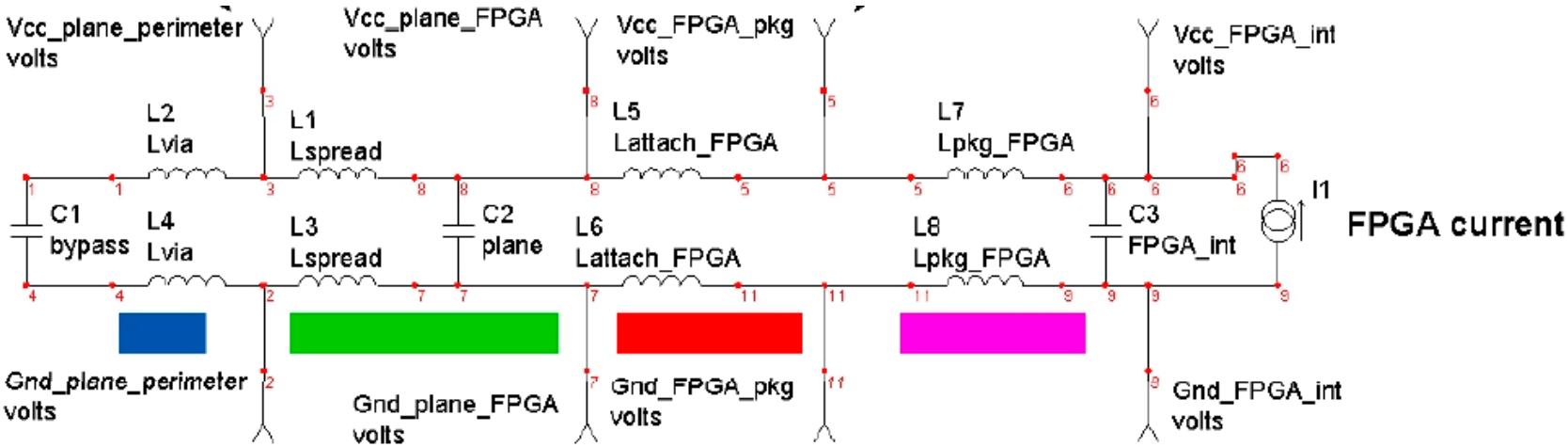


"FPGA Board Design, Steve Weir and X2Y Attenuators, LLC"

The Goal of Decoupling

PDS Example

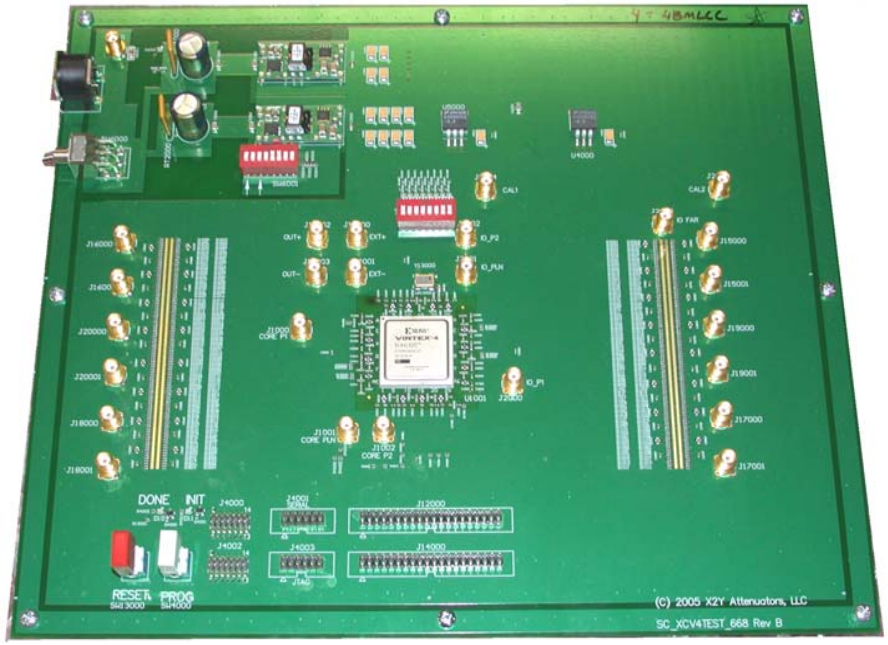


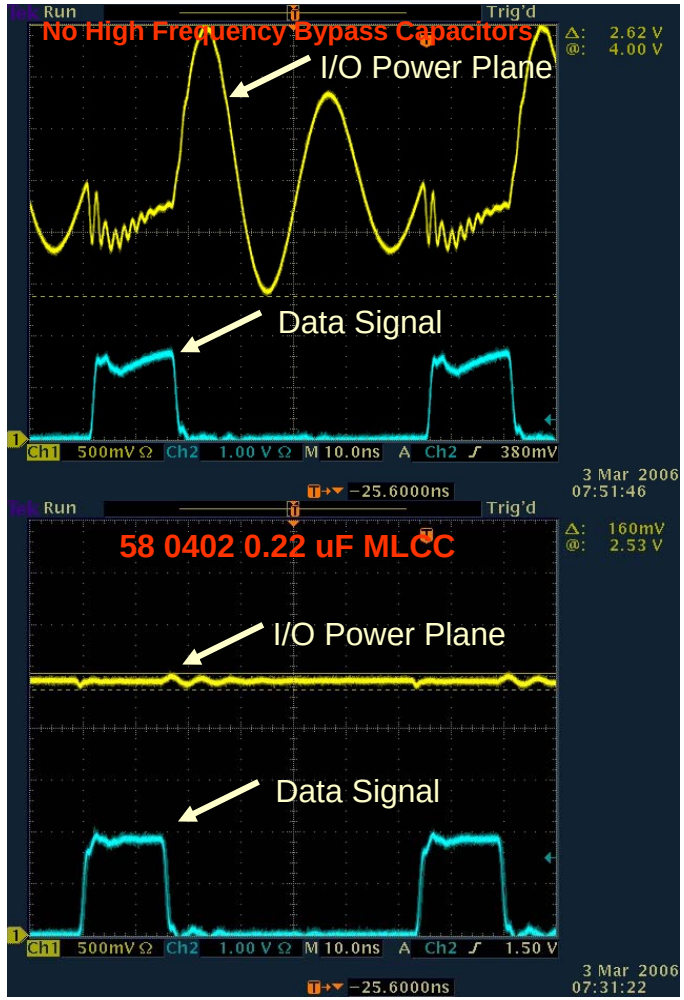


Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

The Goal of Decoupling

Bypass performance using an active FPGA circuit





The Tektronix TDS 3054 Scope Measurements

The Goal of Decoupling (Summary)

- In order to design a power distribution system (PDS) to meet all of IC requirements for power and noise, the total system from decoupling capacitors to IC must be analyzed.

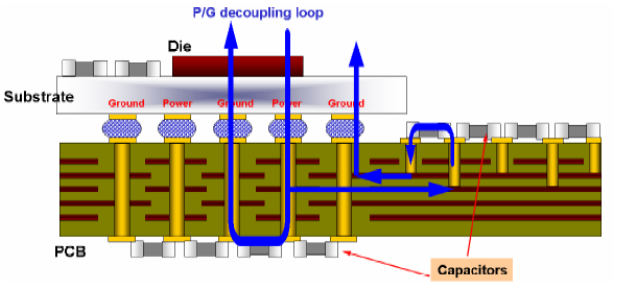
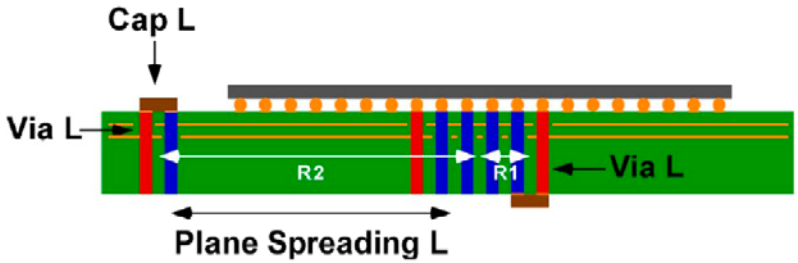
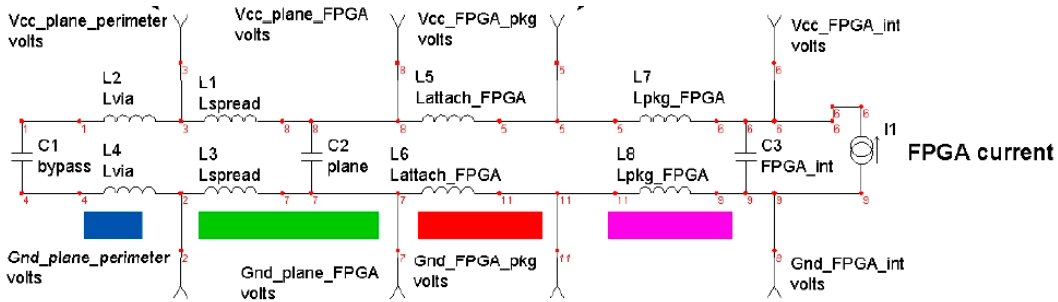


Fig. 1. System decoupling loops for PCB-mounted decoupling capacitors.





Component Evaluation Techniques

- Understand component-only vs. component-in-system evaluation.
- Measurement techniques that represent what an IC would see .

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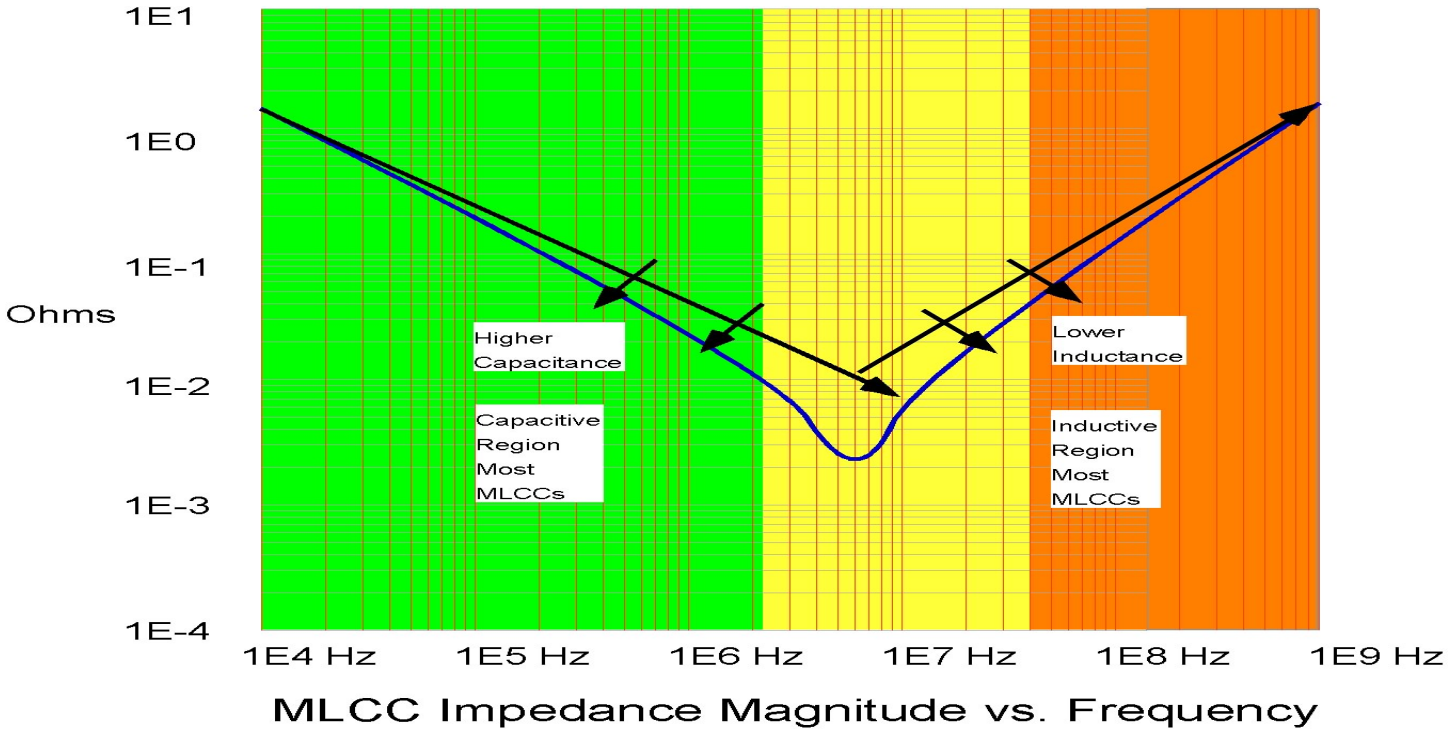
MLCC Bypass Capacitor Basics

Capacitor impedance magnitude follows a familiar "V" shape. Impedance falls from a theoretical value of infinity at DC to a minimum representative of the ESR at device mounted self-resonant frequency where the capacitive reactance and inductive reactance are equal. At higher frequencies the inductive reactance dominates.



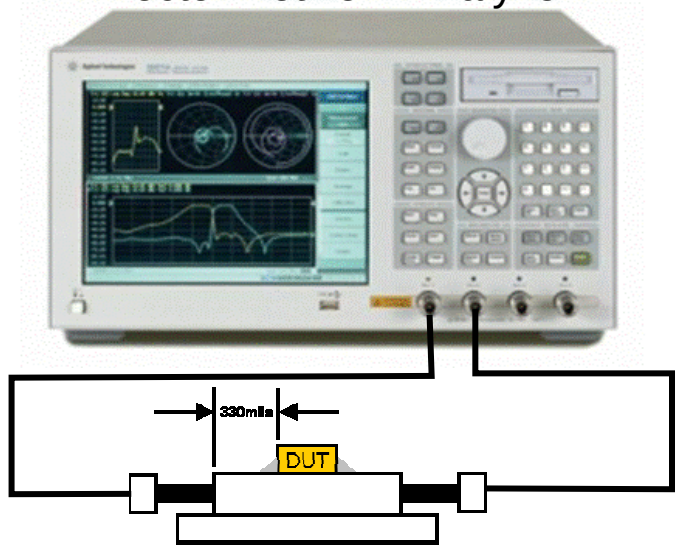
DesignCon East 2005; "Bypass Filter Design Considerations for Modern Digital Systems, A Comparative Evaluation of the Big "V", Multi-pole, and Many Pole Bypass Strategies" ;Steve Weir, Teraspeed Consulting Group

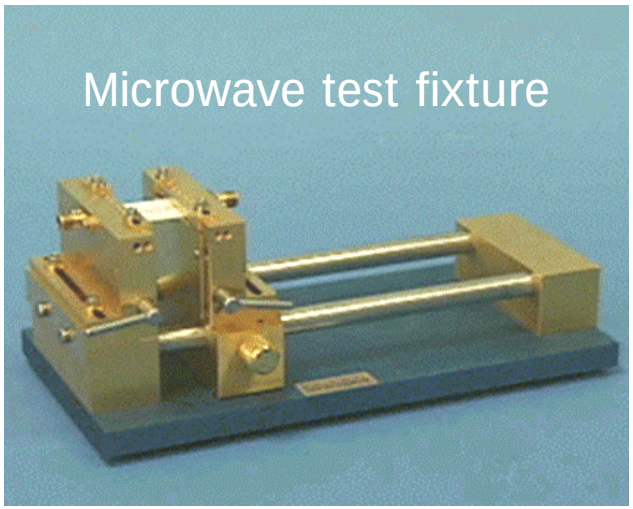
Component Evaluation Techniques

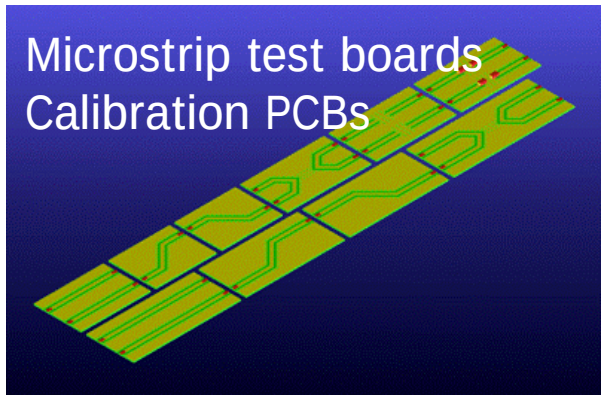
Component-only Measurement System

- WK-3000 Series Universal Substrate Test Fixture
  - Designed by Inter-Continental Microwave
- Agilent 5071A (300kHz – 8.5GHz)
- TRL calibration
- PCBs material, Rogers RT5880
  - 10 mil thick material
  - 20 mil thick material (depending on DUT size, to maintain 50 Ohms)

Vector Network Analyzer

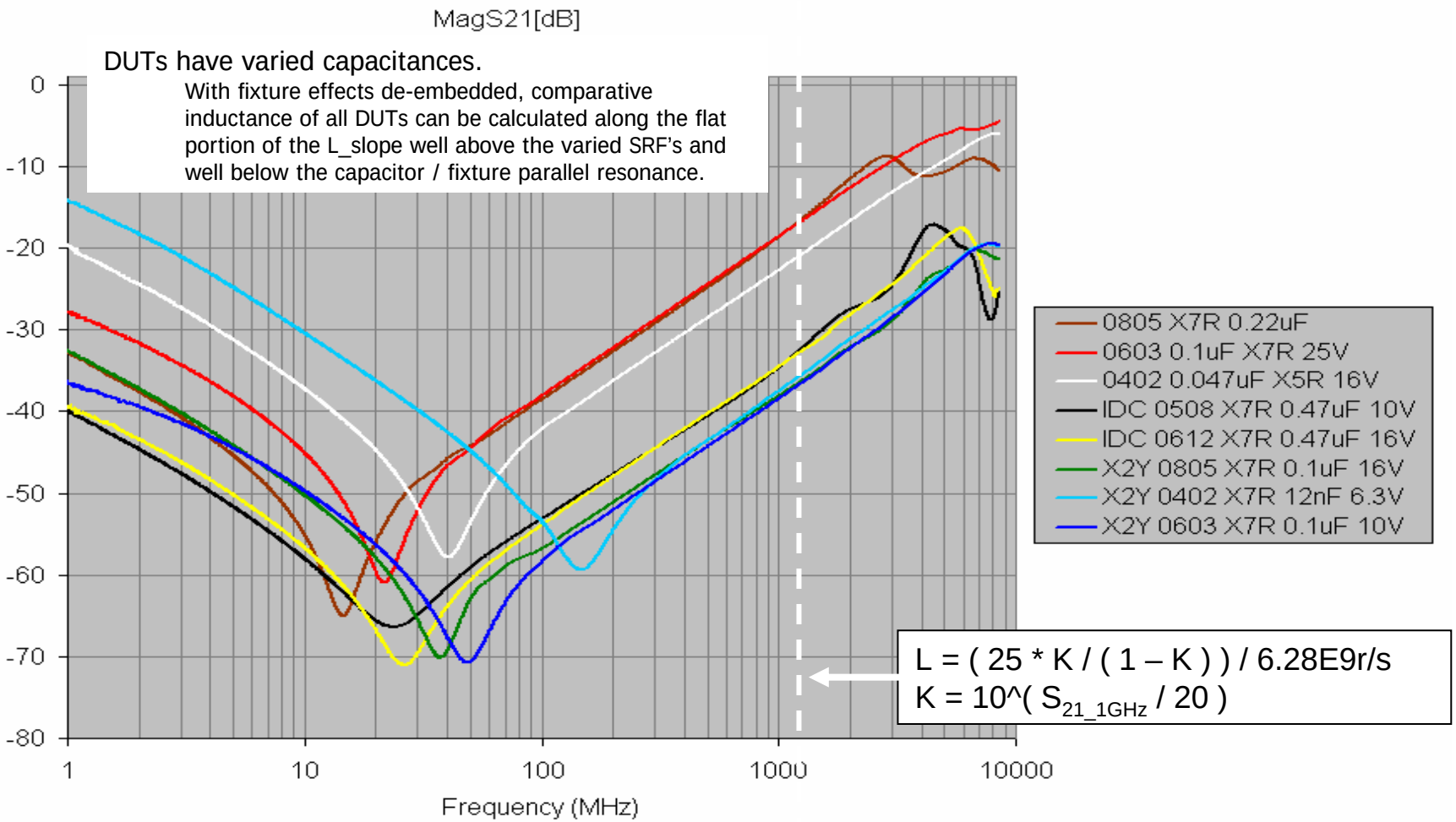






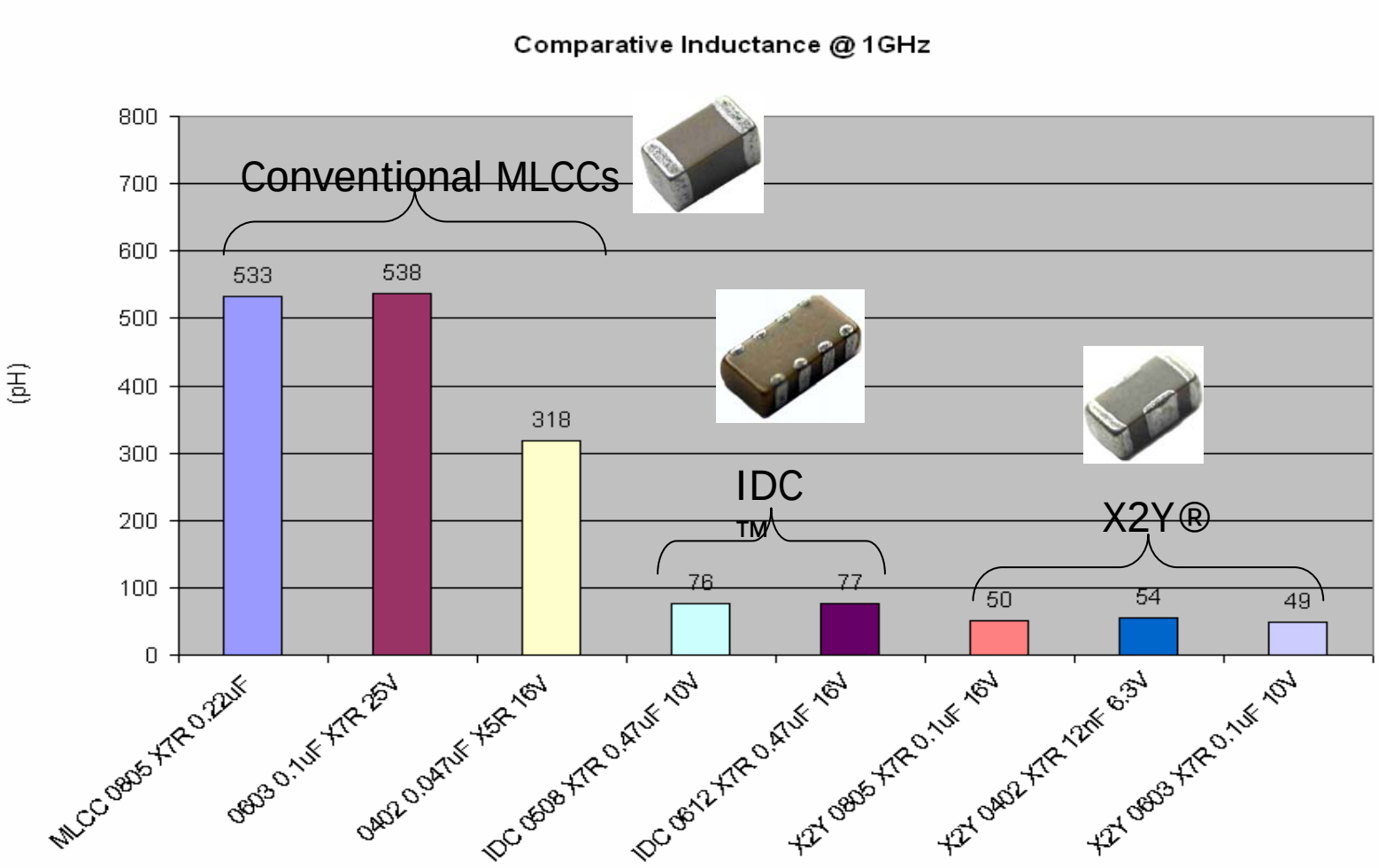
Component Evaluation Techniques

Component-only Measurement Results



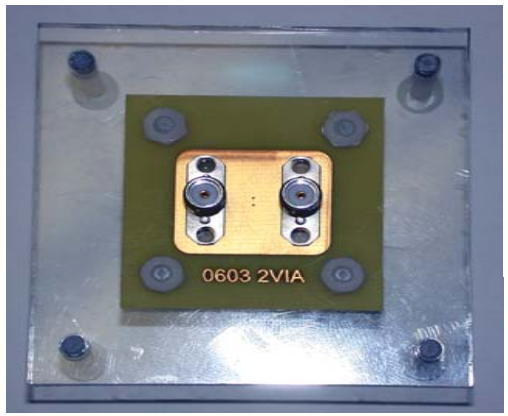
Component Evaluation Techniques

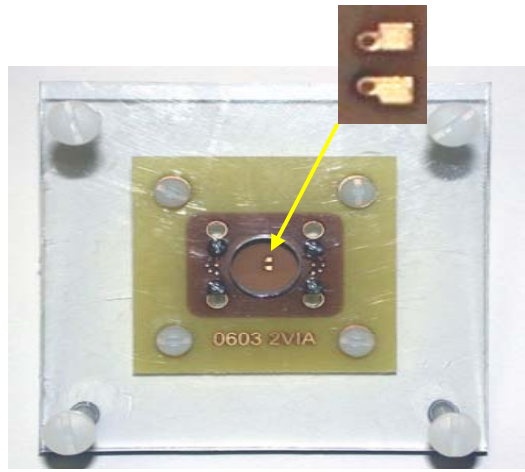
Component-only Extracted Inductance results

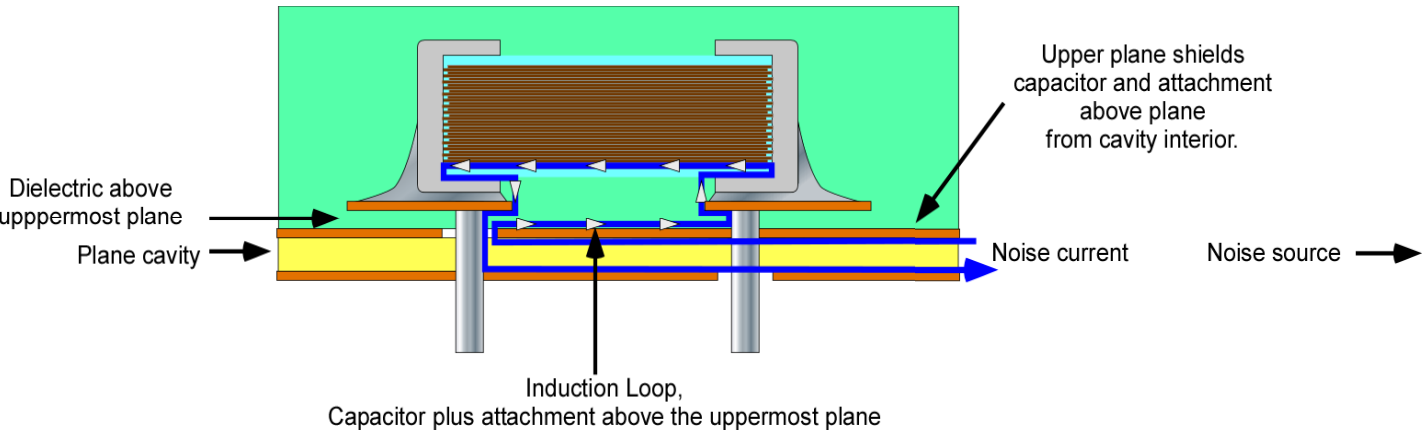


Component Evaluation Techniques

Component-in-System Fixture – where mounting, vias, and plane height are also included in the measurement.





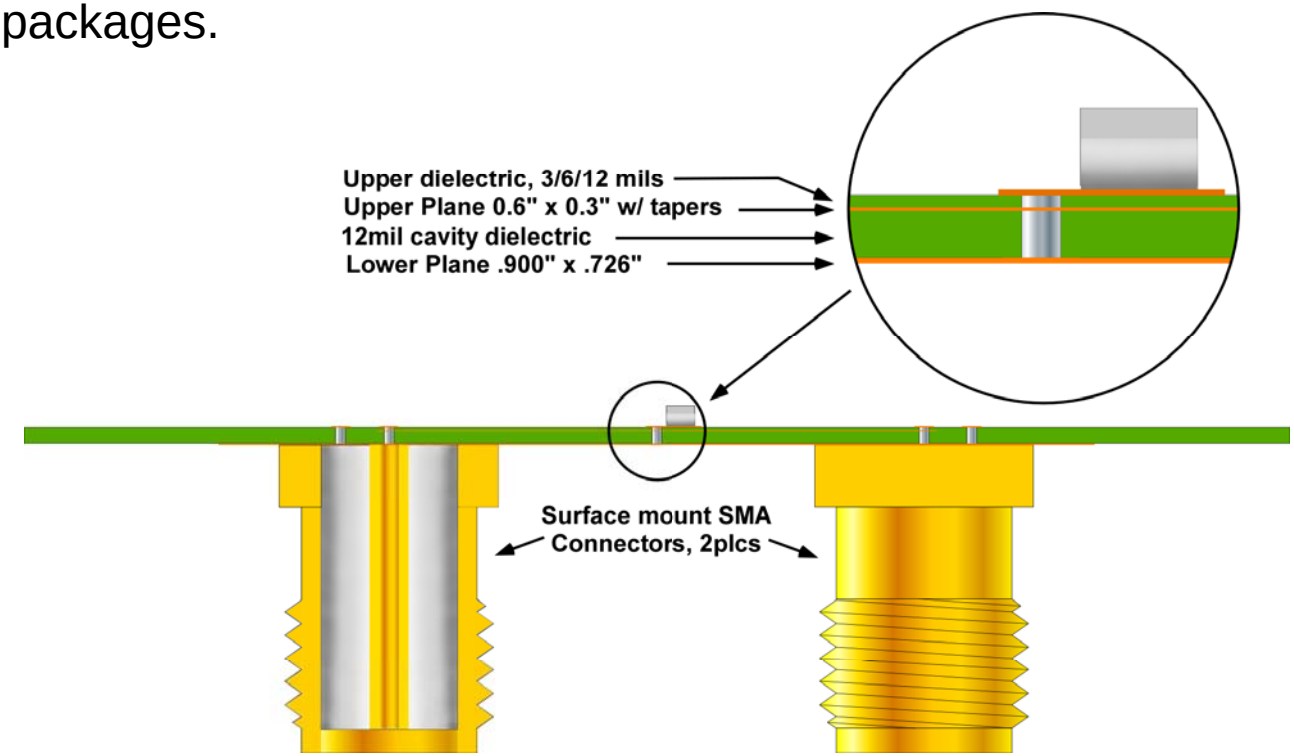


Bypass Capacitor Inductance, Data Sheet Simplicity to Practical Reality, Steve Weir Teraspeed Consulting Group LLC, DesignCon East 2005, TF -7

Component Evaluation Techniques

Component-in-System Fixture

- Joint fixture development between Dr. Howard Johnson, Signal Consulting, Inc, and Teraspeed, LLC.
- Suitable to evaluate bypass capacitors 1nF and larger from 0201 through 1812 packages.

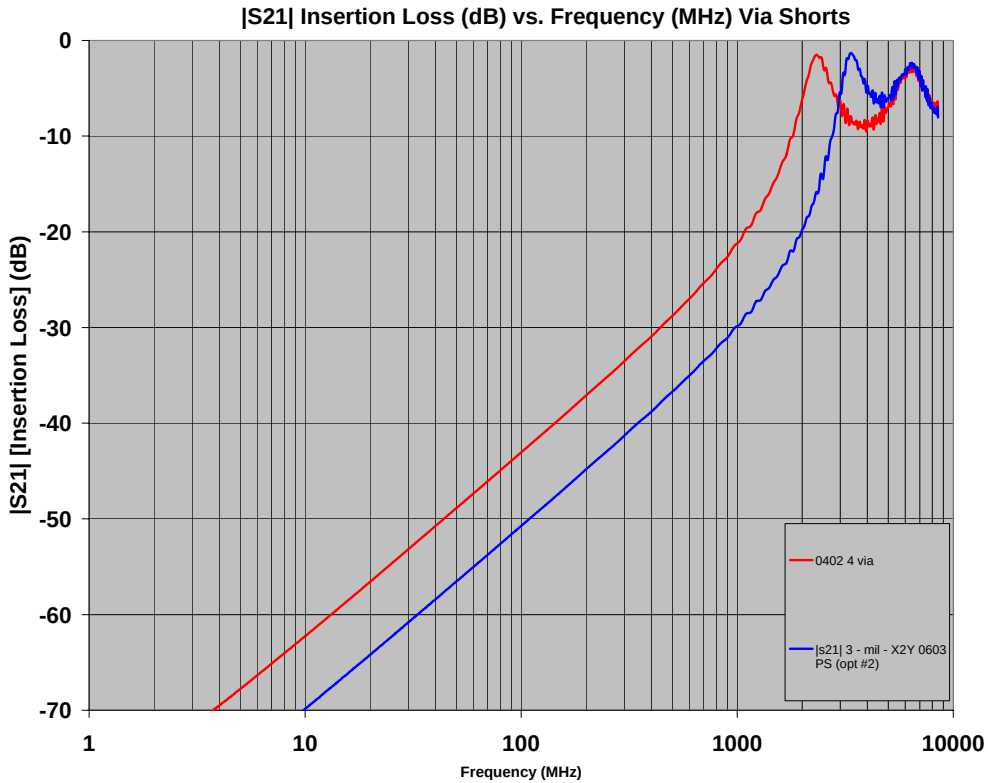


Bypass Capacitor Inductance, Data Sheet Simplicity to Practical Reality, Steve Weir Teraspeed Consulting Group LLC, DesignCon East 2005, TF -7

Component Evaluation Techniques

Component-in-System – via short calibration

Example Results: 4via 0402, 6 via X2Y 0603



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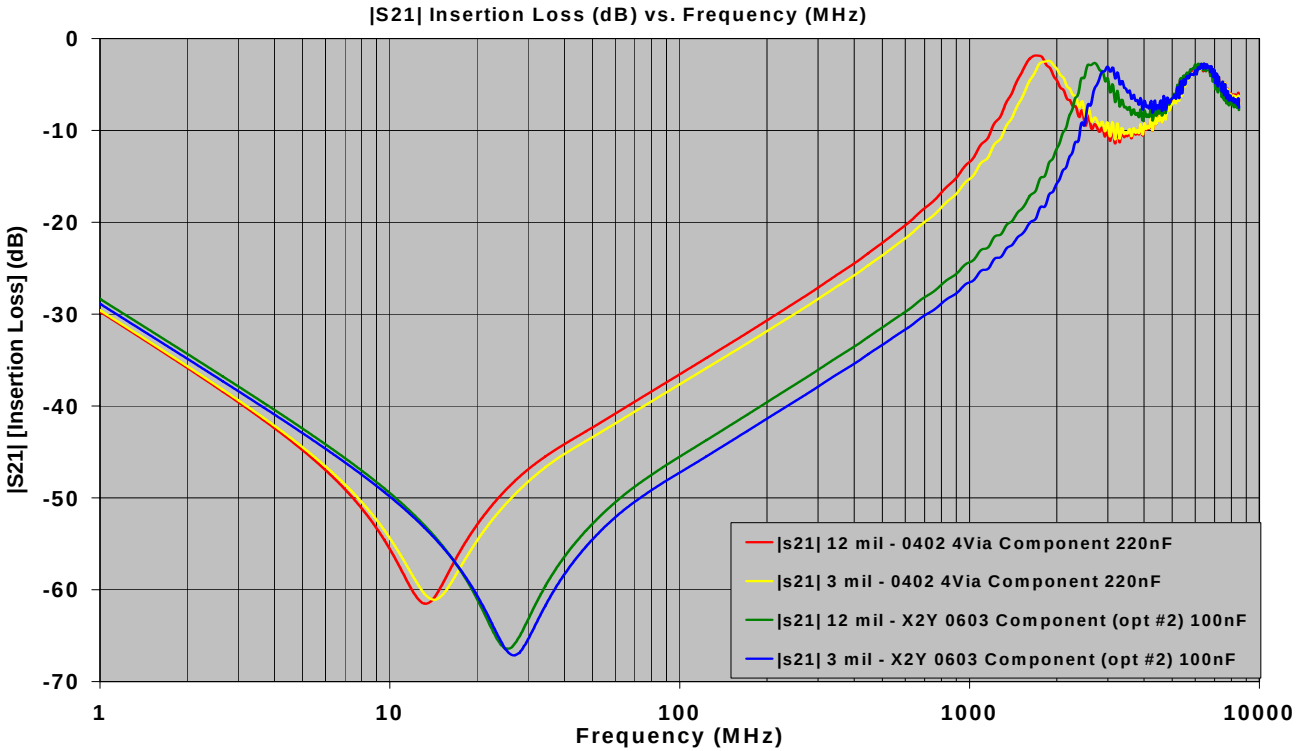
Component Evaluation Techniques

Component-in-System – Component Results

Example Results: 4via 0402, 6 via X2Y 0603
3mil and 12 mil Upper Dielectric



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Component Evaluation Techniques

Component-in-System

De-embedded Test Results X2Y® versus Two and Four Via 0402s

Upper Dielectric Height	Capacitor	C	ESR	ESL			
				LF		HF	
				Value	%	Value	%
3 mils	X2Y® 0603	176nF	10.5mΩ	146pH	1.00	118pH	1.00
	0402 4 Via	193nF	22.1mΩ	547pH	3.75	378pH	3.20
	0402 2 Via	188nF	23.0mΩ	658pH	4.51	452pH	3.83
12 mils	X2Y® 0603	166nF	10.9mΩ	188pH	1.00	154pH	1.00
	0402 4 Via	199nF	20.2mΩ	643pH	3.42	450pH	2.92
	0402 2 Via	201nF	19.6mΩ	807pH	4.29	626pH	4.07

Bypass Capacitor Inductance, Data Sheet Simplicity to Practical Reality, Steve Weir Teraspeed Consulting Group LLC, DesignCon East 2005, TF -7

Component Evaluation Techniques

Component-in-System Fixture

- **The Good**:
  - Low parasitic capacitance < 15pF
    - > High plane / cap PRF >> 1GHz for 0402 caps
    - > Little distortion up to 1GHz, and can be largely deembedded
  - Lower plane 1.5oz Cu effective shield from 2MHz up.
  - Includes via short and pad short sites to deembed instruments and cabling
  - Diamond test coupon limits modal resonances.

- **The Bad**:
  - SMA probe placement on either side of DUT doesn't fully match cantilever relationship of many noise sources.

- **The Ugly:**
  - Costly assembly. Separate fab for each upper dielectric height.

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Component Evaluation Techniques (Summary)

Component-only

- Advantages
  - Accurately measures capacitor
  - Allows for accurate models of capacitor
- Disadvantages
  - PCB structure parameters can be difficult to model.
    - > Component mounting, current loops, via influence, plane stack-up, etc.

Component-in-System

- Advantages
  - More “real world” measurements
  - Allows vias to be included; current path in vias can be difficult to model at H.F. (specifically for multi-terminal capacitors).
- Disadvantages
  - Application specific measurement
    - > Limited to specific parameters – PCB (material & thickness), via size, plane stack-up, etc.

PC Board Design Techniques

- **Understand print circuit board geometry.**

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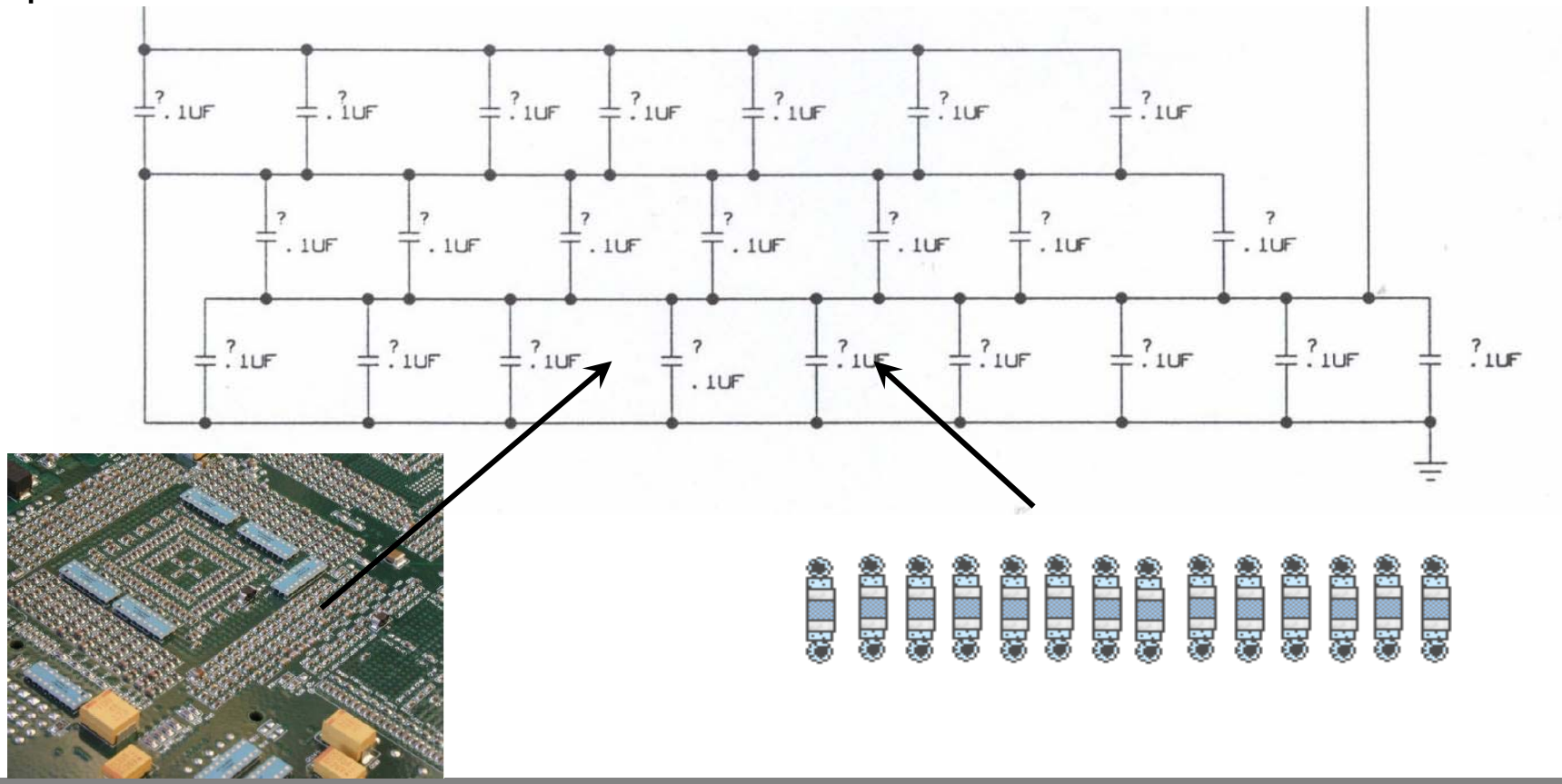
Example of Typical Decoupling Capacitor Arrays

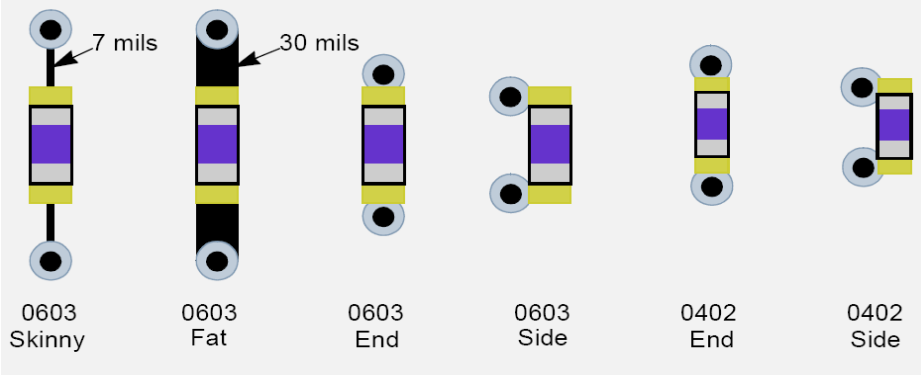
Conventional MLCCs are banked in parallel and consume substantial area on the printed circuit board.



PC Board Design Techniques

Via & Pad Geometries

- Optimized placement and routing of the vias & pads to minimize inductance.
- Considerations should include:
  - Via
    - > Diameter
    - > Length
    - > Location
  - Trace/Pad
    - > Width
    - > Length



Hole Diameter 0.020 inches						
Via length: (inches)	**0603 skinny**	**0603 fat**	**0603 end**	**0603 side**	**0402 end**	**0402 side**
.004	1.51	0.89	0.42	0.33	0.38	0.21
.006	1.66	1.12	0.53	0.38	0.44	0.25
.010	2.13	1.47	0.68	0.51	0.58	0.32
.020	2.68	2.07	1.07	0.67	0.82	0.43
Hole Diameter 0.010 inches						
Via length: (inches)	**0603 skinny**	**0603 fat**	**0603 end**	**0603 side**	**0402 end**	**0402 side**
.004	1.51	0.95	0.50	0.36	0.42	0.26
.006	1.77	1.17	0.59	0.46	0.50	0.32
.010	2.18	1.52	0.77	0.61	0.67	0.40
.020	2.87	2.23	1.16	0.85	1.01	0.60

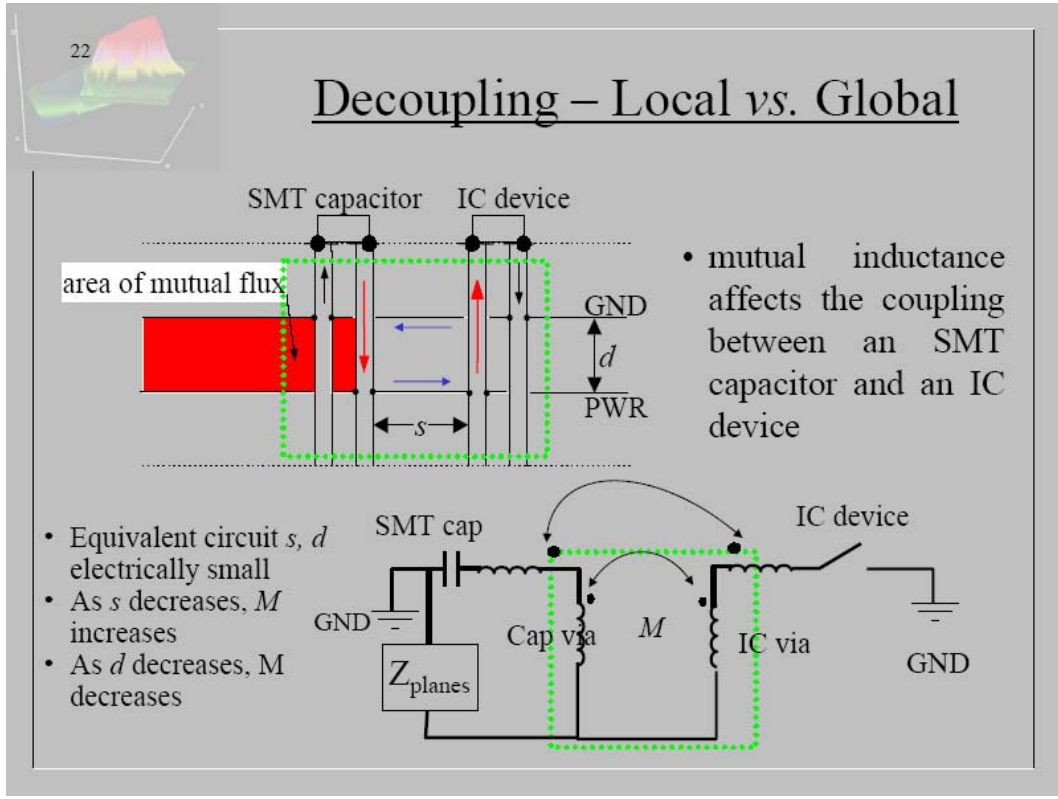
Howard Johnson, PhD, "Parasitic Inductance of a Bypass Capacitor II," HIGH-SPEED DIGITAL DESIGN – online newsletter Vol. 6 Issue 9, Signal Consulting, Inc.

Milliorn, Gary, "Power Supply Design for PowerPCTM Processors," Freescale Semiconductor Application Note AN2447, Rev. 1.1, Sept 2004.

PC Board Design Techniques

Interdigitating Vias

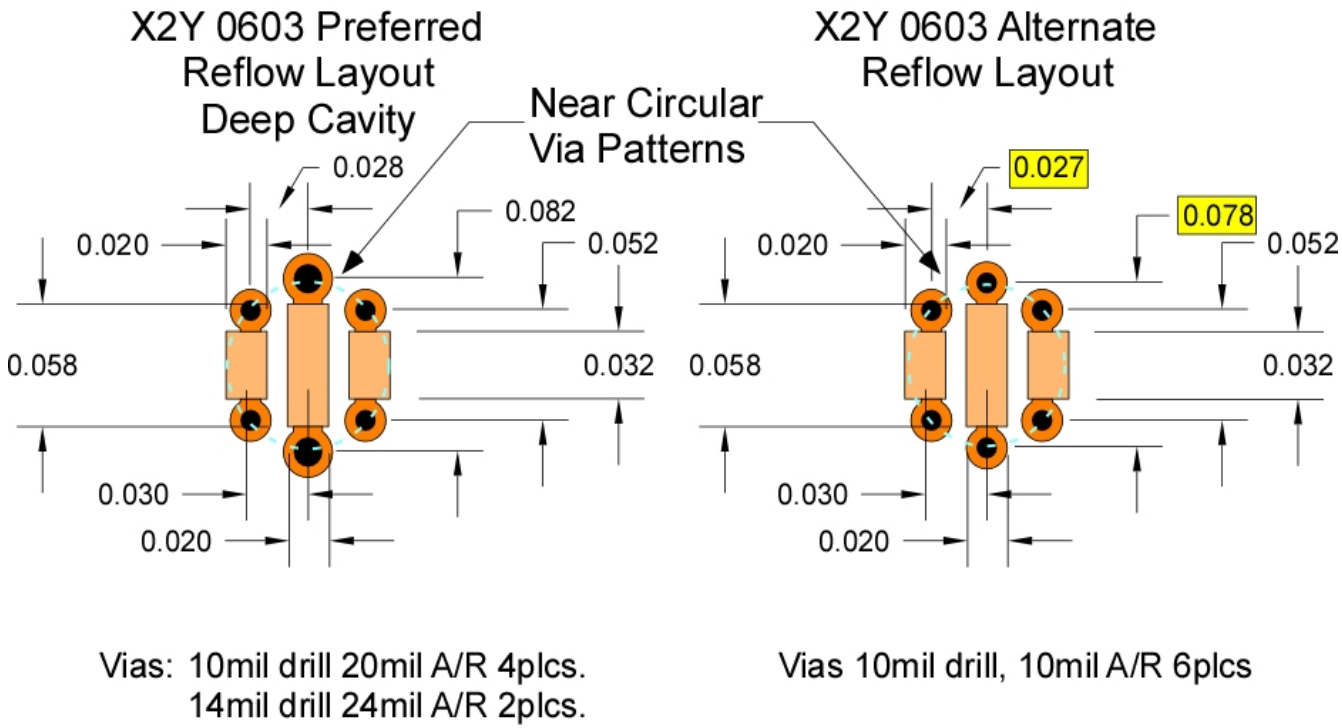
- Maximizing mutual inductance coupling between alternating vias cancels H-field flux, thus lowering over all net inductance of vias.
- Considered “best practice” for vias for capacitors and ICs.
- Minimizing the net inductance of vias allows designers to take advantage of low-inductance capacitor technologies as well as standard MLCC Technology.



James Drewniak, Professor at UMR, “Freescale Presentation - page 22,” Freescale Technology Forum, Orlando, FL June 22, 2005.

Interdigitated Pads/Vias & Low-Inductance Capacitor Technology

X2Y® has developed preferred layouts based on common class II PCB manufacturing rules, and JEDEC rules for high assembly reliability.



Vias: 10mil drill 20mil A/R 4plcs.
14mil drill 24mil A/R 2plcs.

Vias 10mil drill, 10mil A/R 6plcs

PC Board Design Techniques

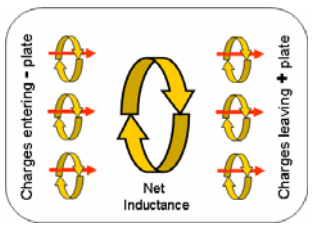
Low-Inductance Capacitor Technology

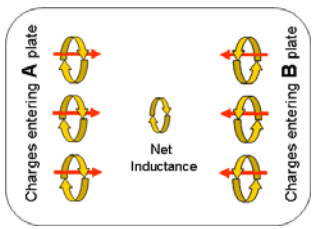
1. **Shorter** current path to ground, therefore smaller current loops.

2. **Dual** current path to ground.

3. **Opposing current flow** internal to the device.

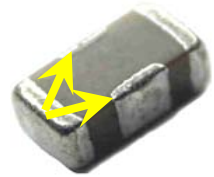
4. **More efficient use of mutual inductance, to lower net ESL.**

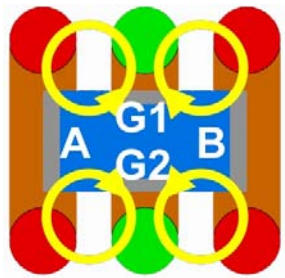




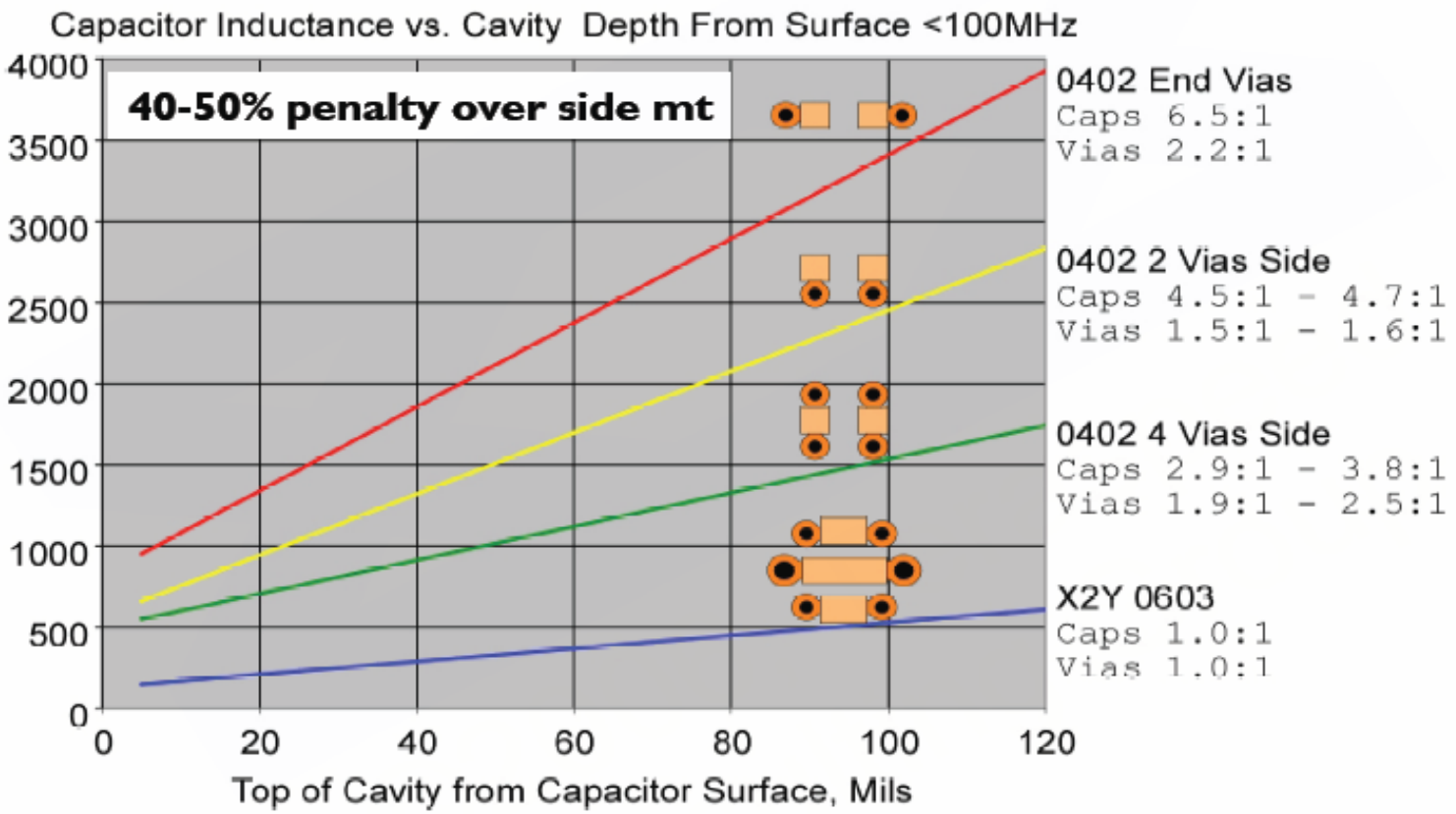
Conventional

X2Y®



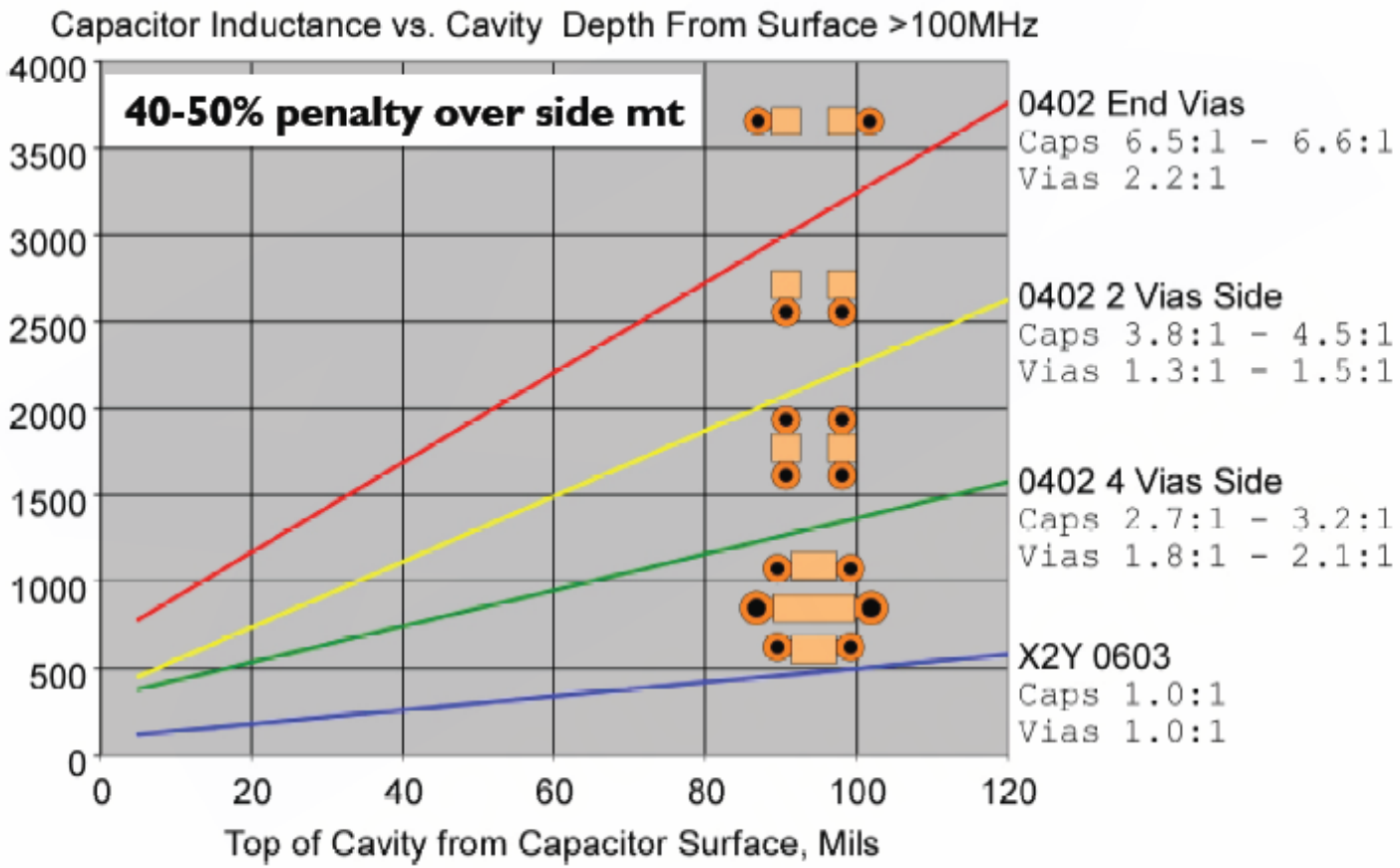


Mounted Capacitor L, <100MHz



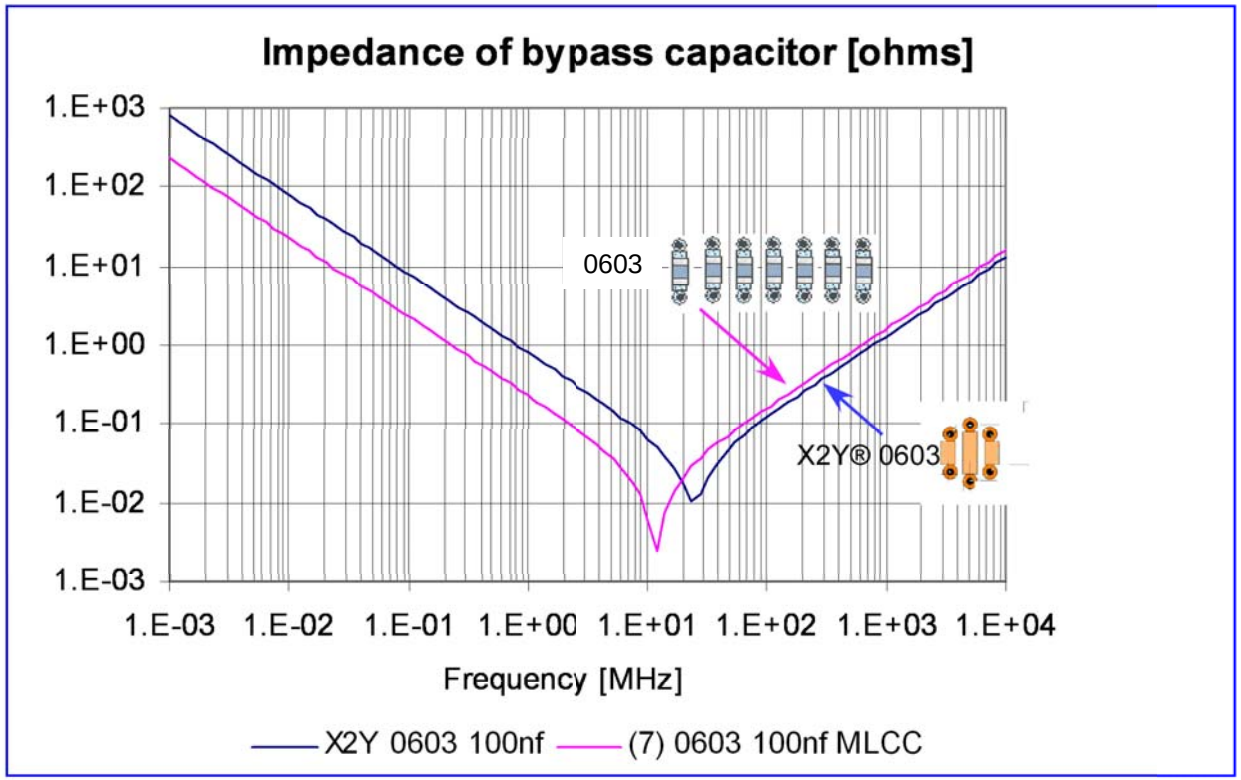
"Impact of PCB Stack-up and Capacitor Via Design In Power Distribution Design," IEEE EMC Society SCV Meeting, Steve Weir, Teraspeed Consulting Group LLC

Mounted Capacitor L, >100MHz



"Impact of PCB Stack-up and Capacitor Via Design In Power Distribution Design," IEEE EMC Society SCV Meeting, Steve Weir, Teraspeed Consulting Group LLC

Benefit of Via Interdigitation and low-inductance Cap Technology



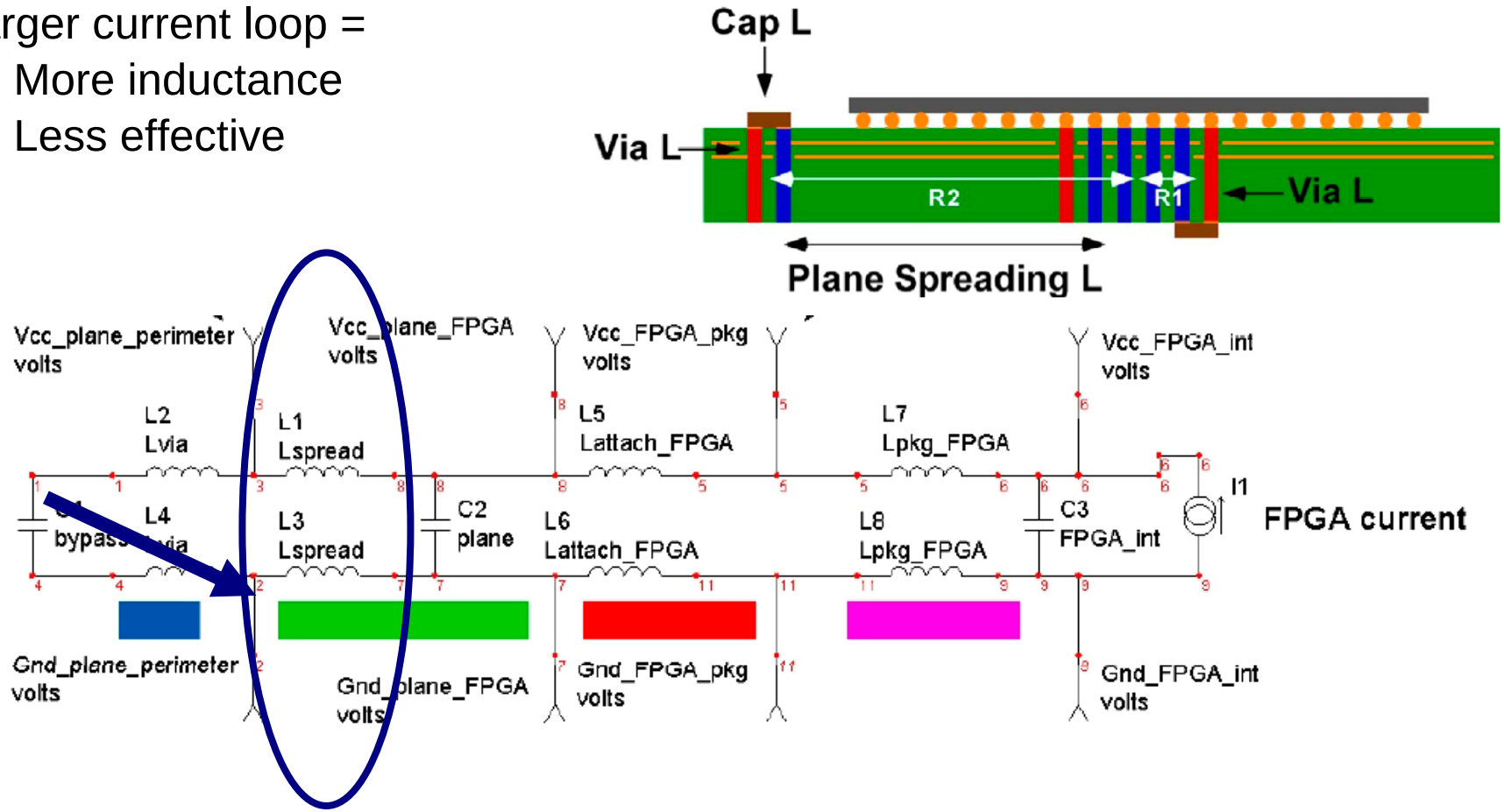
(1) X2Y0603 C2 200nf, 6-vias, dia .010 ", Mounted ESL = 206ph

(7) Std 0403, 100nf, 2-vias mount, dia .010", depth .020",
Mounted ESL (630ph part + 1160ph end mnt = 1790ph)

Simulation using “Bypass.xls” tool by Istvan Novak, Sun Microsystems, http://home.att.net/~istvan.novak/tools.html

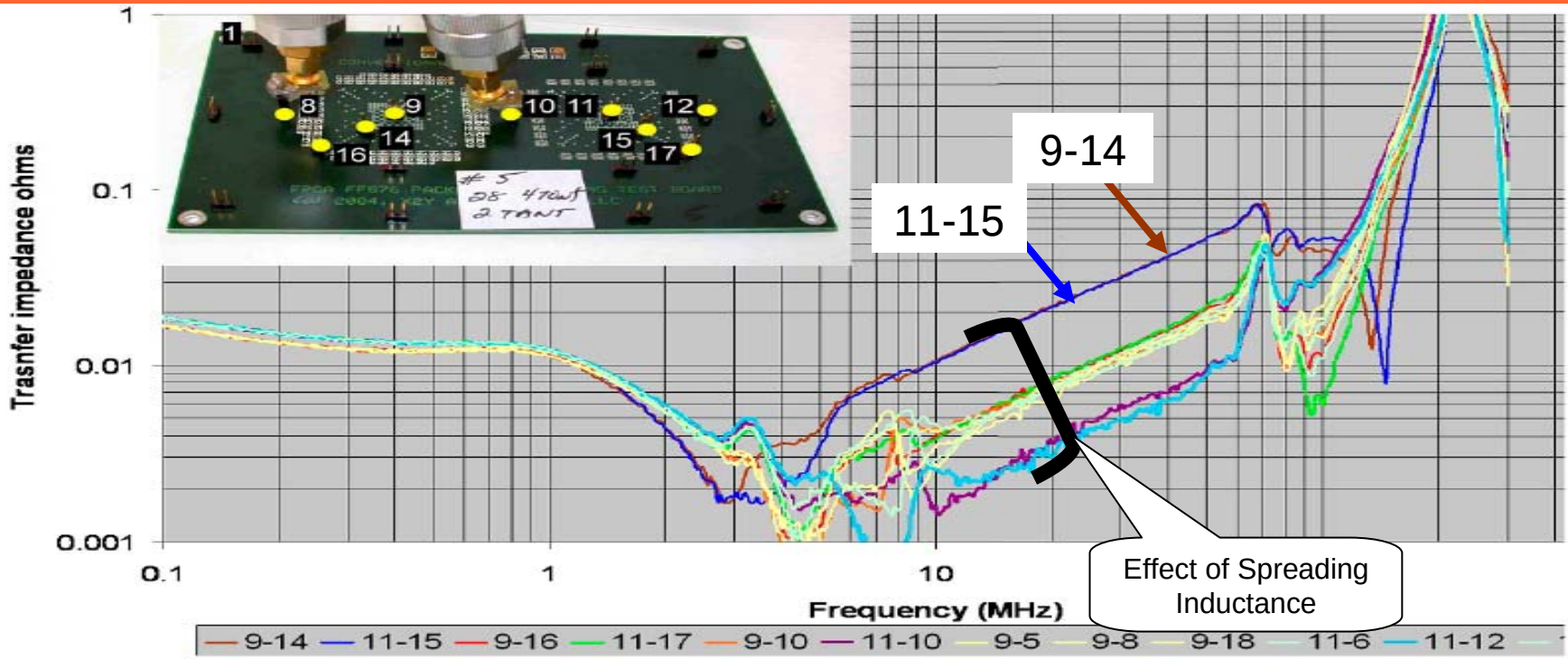
Physical Distance between IC and Cap (Spreading Inductance)

- Larger current loop =
  - More inductance
  - Less effective



Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

PC Board Design Techniques



Effects of spreading Inductance in PDS

- Using position 9 & 11 as I/O & core power position the effects of spreading inductance in the planes can be seen.
- Demonstrates why measuring across a cap for capacitor-in-system measurement isn't accurate.

Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

Spreading Inductance – Example of Effect

fco	5.00E+07
cap ESL	500
cap via space	0.05
cap vias	2
cap mtd L	982
attach L	10
Lspread 1"	27
Lspread 5"	46

Virtex2/Pro Core Power

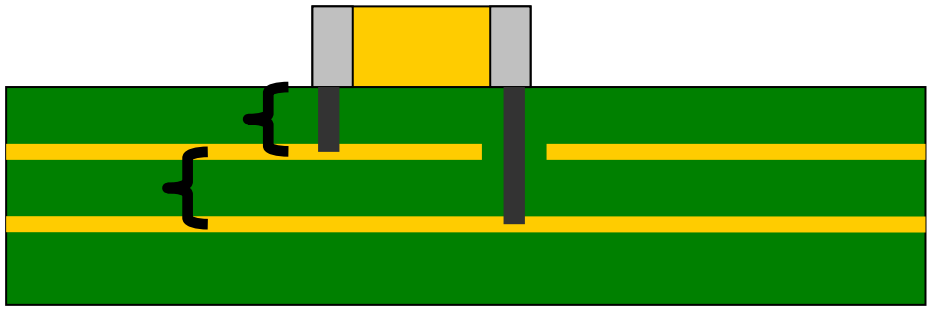
S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
…	

Ztarget mohms	100	50	40	30	25	20	18	16
Lbudget pH	318	159	127	95	80	64	57	51
Radius "								
1	4	9	11	17	23	37	48	70
1.2	4	9	12	18	25	40	54	82
1.5	4	9	12	19	26	45	63	105
2	4	9	12	20	29	53	80	163
3	4	9	13	22	33	71	129	781
5	4	10	14	25	42	124	613	9999
Lattach+Lspread	12%	23%	29%	38%	46%	58%	64%	72%
Cap increase	0%	11%	27%	47%	83%	235%	1177%	14184%

- @ Low performance, capacitor position does not matter.
- As performance increases, position becomes increasingly sensitive.
- Near 50% Lattach + Lspread, 1”-1.5” yields only 10% penalty.

IEEE Presentation by Steve Weir, Teraspeed® Consulting Group LLC, ;“Does position matter? Locating bypass capacitors for effective power distribution and EMC control”

PC Board Plane Stack-up



- Plane stack-up, depth, and height are difficult to define for every circumstance, application, and PCB manufacturer, however the location of the power and ground planes directly affects:
  - Capacitor – IC loop area
  - Spreading Inductance
  - Mounting Inductance
  - The number of Caps need to meet target impedance.

PC Board Design Techniques (Summary)

Things to consider in PC Board Geometries

- “Best Practice” Via and pad geometry
- Interdigitating Vias
- Minimizing Capacitor – IC loop area
- Minimize Spreading Inductance
- Minimize plane depth from IC – Capacitor layer if possible

Optimizing The Power Distribution System

- Reducing system noise.
- Reducing capacitors, via's, PCB area.

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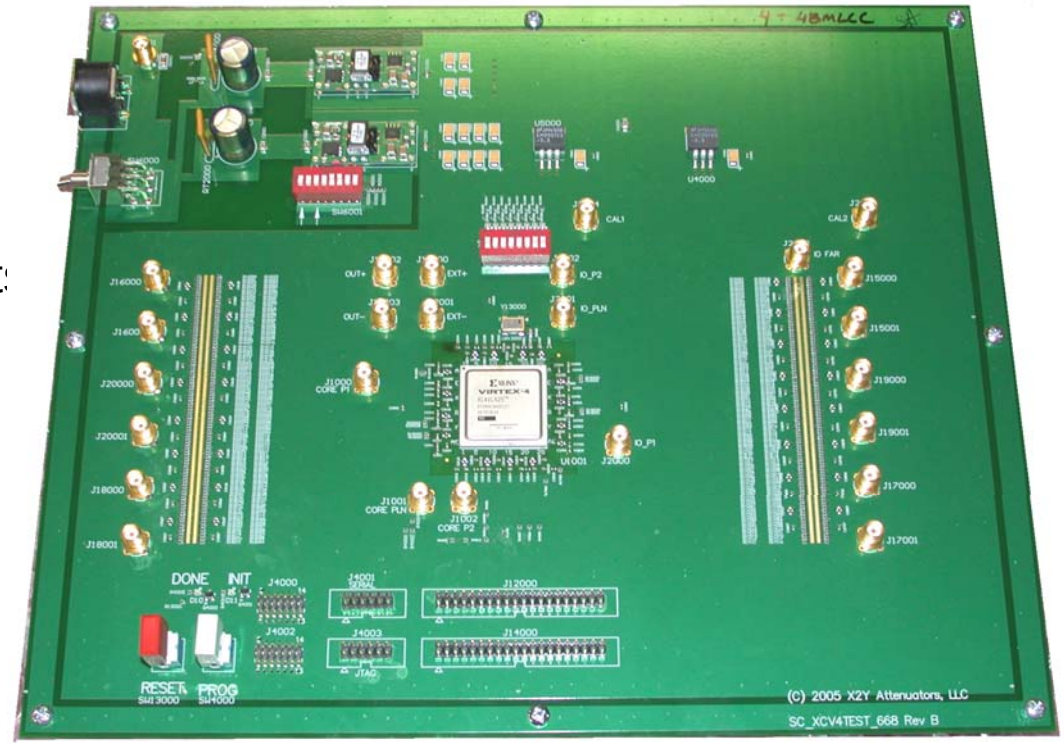
Optimizing The Power Distribution System

Demonstration board designed by Steve Weir as shown in video production by Dr. Howard Johnson titled: "*Low Inductance Capacitor Packages*".

- X2Y bypass performance is compared to conventional two terminal capacitors using an active FPGA circuit:
  - Network analyzer measurements
  - Oscilloscope transient measurements



Optimizing The Power Distribution System

- VCCIO Outside Capacitor Ring
  - Indicates noise transferred to rest of PWB, and EMI
  - Most proportional to capacitor performance
    - > Performance not compressed by plane spreading Inductance
  - Plane cavity height and perforation limits impedance to device attachment
- I/O supply for target device does not have caps under device lid.
  - PCB must support I/O switching currents through entire B/W
  - Low impedance ⇔ Low inductance
- Stack-up optimizes I/O:
  - Power plane on layer 2
  - Vss plane on layer 3
  - Vss flood on surface outside BGA break-out
  - Lowest inductance between BGA substrate and I/O power plane
  - Lowest inductance between I/O power plane and bypass caps

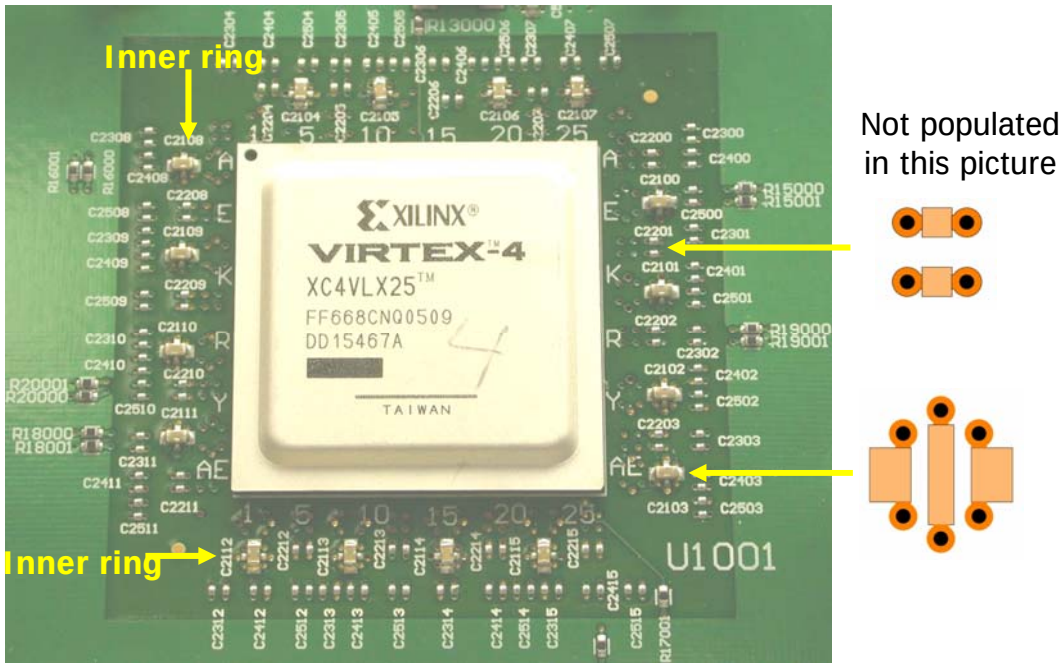
Optimizing The Power Distribution System

- Additional Measures for high performance
  - Singulated planes
    - > Raise power resonant frequency as high as possible
      - – Frequency depends on mounted inductance
- Virtex 4 FPGAs
  - Rise/fall times of 0.4ns through mid-band region
  - Little energy above 1GHz
  - Makes well-behaved power system easier to realize
  - I/O prioritization in upper planes is CRITICAL
    - > Large V4 parts w/internal caps still rely substantially on planes / external caps for support and do not escape this requirement
    - > Parts like StratixII w/o internal caps MUST be affixed with I/O power closest to the part.

Optimizing The Power Distribution System

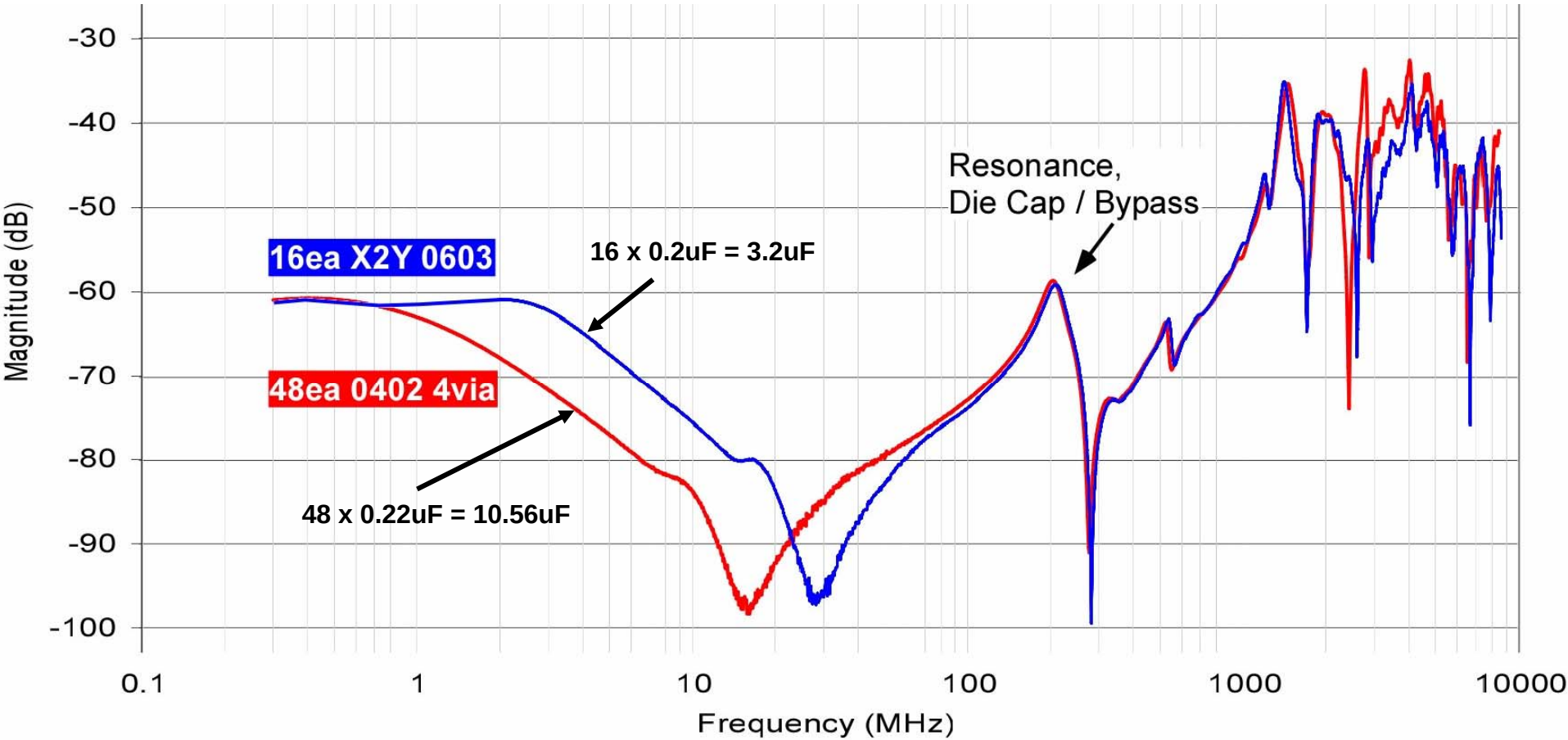
Capacitor Layout on PC Board

- Inner ring capacitor population consists of either 16 ea X2Y population OR 16 ea 0402 population
  - 0402 4via mounts, near zero SM dam allowance
- Outer ring capacitor population can accommodate up to 48 ea 0402s



Optimizing The Power Distribution System

Transfer Impedance Active Test Card

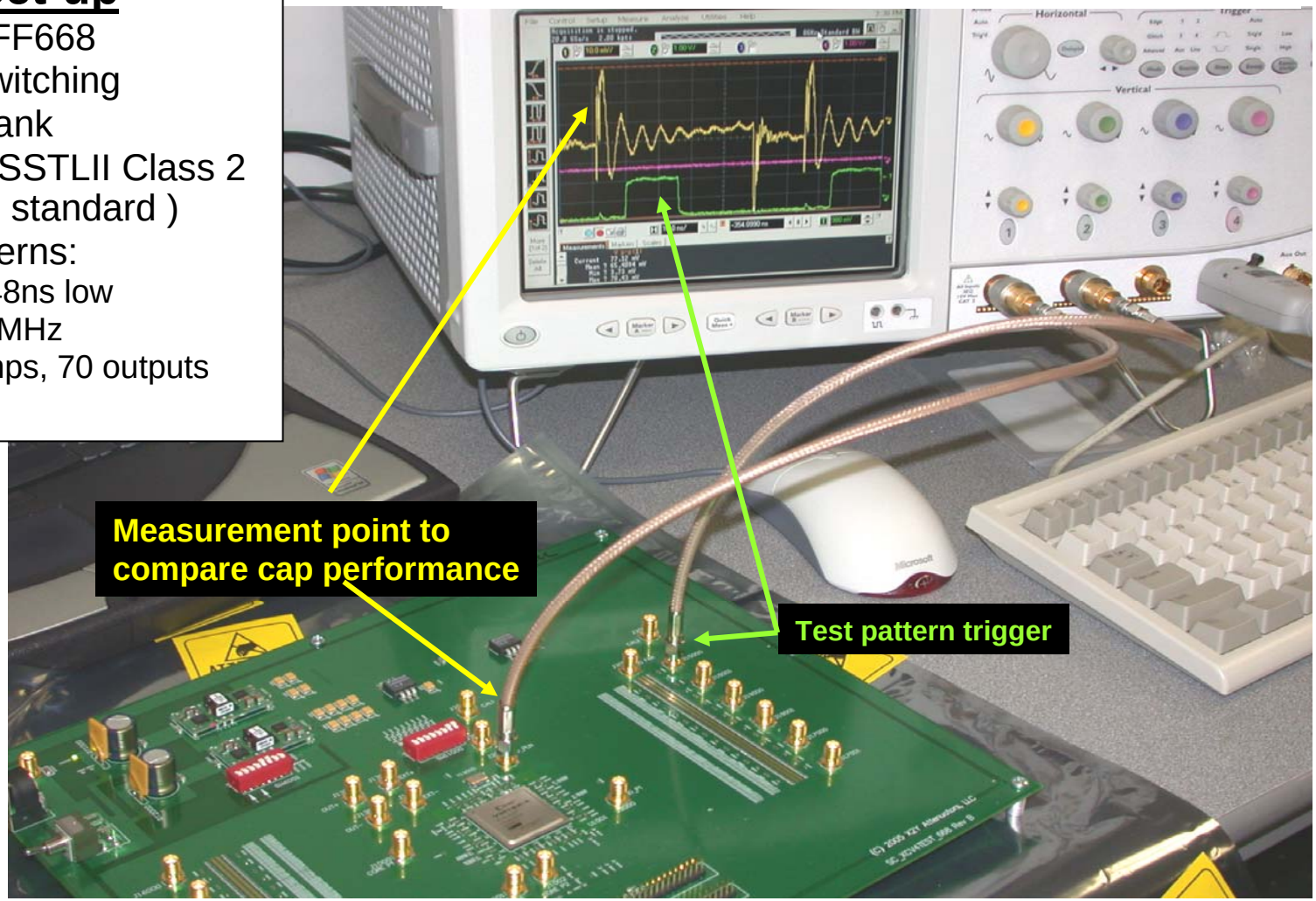


Optimizing The Power Distribution System

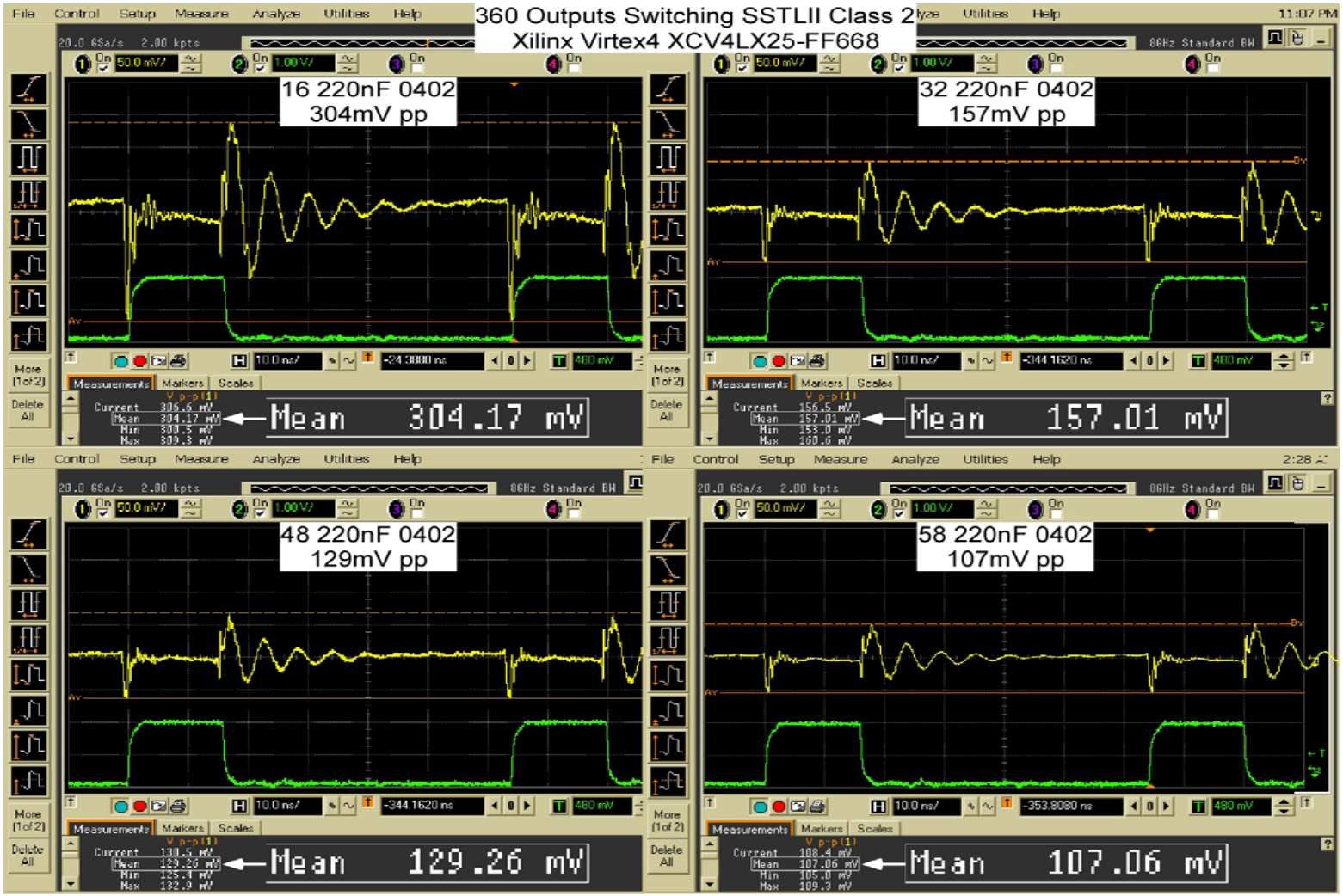
Active Test Set-up

- Virtex 4 LX25 FF668
- 1 – 6 Banks Switching
- 60 Outputs / Bank
- Outputs set to SSTLII Class 2 (DDR RAM I/O standard)
- Three test patterns:
  - 16ns high / 48ns low
  - PRBS5, 125MHz
  - PRBS, 250mps, 70 outputs switching

Agilent DSO81204A Infinium 12 GHz 40GS s/a

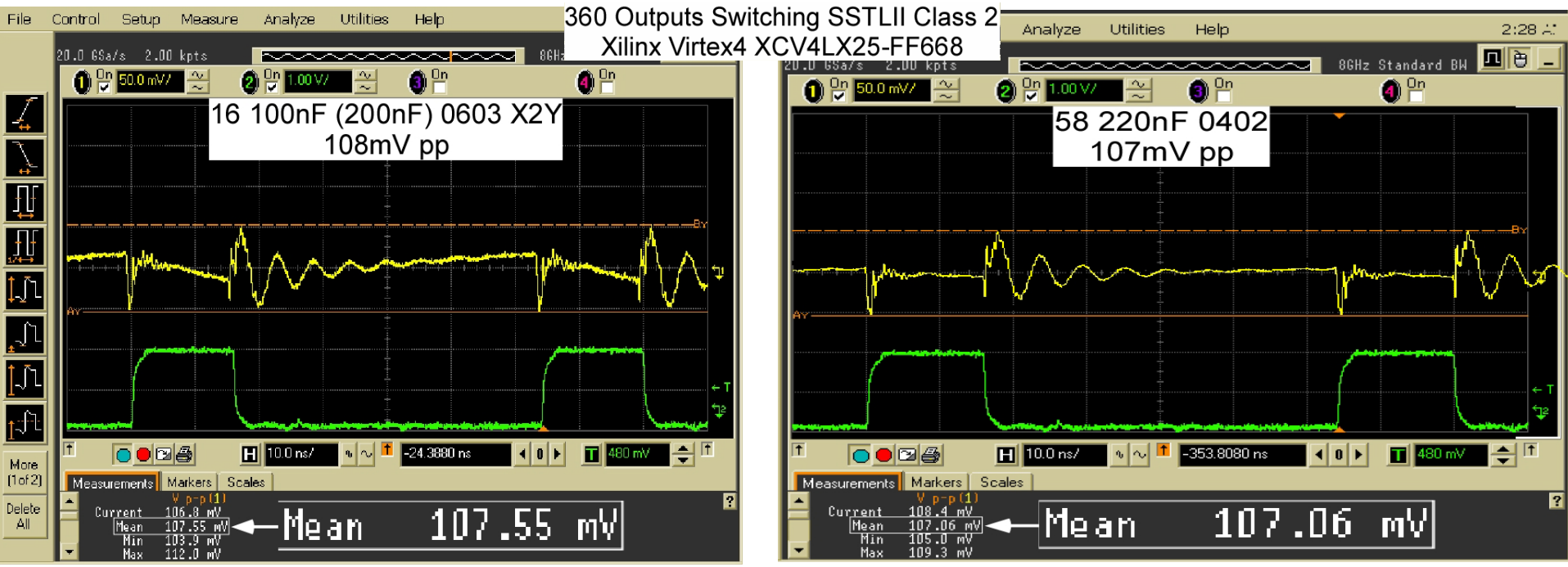


Optimizing The Power Distribution System



Optimizing The Power Distribution System

- **16** 0603 X2Ys match pp noise of **58** 0402s
  - **96** Vias total X2Y, **232** Vias total 0402
- **3.6:1** Capacitor ratio, **2.4:1** via ratio



Optimizing The Power Distribution System (Summary)

16 X2Y w/ 96 vias total deliver:

- Just 36% the noise of 16 0402 caps even when 0402s use 4 aggressively mounted vias
  - Improved IC Power Delivery
  - Improved Vtt Power Delivery
- Less noise than 48 0402 caps using 192 vias
- **Matched noise of 58 0402 caps using 232 vias**
  - **3.6:1 Capacitor Ratio**
  - **2.4:1 Via Ratio**

Optimizing The Power Distribution System (Summary)

X2Y Attenuators, LLC will distribute a free copy of the newly released SiLab training video; “Low Inductance Capacitor Packages” produced by Dr. Howard Johnson.

In the video, Dr. Johnson explains the importance of low-inductance capacitor structures and shows how they affect real digital systems.

The film demonstrates proper measurement of capacitors and shows comparative results of low inductance capacitors vs. ordinary capacitors on test fixture cards. There are also several performance demonstrations using an “active” FPGA demo board commissioned by X2Y Attenuators, LLC and developed by Steve Weir of Teraspeed® Consulting LLC.

Important design topics covered in the video include:

- How to determine and minimize bypass current loops.
- Where to place power and ground planes in a PCB stack-up.
- Metrics used to evaluate the advantage of low-inductance capacitors in designs.
- Best practices when mounting bypass capacitors and the impact of positioning on the printed circuit board.
- Animated Illustration of distributed plane behavior contributed by Dr. Bruce Archambeault.