DesignCon 2005
High Performance FPGA Bypass Networks

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From DC to Near Daylight

Bypass networks in four (easy???) steps:

- Determine the AC noise voltage budget
  - Easy, mfg spec sheet. But at the part.
- Determine the AC noise current vs. Freq
  - Application dependent. Not so easy.
- Derive |Z| vs. Freq.
  - $|Z| < dv/dt / di/dt$
- Design the physical layout and bypass network accordingly

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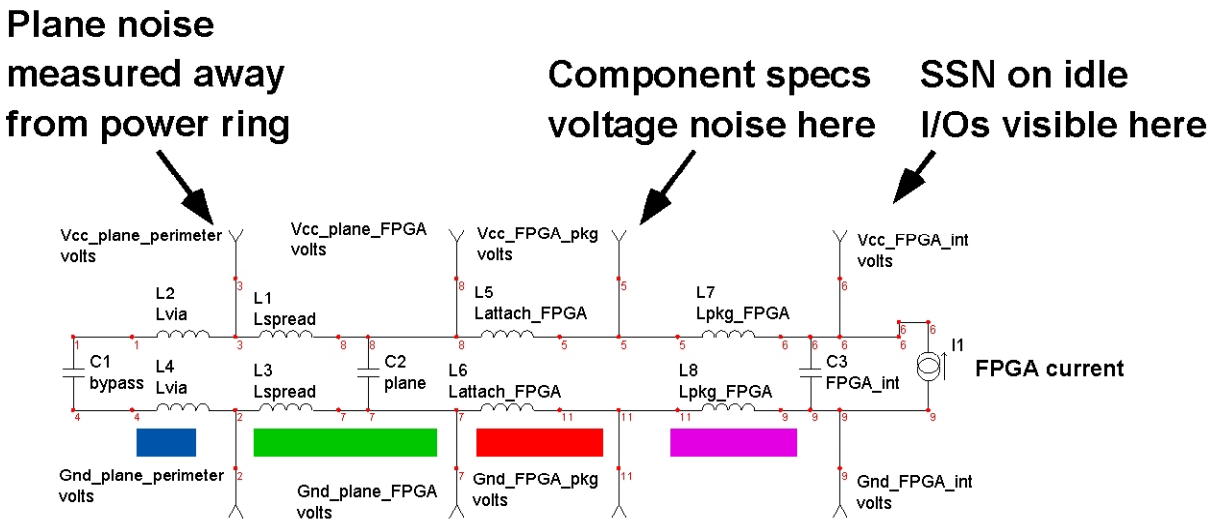
Shunt Path



FPGA attachment, plane spreading, and capacitor attachment via inductance all work to decouple the bypass capacitors from the FPGA.

The IC attachment vias, plane spreading inductance, and attached bypass capacitor inductance all impede the shunt.

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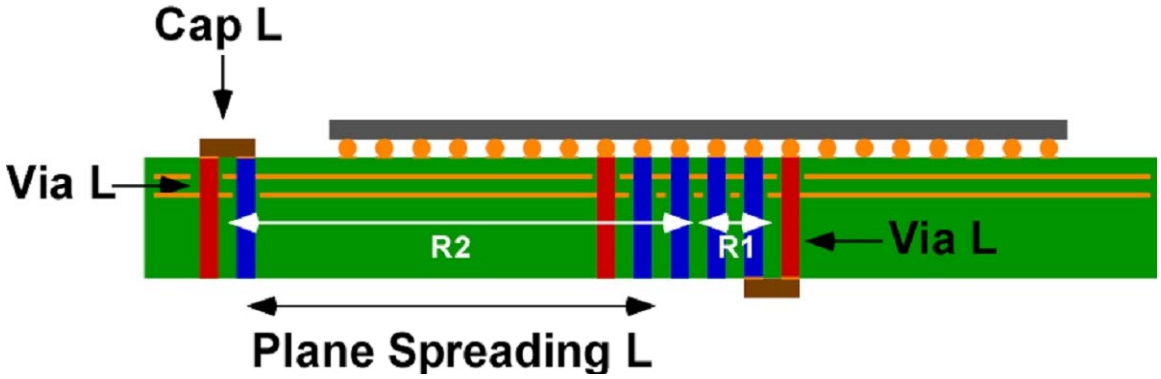
Spreading Inductance



- For simple power / ground patterns, spreading inductance may be readily determined by application of the Biot-Savart law.
- Radial spreading inductance:

$$u_0 */2\pi * H * \ln(R2/R1)$$

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Spreading Inductance

$$u_0*/2\pi * H * \ln(R2/R1)$$

u_0 is the permeability of free space, 31.9nH/square.

H is the plane separation in same units as R1, R2.

R2 is the radius from the die center to the bypass capacitor vias.

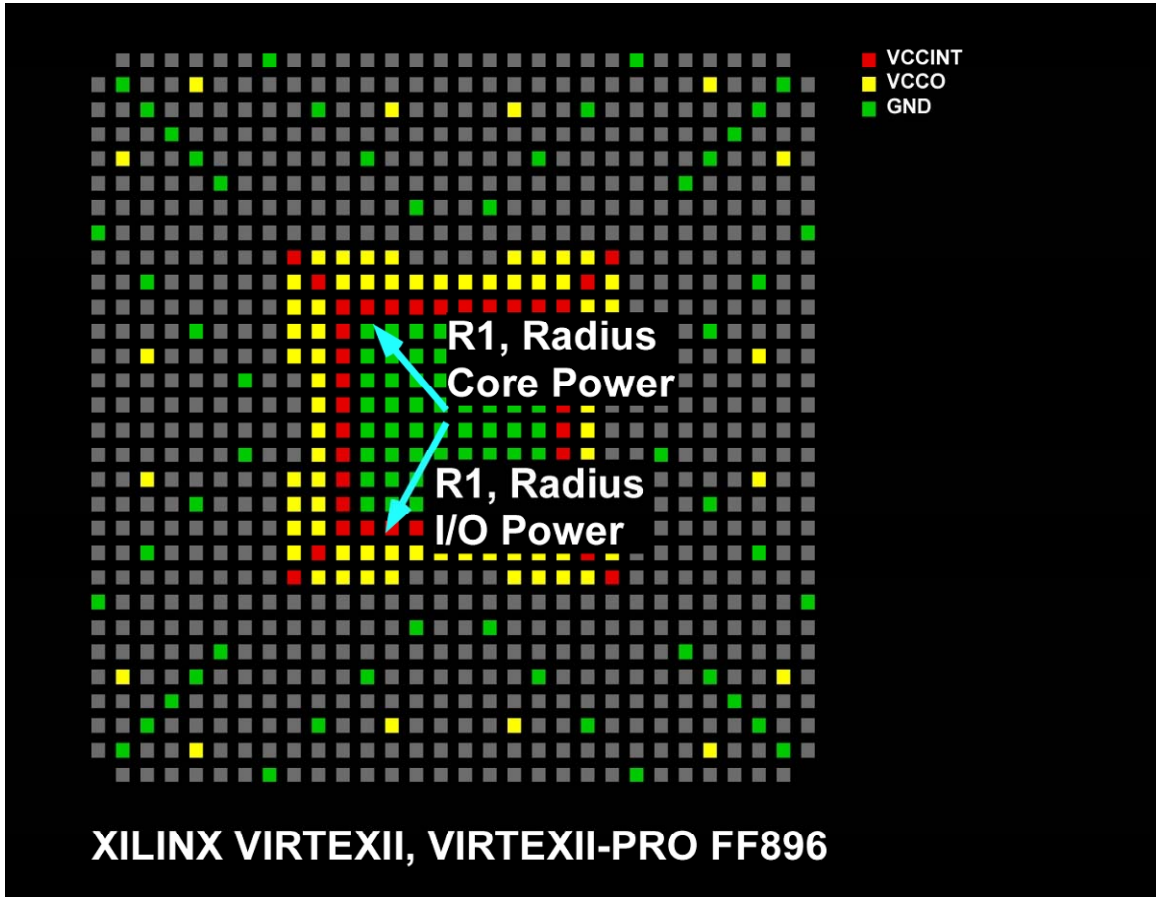
R1 is the radius from the die center to the IC power / ground vias

Spreading Inductance

Spreading Inductance depends on

- The **ratio** of the radius from die center to bypass capacitor attachment vias, vs the radius to the IC power / gnd attach
- Plane separation
- Plane perforation

FPGAs w/ Power / Gnd Slug



VirtexII, VirtexII-Pro locate most ground and power at the package center.

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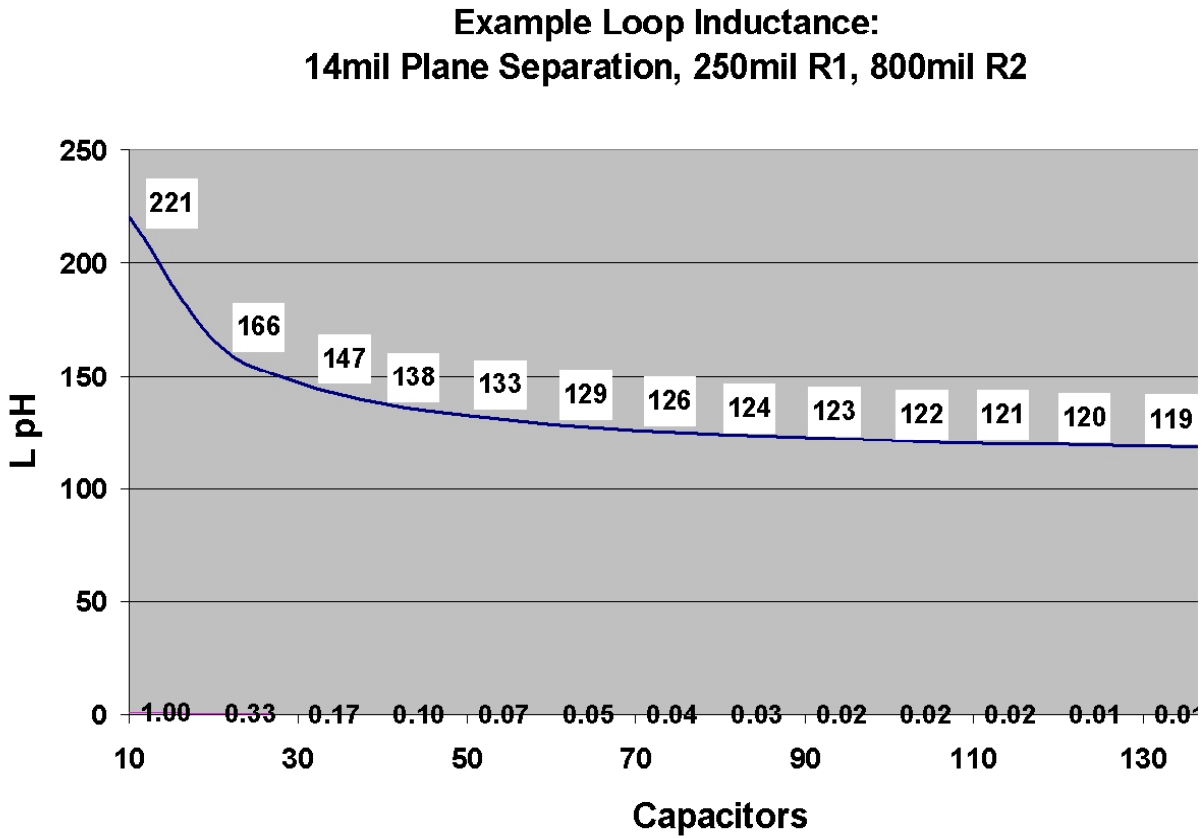
FPGAs w/ Power / Gnd Slug

- Including perforation effects, for 20 mil antipads, V2/Pro result in 7.4pH / mil plane separation to a capacitor ring located 1" from the device center.

- With 30 mil antipads, this number rises to over 12pH / mil.

Spreading Inductance Limitations



- Spreading inductance limits the effectiveness of bypass capacitor arrays

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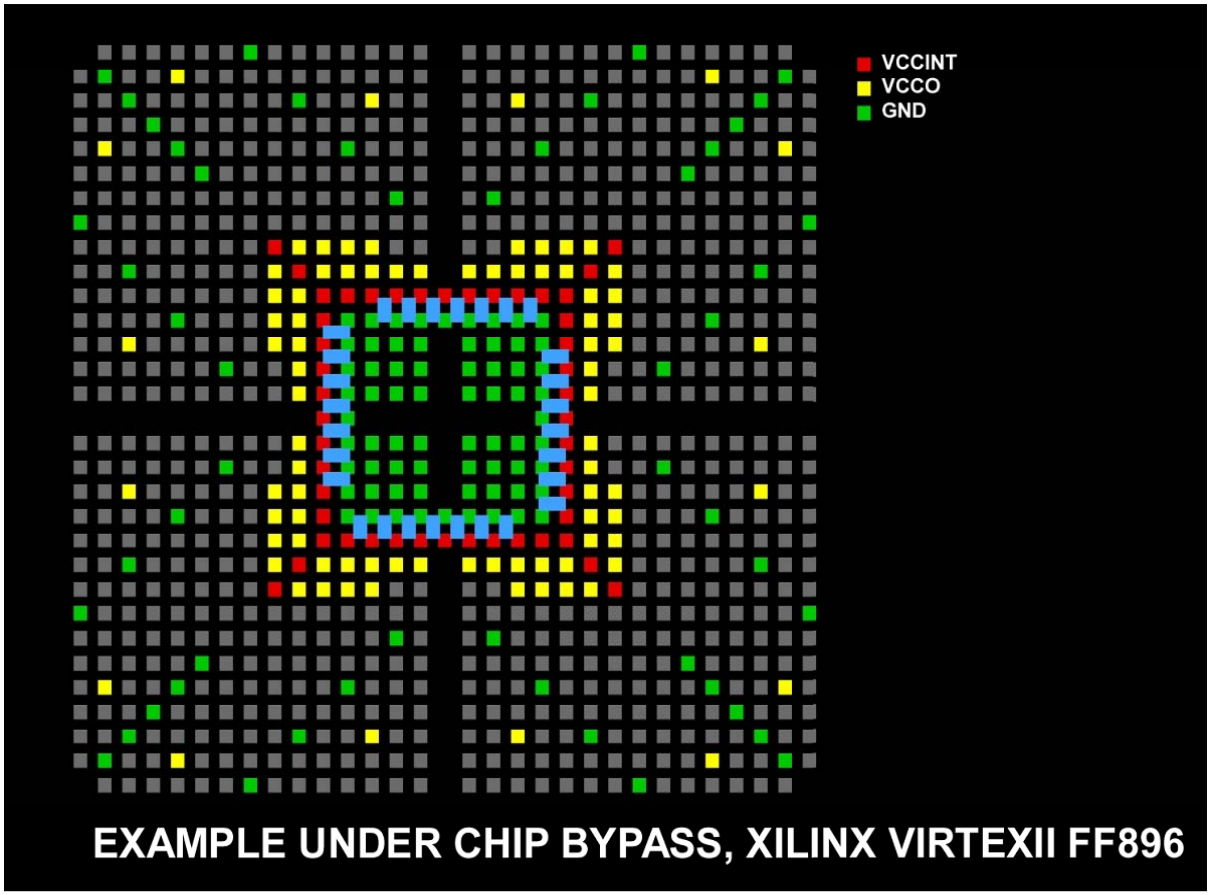
BackSide Capacitors



- Backside capacitors at the power / gnd ring trade via depth for radius

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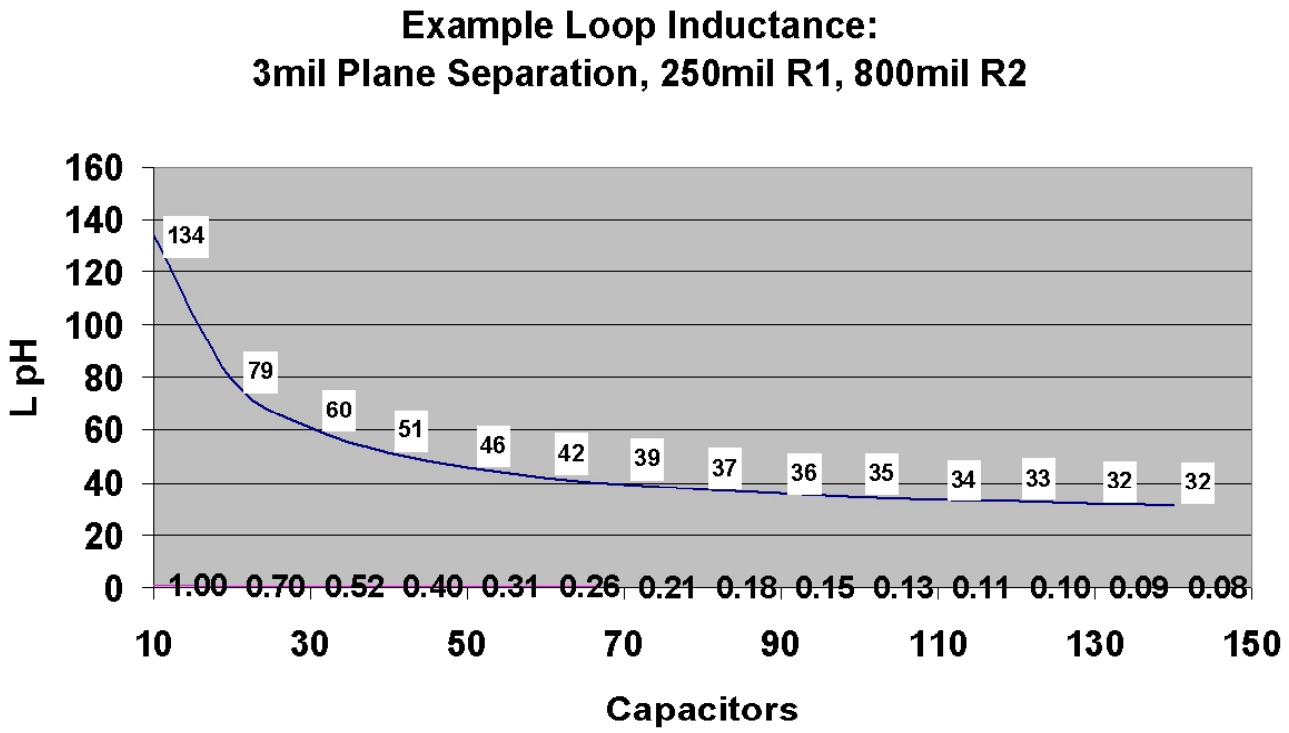
Dedicated Power / Gnd Planes



- Dedicated pwr/gnd = dramatic improvements
- Up to 40 ordinary capacitors effective

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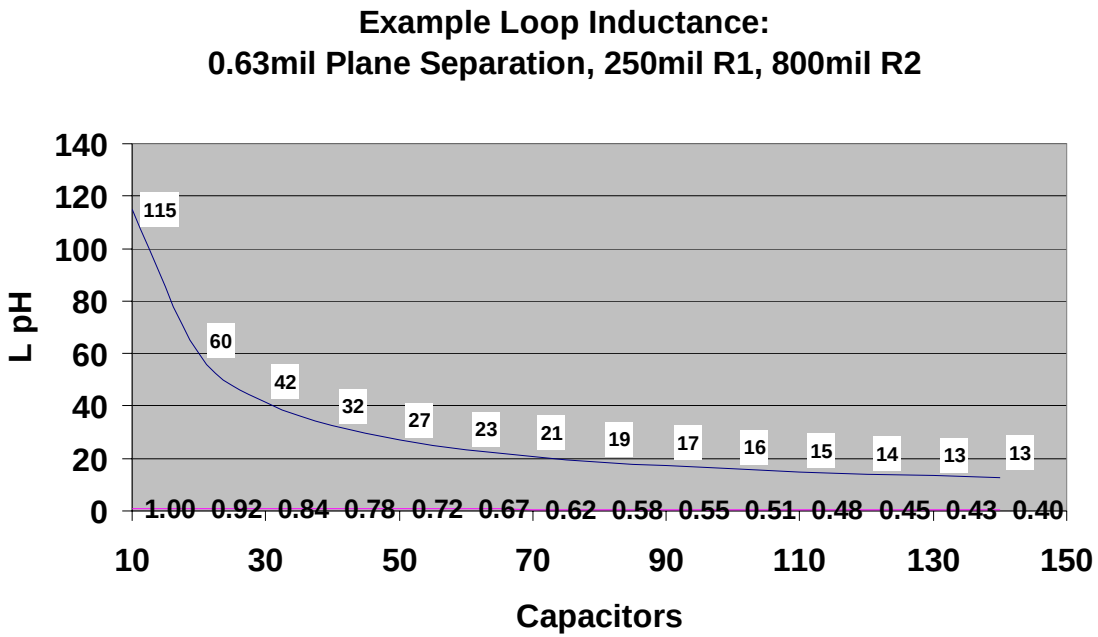
Dedicated Power / Gnd Planes



- The thinner the dielectric the lower the impedance floor, and the more capacitors can be effectively used.

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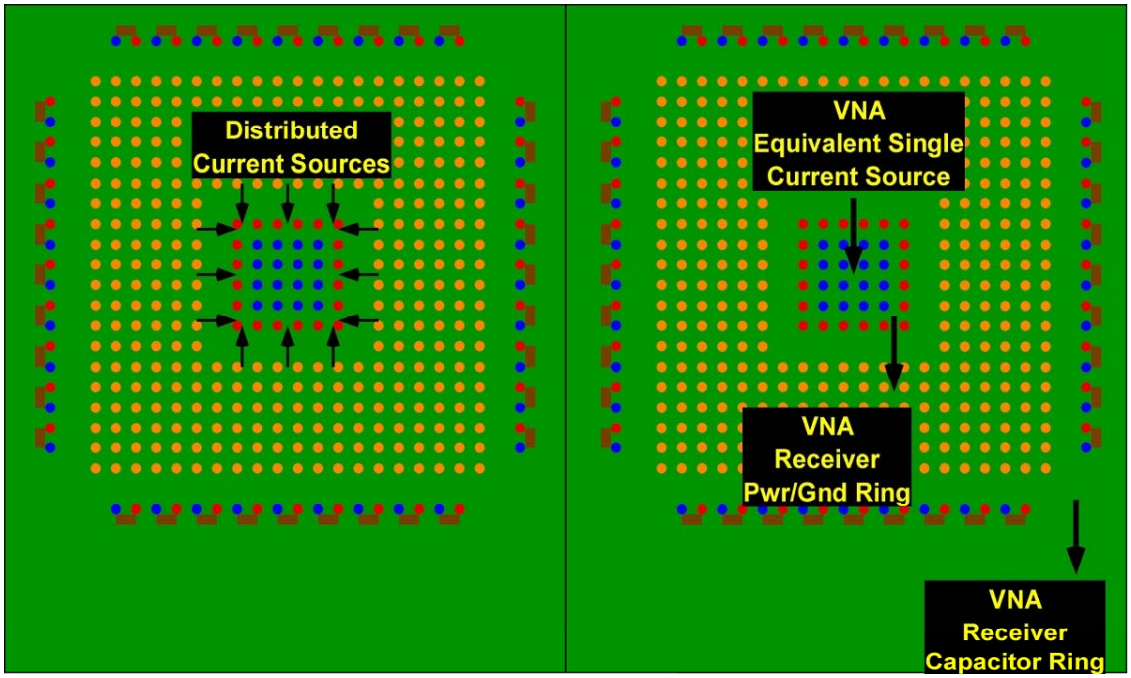
Spreading L Demo Fixture



- Distributed current sources modelled as single center source
- VNA receiver @ gnd/pwr ring "sees" IC impedance.

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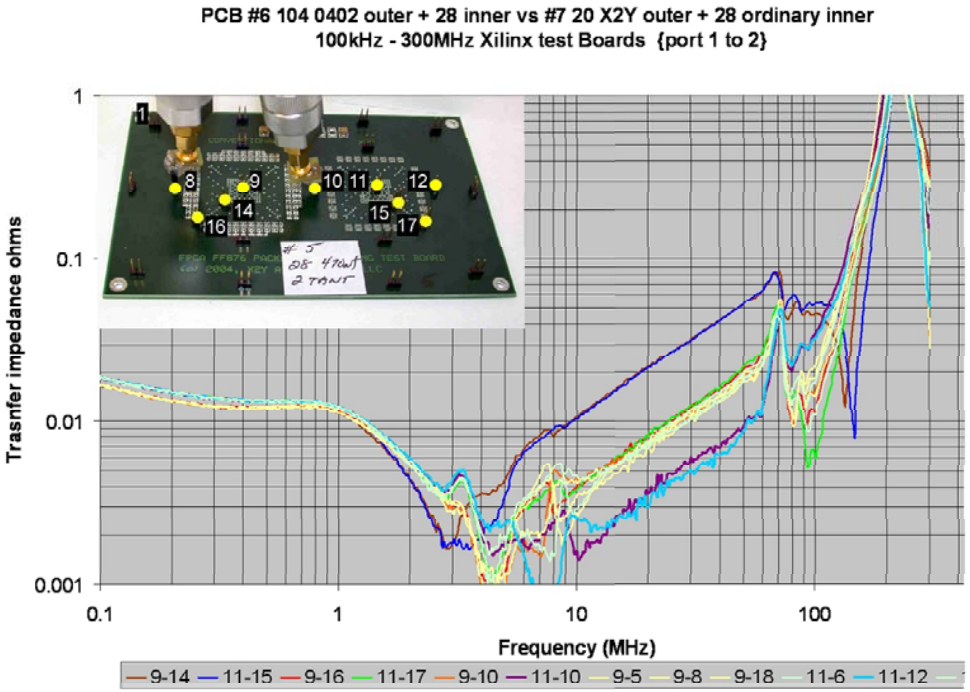
Spreading L Demo Fixture



- FPGA pwr/gnd xfer |Z| is 4X |Z| @ BGA perimeter
- Low ESL X2Y caps exhibit much lower local |Z|.

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Via Inductance

- Two components:
  - Between the planes, this is the entire cavity
  - Above the topmost plane in the cavity

$$5.08\text{nH} * ((H_1^2 * (2 - K_1) / (S * K_1)) + (2 * H_2 * \ln(2 / K_1)))$$

H_1	Via length above the uppermost plane
H_2	Plane to plane separation
D	Via diameter
S	Via separation, on centers

Capacitor ESL

- Geometry defined.
  - Smaller is usually better
  - Must consider attachment vias.

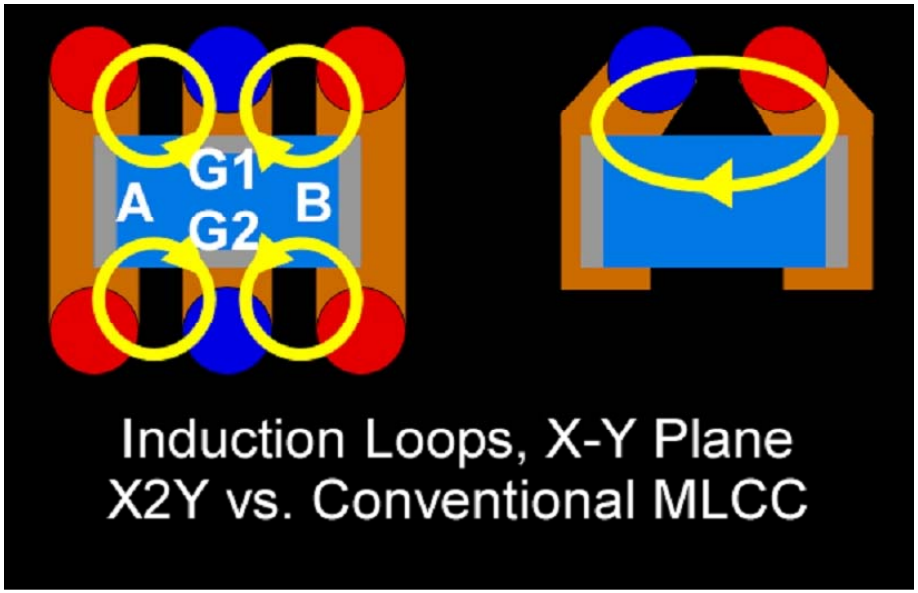
$$5.08nH * ((H_1^2 * (2 - K_1) / (S * K_1)) + (2 * H_2 * \ln(2 / K_1)))$$

H_1	Via length above the uppermost plane
H_2	Plane to plane separation
D	Via diameter
S	Via separation, on centers

K1 = D/S

The X2Y Capacitor

- Unique device, terminals on all sides.
- Four, very small current loops.



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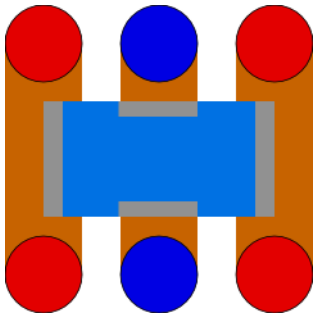
The X2Y Capacitor

- **ALWAYS** attach with **SIX** vias.
  - Imperative to form small induction loops in the X-Y Plane
- Typically replaces 4 – 5 ordinary capacitors.
- In practice always replaces **at least three** ordinary capacitors.



$$N = 2.7 * (L_{CONV\_ESL} + L_{VIA\_PAIR}) \; / \; (162pH + L_{VIA\_PAIR})$$

For $L_{VIA\_PAIR} >> L_{CONV\_ESL}$, N has a lower limit at 2.7.

For $L_{VIA\_PAIR} << L_{CONV\_ESL}$, N approaches $L_{CONV\_ESL} / 60pH$.

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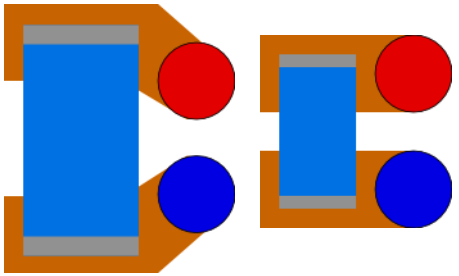
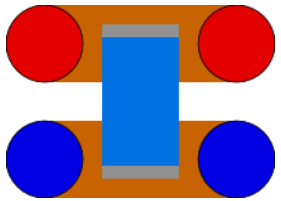
Strategies for Conventional Caps

- 0402 capacitors
  - Good for space reduction and $$$
  - Improvement vs. 0603 for short vias



- Two vias / pad reduces inductance.
  - Effective only for long vias
  - Always increases total via count



	Capacitors on Component Side					Capacitors on Back side[1]		
H1	0.005	0.020	0.005	0.020	0.005	0.005	0.005	0.005
H2	0.014	0.003	0.003	0.001	0.001	0.014	0.003	0.001
S	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03
D	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
K1 D/S	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33
L / via pH	318	393	76	217	40	1580	1530	1540
L mounted	718	793	476	617	439	1980	1930	1940
Total Caps	0.71	0.67	0.86	0.74	0.92	0.56	0.56	0.56
Total Vias	1.42	1.34	1.73	1.48	1.84	1.11	1.12	1.11

Examples: 2Via / Pad 0402 One Via / Pad 0402 0.062" Board

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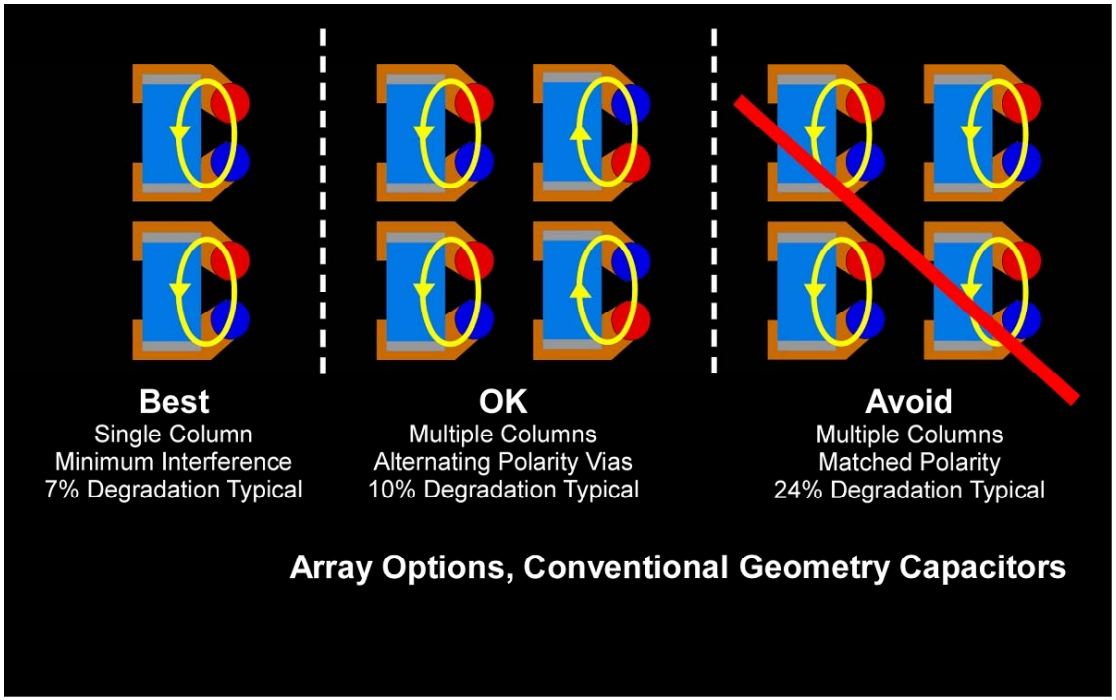
Mutual Coupling in Arrays

- Capacitor arrays couple, increasing the effective inductance of each capacitor and its attachment vias.



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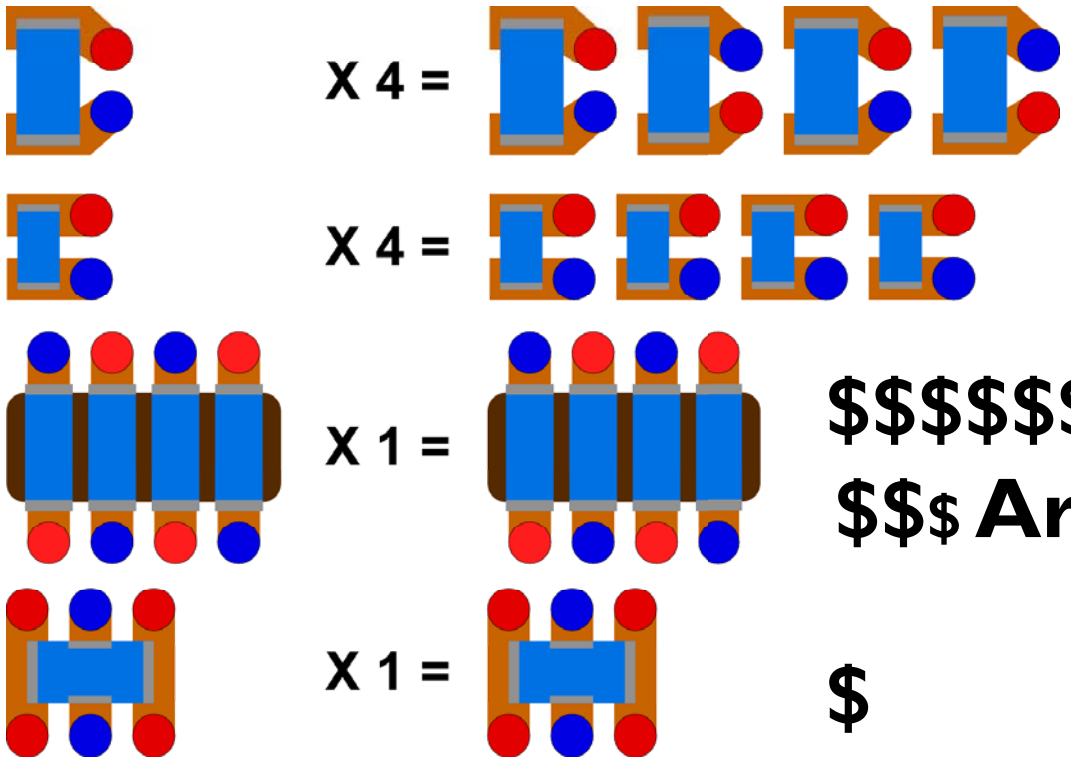
The PCB Bypass Landscape



Raw capacitor cost + placement + via holes

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Capacitor SRF

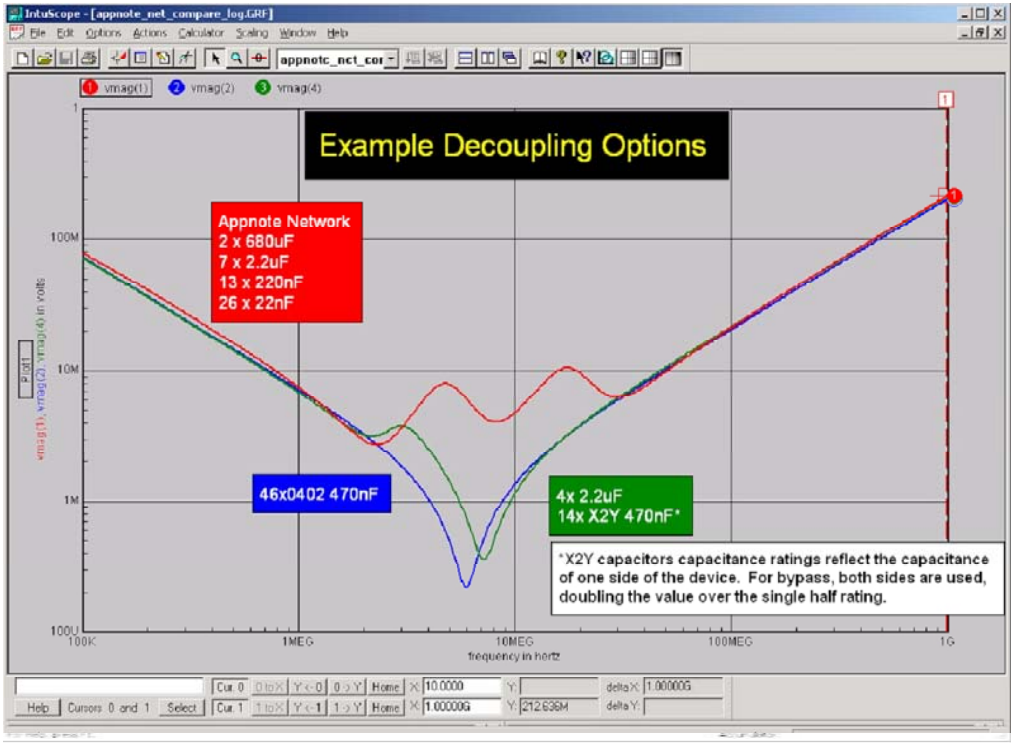
- Bypass goal is driven by **INSERTION LOSS.**
- High frequency insertion loss is set by **INDUCTANCE**.
- SRF for a given package moves with capacitance.
- Capacitance has no impact on high frequency effectiveness.
- Capacitor **SRF has NO EFFECT** on high frequency effectiveness.

Discrete Capacitor / Plane AR
Is This a Problem?

- Bypass capacitors resonate w/plane cavities.
- Single capacitor value exhibits higher peak |Z| than F^N network (flat impedance) at resonance.
- What does this affect?
  - Signals that use multiple voltage planes as return paths.
    - Reference signals against returns properly
  - EMC if resonance is excited
    - Tune if needed
    - Break-up cavities
  - Power deliver IFF AR < IC LPF cut-off
    - Choose dielectric appropriately

Example

				QTY		
Size	Pkg	ESL mounted	ESR	App Note	0402	X2Y
680uF	E box	2.8nH	570mΩ	2[1]	-	-
2.2uF	0805	2.0nH	20mΩ	7	-	4
220nF	0603	1.8nH	60mΩ	13	-	-
22nF	0402	1.5nH	200mΩ	26	-	-
470nF	0402	1.5nH	10mΩ	-	46	-
940nF	X2Y 0603	0.53nH	5mΩ	-	-	14
Vias				92	92	92



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Example Vccint, Conventional MLCC Capacitors

fco	5.00E+07
cap ESL	500
cap via space	0.05
cap vias	2
cap mtd L	982
attach L	10
Lspread 1"	27
Lspread 5"	46

Virtex2/Pro Core Power

S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
...	

Ztarget mohms	100	50	40	30	25	20	18	16
Lbudget pH	318	159	127	95	80	64	57	51
Radius "								
1	4	9	11	17	23	37	48	70
1.2	4	9	12	18	25	40	54	82
1.5	4	9	12	19	26	45	63	105
2	4	9	12	20	29	53	80	163
3	4	9	13	22	33	71	129	781
5	4	10	14	25	42	124	613	9999
Lattach+Lspread	12%	23%	29%	38%	46%	58%	64%	72%
Cap increase	0%	11%	27%	47%	83%	235%	1177%	14184%

- Keep L_{SPREAD} + L_{ATTACH} <= 50% of L_{BUDGET}
- Capacitor position may vary by 0.5” for 10% count increase

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Example Vccint w/X2Y Caps

fco	5.00E+07
cap ESL	100
cap via space	0.03
cap vias	6
cap mtd L	225
attach L	10
Lspread 1"	27
Lspread 5"	46

Virtex2/Pro Core Power

S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
…	

Ztarget mohms	100	50	40	30	25	20	18	16
Lbudget pH	318	159	127	95	80	64	57	51
Radius "								
1	1	2	3	4	6	9	11	16
1.2	1	2	3	4	6	10	13	19
1.5	1	2	3	5	6	11	15	24
2	1	2	3	5	7	12	19	38
3	1	3	3	5	8	17	30	179
5	1	3	4	6	10	29	141	9999
Lattach+Lspread	12%	23%	29%	38%	46%	58%	64%	72%
Cap increase	0%	50%	33%	50%	67%	222%	1182%	62394%

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Example Vcco

fco	5.00E+07
cap ESL	500
cap via space	0.05
cap vias	2
cap mtd L	1361
attach L	70
Lspread 1"	54
Lspread 5"	73

Virtex2/Pro I/O Power	
S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
...	

Ztarget mohms	100	90	85	80	75	70	60	55
Lbudget pH	318	286	271	255	239	223	191	175
Radius "								
1	8	9	10	11	12	14	21	27
1.2	8	9	10	11	13	15	22	30
1.5	8	9	10	12	13	16	24	33
2	8	10	11	12	14	17	27	40
3	9	10	12	13	16	19	34	54
5	9	11	13	15	18	23	47	104
Lattach+Lspread	39%	43%	46%	49%	52%	56%	65%	71%
Cap increase	13%	22%	30%	36%	50%	64%	124%	285%

- L_{ATTACH} now > L_{SPREAD} @ 1" radius
- 1 Capacitor / Vcco pin is conservative
- 100 or more caps for one chip!

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Example Vcco w/X2Y Caps

fco	5.00E+07
cap ESL	100
cap via space	0.03
cap vias	6
cap mtd L	323
attach L	70
Lspread 1"	54
Lspread 5"	73

Virtex2/Pro I/O Power	
S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
...	

Ztarget mohms	100	90	85	80	75	65	60	55
Lbudget pH	318	286	271	255	239	207	191	175
Radius "								
1	2	2	3	3	3	4	5	7
1.2	2	3	3	3	3	5	6	7
1.5	2	3	3	3	4	5	6	8
2	2	3	3	3	4	5	7	10
3	2	3	3	4	4	6	8	13
5	3	3	3	4	5	8	12	25
Lattach+Lspread	39%	43%	46%	49%	52%	60%	65%	71%
Cap increase	50%	50%	0%	33%	67%	100%	140%	257%

- Manageable capacitor count, 24 – 32 for all Vcco

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Example Vcco Top of Stack

fco	5.00E+07
cap ESL	500
cap via space	0.05
cap vias	2
cap mtd L	982
attach L	39
Lspread 1"	27
Lspread 5"	46

Virtex2/Pro I/O Power	
S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
…	

Ztarget mohms	100	80	60	50	40	35	30	25
Lbudget pH	318	255	191	159	127	111	95	80
Radius "								
1	4	6	8	11	17	22	34	74
1.2	4	6	9	11	17	23	37	88
1.5	4	6	9	12	18	25	41	114
2	5	6	9	12	19	27	47	188
3	5	6	9	13	21	31	60	2142
5	5	6	10	14	24	38	95	9999
Lattach+Lspread	21%	26%	35%	42%	52%	59%	69%	83%
Cap increase	25%	0%	25%	27%	41%	73%	179%	13412%

- 2X |Z| reduction from double plane angle & plane priority
- Now need 1.5 caps / pin!

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Example Vcco Top of Stack w/X2Y Caps

fco	5.00E+07
cap ESL	100
cap via space	0.03
cap vias	6
cap mtd L	225
attach L	39
Lspread 1"	27
Lspread 5"	46

Virtex2/Pro I/O Power	
S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
...	

Ztarget mohms	100	80	60	50	40	35	30	25
Lbudget pH	318	255	191	159	127	111	95	80
Radius "								
1	1	2	2	3	4	5	8	17
1.2	1	2	2	3	4	6	9	20
1.5	1	2	2	3	4	6	10	27
2	1	2	2	3	5	7	11	43
3	1	2	3	3	5	7	14	491
5	1	2	3	4	6	9	22	9999
Lattach+Lspread	21%	26%	35%	42%	52%	59%	69%	83%
Cap increase	0%	0%	50%	33%	50%	80%	175%	58718%

- Cap count remains manageable

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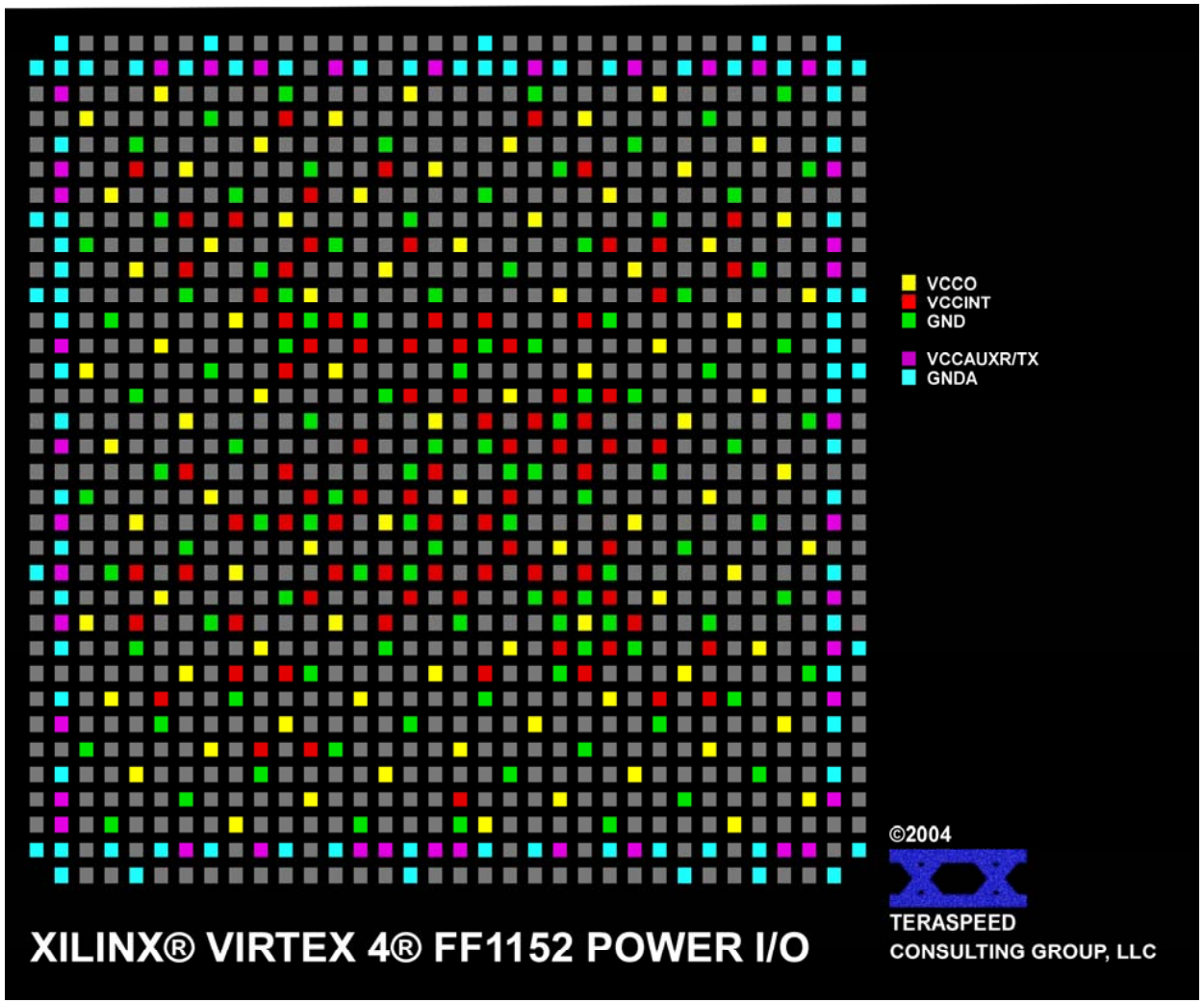
New Package Architectures



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New Package Architectures

- Lower application PCB spreading inductance
  - Thin planes inside the pkg maximize attachment utility
  - More extensive in-package bypass caps
- Lower attachment inductance
- Tighter I/O pwr/gnd chevron
- More uniform I/O impedance
- Rocket I/O™ SERDES moved to boundary
  - Better impedance control
  - Better power isolation

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Bypass Synthesis Procedure

- Budget specific impedance vs. frequency for each supply.
- Translate to inductance budget for each supply.
- Determine plane separations for each supply as nominal spreading L to capacitor ring as 25% L budget.
- Confirm design is still realizable

Synthesis Procedure

- Assign planes in order of increasing impedance requirements from IC mtg. surface
- Determine max. upper plane depths such that IC via attach and spreading L < 50% L budget
- Confirm stack-up viable
- Compute plane spreading inductances
- Budget mounted capacitor array inductance per supply

Synthesis Procedure

- Select bypass capacitor type:
  - Conventional or
  - Low inductance
- Determine capacitor qty. required
- Confirm realizable design
- Determine LF cut-off
- Determine whether one capacitance value will damp properly at LF cut-off

Synthesis Procedure

- If second cap value needed to extend LF response:
  - Determine capacitance shortage
  - Select lowest inductance capacitor to make up shortfall in a reasonable number of parts
  - Check AR peaking w/ primary array
  - As necessary iterate size / count to correct AR peak
  - Simulate final result

Conclusions

- All elements:
  - FPGA attachment vias
  - Power / ground planes
  - Bypass capacitor attachment vias
  - Bypass capacitors

Contribute to bypass network performance

Conclusions

- Excessive via attachment or plane spreading inductance defeats even "TIG welded" planes.
- X2Y™ capacitors make possible dramatic component reduction. The higher the required performance the better the X2Y™ advantage.
- Backside capacitor attachment can mitigate the need for a dedicated plane pair in **some** circumstances

Conclusions

- Capacitor array performance is sensitive to orientation and via patterns
- Multiple MLCC values should only be used to extend **low frequency response**
- Virtex4 packaging represents a major advancement in PDS to FPGA interface.