Measurement and comparative S21 performance of raw and mounted decoupling capacitors

Simple fixtures provide straightforward capacitor characterization for raw device and in-circuit performance.

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All IC power systems require some level of passive decoupling. Accurate prediction of in-system capacitor performance is critical to reliable power system design. The following article simplifies capacitor choice by detailing reliable methods for readily obtaining both raw device and practical in-system performance data for any capacitor of interest

CAPACITORS

Decoupling capacitors perform a lowly, but critical system function. Before designing a power distribution system (PDS), an understanding of basic capacitor function is necessary. Basically, a decoupling capacitor acts as a noise shunt impedance across the power distribution network. Noise currents drawn from active circuitry become noise voltages as $e_{noise} + i_{noise} * Z_{pds}$.

Decoupling capacitors have typically served two purposes:

- Stabilization of DC power rails against active circuitry load transients
- Coupling of DC power rails to ground as digital logic signal returns

At high frequency, decoupling capacitor impedance is inductive. The number of capacitors needed to realize a given impedance is directly proportional to the mounted inductance. Both performance and economy are boosted by optimizing capacitor mounting inductance.

DC POWER IC CUT-OFF FREQUENCY

In modern circuits, DC power stabilization requires maintaining power system impedance up to frequencies of 20 to 100 MHz, depending on the active devices used. Within an IC, power pins, package inductance, and in-package and on-die capacitance together create a low-pass power filter. For practical reasons, this filter has a cut-off that is rarely lower than 20 MHz and rarely higher than 100 MHz. Lower frequency cut-offs demand more in-package and on-chip capacitance and boost costs. Higher frequency cut-offs require a massive increase in the number of power and ground pins.

Consequently, if IC manufacturers were to attempt a significant hike in the cut-off frequency of IC packs, they would be forced to contend with drastically higher packaging costs along with vastly increased demands on the PCB power systems. Beware the ASIC or ASSP (application specific standard product) supplier who knows little, and/or is willing to disclose little, about the impedance-versus-frequency requirements of their parts. Such "reticence" can be a recipe for disaster. Substantial modification of a power system is very difficult once boards have been built. Power characteristics of devices must be factored into the earliest stages of the design process.

RETURN SIGNAL COUPLING

High-speed logic signals contain frequency spectra determined by both the signal repetition rate and the signal rise/fall time. Common practice for many years has been to use

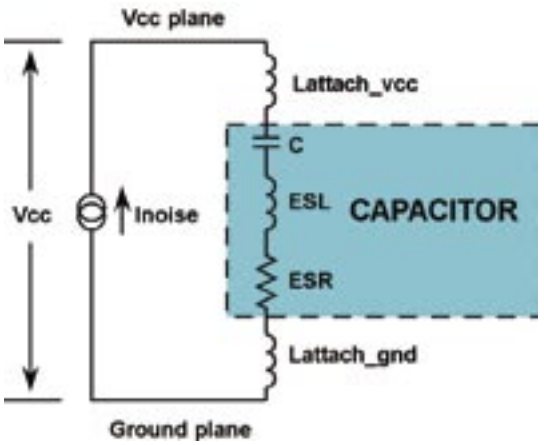

Figure 1. *SPICE model, mounted decoupling capacitor.*

DC power rails as signal returns. When rise times were slow, this was a sensible reuse of valuable copper consumed by power planes. In an era of 10- to 100-ps rise times, it is an invitation to EMC headaches that demand very expensive solutions such as a lot of buried capacitance (BC)[1]—or worse, that require a complete redesign. [Note that there are techniques to extend the frequency response of boards, including distributed edge termination, among others.[2]]

The upshot is that successful decoupling design begins with an architecture for both power and signaling. The power distribution impedance-versus-frequency requirements are then determined from this architecture. Given these requirements, a designer can "chart" the mounted capabilities of the decoupling capacitors chosen for the finished product. The focus of this article is determining capacitor capabilities before schematic capture.

RAW CAPACITOR PERFORMANCE

All capacitors include a certain amount of intrinsic inductance. The mounted inductance limits performance at high frequency. As shown in Figure 1, the mounted inductance consists of two parts:

- Raw component inductance
- Attachment inductance

The first task is to extract the raw parameters for any prospective capacitor. Determining what the capacitor can do in an ideal environment allows a designer to evaluate trade-offs in mounting and grouping.

Accurate raw device measurement can be achieved with a simple microstrip fixture for each likely capacitor type. The fixture (Figure 2) for each capacitor consists of two SMA connectors with a 50-Ω microstrip connection to the device-under-test (capacitor). Near the DUT the

Figure 2. *Example microstrip test fixture.*

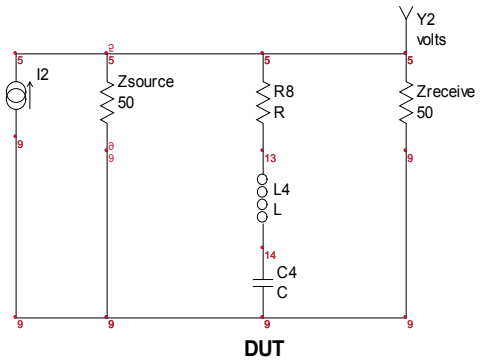

Figure 3. *SPICE model, microstrip fixture.*

50-Ω microstrip impedance is discontinuous. The smaller the fixture, the smaller the discontinuity and the more accurately the fixture reports high frequency performance. With little effort, capacitor performance to 300 MHz and beyond is easily attainable. S21 (scattering parameters indicating insertion loss) may be measured with almost any VNA (vertical network analyzer).

An example is a fixture for 0.36-µF capacitors—the fixture is just large enough to provide the SMA connections and the capacitor attachment.

EXTRACTING THE CAPACITOR PARAMETERS

The idealized model of the test setup is as shown in Figure 3.

First, calibrate the VNA using the test fixture with no capacitor soldered in. Then solder the capacitor and collect S21 parameters.

The voltage amplitude in dB is:

$$S21\ dB = 20 * Log_{10} * Z_{DUT}/(Z_{DUT}+25)$$

Solving for Z_{DUT}:

$$Z_{DUT} = 25 * 10^{(S21dB/20)}/(1-10^{(S21dB/20)})$$

Insertion loss for a capacitor follows a "V" curve (Figure

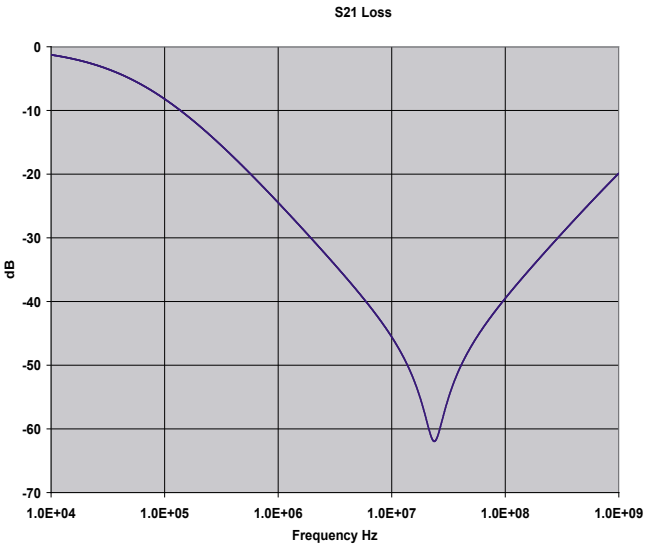

Figure 4. *Insertion loss, typical 100-nF MLCC.*

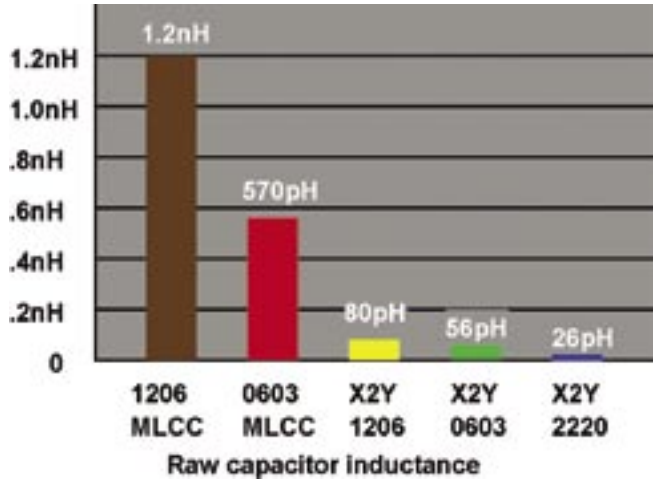

Figure 5. *Example extracted inductance.*

4). Multilayer ceramic chip (MLCC) capacitors have high Qs and consequently steep inflections near the SRF (series resonant frequency).

For a simple series R-L-C:

$$Z = \sqrt{[ESR^2 + (Z_C - Z_{ESL})^2]}$$

At the SRF, the inductive and capacitive reactances cancel, leaving only the ESR (equivalent series resistance).

$$ESR = 25 * 10^{(S21dB\_MAX\_LOSS/20)}/(1 - 10^{(S21Db\_MAX\_LOSS/20)})$$

Given ESR, then capacitance can be determined.

The capacitance may be accurately obtained by solving the impedance equation at a frequency F_1 well below the SRF. Note that at the SRF, the capacitive and inductive reactances are equal, allowing for substitution:

$$Z_{F1} = 25 * 10^{(S21dBF1/20)}/(1 - 10^{(S21dBF1/20)})$$

$$C = (F_{SRF}/F_1 - F1/F_{SRF})/[2\Pi * F_{SRF} * \sqrt{(Z_{F1}{}^2 - ESR^2)}]$$

Once the capacitance has been determined, the solution for inductance is based on the SRF as simply:

$$L = 1/[(2\Pi * F_{SRF1})^2 * C]$$

The advantage of this extraction method[3] is that it minimizes errors caused by stray inductance in the test fixture and provides a repeatable, accurate measurement.

RAW DEVICE RESULTS

Typical results for several popular devices are shown.

Here we see that the three capacitors to the right of the graph (Figure 5) exhibit 1/10th or less the inductance of their MLCC (multi-layer ceramic chip) counterparts. In a perfect world, this observation might allow us to get away with only 1/10th the number of decoupling capacitors. In reality, the attachment inductance drops the gain down to about 3:1 for a typical 0.062" thick 4/6 layer board.

MOUNTED INDUCTANCE MEASUREMENTS

The designer's end objective is to predict performance in real

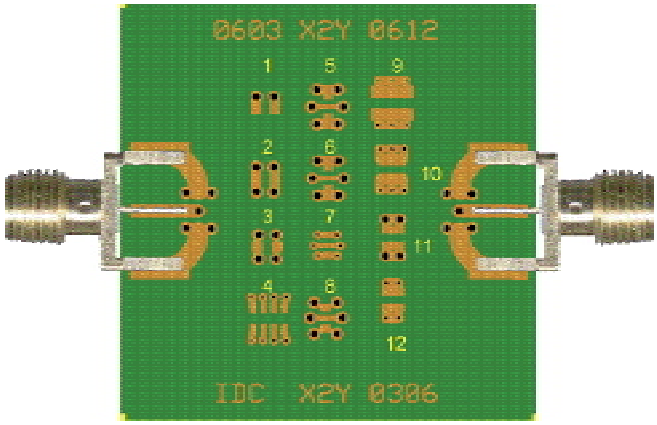

Figure 6. *Example test fixture.*

systems. The capacitor attachment and power distribution plane arrangement have as much effect on the decoupling performance as the capacitors themselves. The evaluation process is similar as with the microstrip test boards, except that now a multilayer board representative of the proposed board construction of interest is used (Figure 6).

For accurate measurements:

- Keep overall board area to a minimum to limit the highest board SRF and to minimize result coloring caused by plane capacitance.
- A good size is a square section that separates the SMA connectors by about the size of the largest BGA (ball grid array) that is used in designs with comparable board construction.
- Mount capacitors near the middle of the test board. Spreading inductance has little effect, especially on thin planes for capacitors mounted somewhat off-axis. This arrangement facilitates using one board to evaluate 9 to 12 different types of capacitors with minimal error.

A SPICE model of the test fixture with DUT mounted is shown in Figure 7.

The measurement and extraction procedure is similar to that for raw parts on a microstrip board:

$$ESR = 25 * 10^{(S21dB\_MAX\_LOSS/20)}/(1-10^{(S21Db\_MAX\_LOSS/20)})$$

$$Z_{F1} = 25 * 10^{(S21dBF1/20)}/(1-10^{(S21dBF1/20)})$$

$$C = (F_{SRF}/F_1 - F_1/F_{SRF})/[2\Pi * F_{SRF} * \sqrt{(Z_{F1}{}^2 - ESR^2)}]$$

$$L = 1/[(2\Pi * F_{SRF1})^2 * C]$$

Where F_1 is a frequency significantly below the SRF, typically, select F1 near SRF/10.

Boards with multiple patterns provide an easy means to experiment with several different mounting strategies for maximizing the efficiency of the mount. Attachment inductance increases with any:

- Lateral distance from the capacitor pad to the attachment via.
- Length of the via tube to the respective plane.
- Plane separation.
- Proximity of like polarity vias/traces

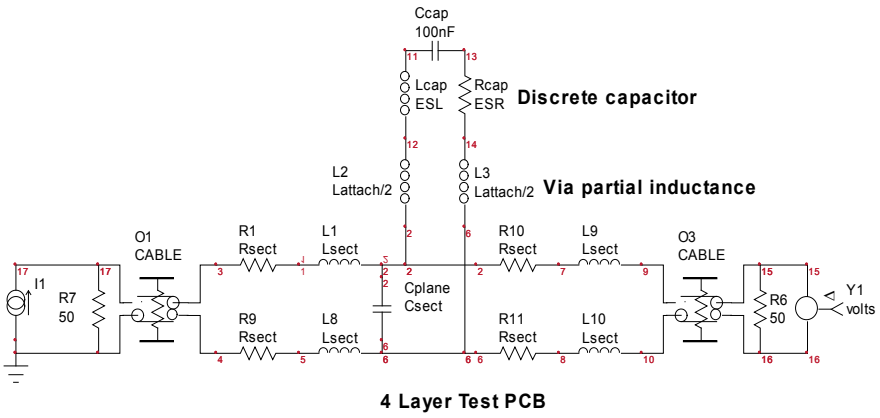

Figure 7. *SPICE model of 4-layer test board.*

Attachment inductance decreases with:

- Increased via tube diameter
- Proximity of opposing polarity vias/traces.
- Additional vias.

MEASUREMENT EXAMPLES AND CAPACITOR CHOICE

These measurements demonstrate that the single mounted low inductance capacitor at right on Figure 8 has 1/3 the inductance of an ordinary MLCC, and outperforms four MLCC s mounted in a cluster designed to minimize mutual inductance. Plane spacing on these test boards is 0.038. Boards with thinner plane spacing increase the advantage of low inductance capacitors over conventional devices, resulting in even better gains. Practical application of these measurement techniques and results with FPGA (field programmable gate arrays) PCB layouts bear out superior results, replacing over one hundred conventional MLCC capacitors with fewer than one-third as many multi-layer capacitors with a unique proprietary circuitry.[4]

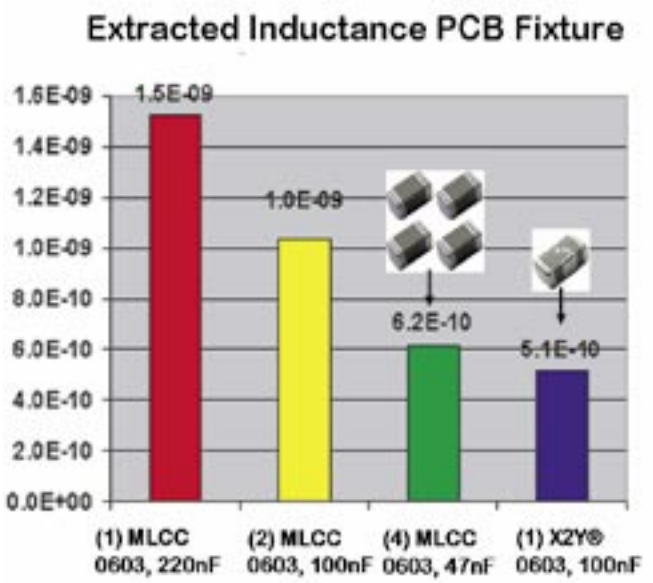

Figure 8. *SPICE model of 4-layer test board.*

CONCLUSION

Capacitor high frequency performance is limited by the mounted capacitor inductance. Simple microstrip and four-layer fixtures enable straightforward extraction of both raw device characteristics, as well as mounted device system performance. Using these methods, comparison and assessment of the advantages of modern low inductance capacitors versus traditional decoupling methods can be accurately assessed, thus clarifying the designer's choice of capacitor. Testing of completed board designs correlates well with test board measurements.

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3. Additional details on this extraction methodology may be found on the X2Y website: www.x2y.com, Application Note: "TT#3004 - Accurate Capacitor Inductance Extraction from s21 Measurements."
4. "High Performance FPGA Decoupling w/ X2Y Capacitors" www.x2y.com

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