EMC Guideline for Synchronous Buck Converter Design

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***Abstract*— Synchronous buck converters generate broadband noise typically in 50 – 300 MHz range. In this paper, the root cause of this broadband noise and possible coupling mechanisms are analysed. Then, a list of EMC design guideline for minimizing the broadband noise is presented. The guideline contains circuit level guideline which involves input filtering, component selection, and an effective snubber strategy using a parallel resistor and inductor. The guideline also contains layout level guideline, which involves decoupling capacitor placement, layer stackup, and minimizing exposed phase voltage area. For each suggested guideline item, an example illustrates the impact of the particular strategy through experimental results or SPICE simulations, leading to a strong reduction of broadband noise from the synchronous buck converter.**

Key words: Broadband EMI, Synchronous Buck Converter, SMPS, Snubber

I. Introduction

Switched-Mode Power Supply (SMPS), in spite of their superior efficiency, generates electrical noise due to its high dv/dt and di/dt from switching. One of the popular SMPS DC/DC converter topology is synchronous buck converter [1] [2]. The synchronous buck converter typically generates three types of EMI: low frequency conducted noise (<30 MHz) as harmonics of the switching frequency, broadband noise (50 – 300 MHz) from the phase voltage ringing, and high frequency noise (>300 MHz) as a result of reverse recovery [3]. The main focus of this EMC design guideline is to minimize the 50 – 300 MHz broadband EMI.

Based on the root causes, a list of EMC design guideline for minimizing the broadband noise is presented. The guideline contains circuit level advice which involves input filtering, component selection, and patent-pending effective snubber strategy using a parallel resistor and inductor. The guideline also contains layout level advice which involves decoupling capacitor placement, layer stackup, and minimizing exposed phase voltage area.

II. Brief Description of Synchronous Buck Converter Operation

Figure 1 shows the schematic of a typical synchronous buck converter [1] [2]

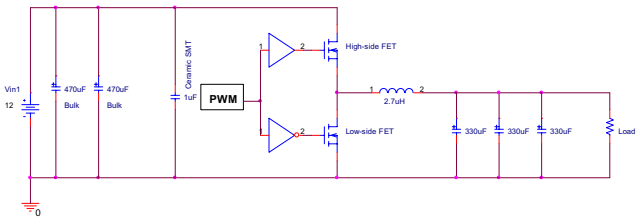

Figure 1. Typical Synchronous Buck Converter Schematic

In an ideal operation, the two MOSFETs (high-side and low-side) switch alternatively. The switching of the MOSFETs is controlled by a controller IC which generates a PWM signal and drives the gates.

Usually, two types of capacitors are placed at the input side: Electrolytic Bulk Capacitor and Ceramic SMT Capacitor. The bulk capacitors are generally very high-valued (>100 uF) and are used to decouple low-frequency switching noise (typically 100 – 300 KHz switching rate and its harmonics) and to provide charge. The ceramic SMT capacitors are placed closer to the switches (MOSFETs) to provide high-frequency current corresponding to the rise/fall time of the switching waveform (>30 MHz).

III. Broadband EMI from Synchronous Buck Converter

Figure 2 shows the measured far-field EMI from a synchronous buck converter test board.

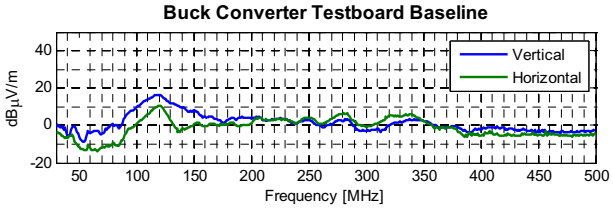

Figure 2.Far-field EMI from Synchronous Buck Converter Test Board

Figure 2 shows the radiated broadband EMI centered at 120 MHz. Depending on the design of the converter, this center frequency can typically range from 50 to 300 MHz.

IV. Root Cause of the Broadband EMI from Synchronous Buck Converter

To illustrate the root cause of the broadband EMI let us analyze the circuit diagram shown in Figure 3. It shows the input side of the converter and includes parasitics: trace inductances and capacitor ESR and ESL.

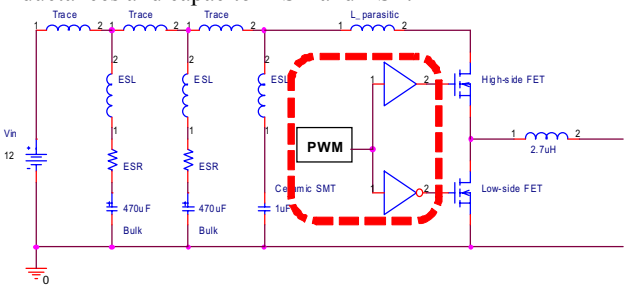

Figure 3. Input and Switching Cell Part of the Synchronous Buck Converter with Parasitic Inductances

The parasitic loop inductance, 'L_parasitic' corresponds to the parasitic inductance associated to the geometry of the loop formed by the ceramic SMT capacitor and the two MOSFETs, indicated by the thick red line.

This switching loop can be modeled as an RLC circuit [5]. It is formed by the input decoupling capacitor and the high- and low-side MOSFETs. The ringing occurs when the high side FET is on and the low side FET is off, thus, it acts as a capacitor. Figure 4 shows the equivalent circuit of the switching loop during this state.

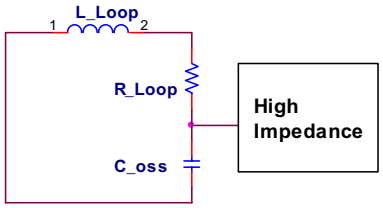

Figure 4. Switching Loop (Top) and the Equivalent Model when High-side MOSFET is on and Low-side MOSFET is off

The inductance in this model (L_Loop) corresponds to the total loop inductance of the switching loop, which consists of ESL of the capacitor, package inductance of the MOSFETs and the parasitic inductance associated with the geometry of the loop. The total capacitance of the loop can be approximated as the output capacitance, Coss of the low-side MOSFET which typically ranges from 200pF to 3nF. The value of the input capacitor is irrelevant since its value is usually much larger than Coss. Finally, the total resistance of the loop is modeled as a loop loss (R_Loop). This loop loss contains the "on resistance" of the high-side MOSFET and the loss term associated with the output capacitance, Coss of the low-side MOSFET, and any other losses that might occur, like small radiation losses, trace losses etc.

This RLC structure in the switching loop forms a series resonant structure. This resonance occurs when the high-side MOSFET turns on and the low-side MOSFET turns off, which corresponds to the rising edge of the phase voltage waveform. The resonance causes ringing in the phase voltage as shown in Figure 5.

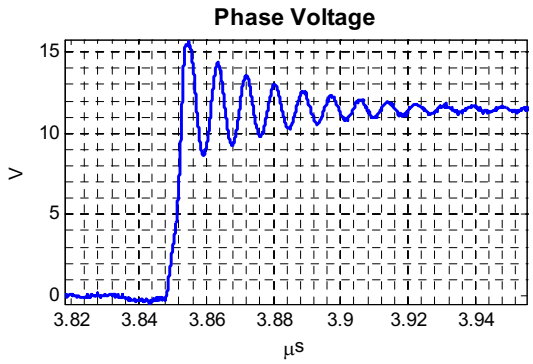

Figure 5. Ringing in the Phase Voltage Waveform Due to Parasitic Resonance in the Switching Loop

The frequency of the oscillation correlates to the resonant frequency of the RLC structure. This also corresponds to the frequency at which the measured far-field broadband EMI is centered at. The correlation between the switching resonance and the radiated broadband EMI noise has been shown through series of experiments and measurements [5].

V. Switching Loop Resonance

The resonant frequency of the switching loop is determined by the total parasitic loop inductance and the low-side MOSFET output capacitance as following:

$$f_{resonance} = \frac{1}{2\pi\sqrt{L\_loop \times Coss}}$$

Equation 1

To minimize the broadband EMI caused by this parasitic resonance in the switching loop, the design goal should be to push this resonant frequency up as high as possible. There are multiple reasons for pushing the resonant frequency up. The typical rise times are in the range of a few nanoseconds, often measured to be about 5ns. For the frequency range of interest there is decay in spectral density, thus, the ringing can be reduced if its frequency is moved up. This can also reduce the overshoot and place less stress on the MOSFETs. Further, it also can prevent non-ideal effects such as c dv/dt induced accidental turn on [6].

In order to move the resonant frequency up, there are two options: reduce L_loop or reduce Coss.

To decrease the inductance, one option is to reduce the size of the switching loop. In other words, the input decoupling capacitor and the two MOSFETs (high-side and low-side) must be placed as close as possible.

Also, by using multiple input decoupling capacitors and placing them in a minimal inductance arrangement [7], the resonant frequency can be shifted further up.

An experiment illustrates this. Figure 6 shows a layout. Capacitors can either be placed close to the high side FET or 5mm further away, as indicated by the arrows. This change

in decoupling capacitor placement increases the loop inductance and therefore should decrease the resonant frequency in the switching loop.

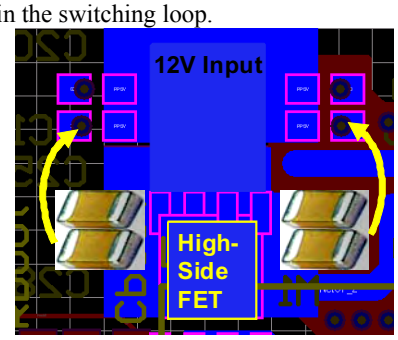

Figure 6. Capacitor Placement Experiment

Figure 7 shows that impact of this change in capacitor placement on measured radiated broadband noise.

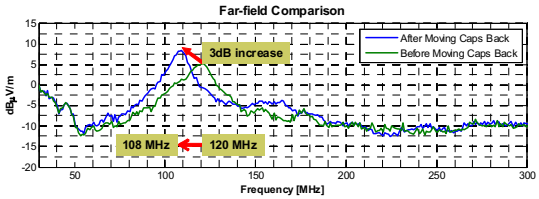

Figure 7. Impact of Input Decoupling Capacitor Placement on Radiated Broadband Noise

Figure 7 shows that when the capacitors were moved away from the high-side MOSFET, the resonant frequency shifted down as expected, and is indicated in the peak frequency of the measured far-field broadband noise. This is a result of an increase in the loop inductance from 4.6nH to 6.6nH. The measured far-field noise also shows that the peak value has increased by 3dB when the change was made. Although it may seem small, sometimes, 3dB can make a difference in passing or failing the compliance limit. The experiment illustrates that proper capacitor placement can reduce the radiated broadband noise from the synchronous buck converter.

Another way of reducing the switching loop inductance is placing a solid ground plane right underneath the layer which contains the switching loop using a thin dielectric material. Figure 10 illustrates the difference in the current path with different dielectric thickness.

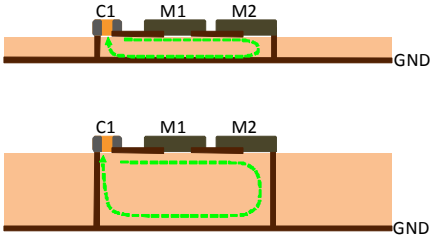

Figure 8. Dielectric Thickness

As shown in figure 8, by placing the ground plane as close as possible to the switching loop (in other words, using minimum dielectric thickness), the switching loop size can be also minimized. This will not only reduce the magnetic coupling to the external environment, but also the internal coupling through inner layers.

VI. Possible Coupling Paths:

There are four main possible coupling paths:

1. Conducted path through the DC input side
2. Conducted path through the DC output side
3. Electric coupling from the phase voltage
4. Magnetic coupling from the switching loop

Figure 9 shows the coupling paths in the schematic:

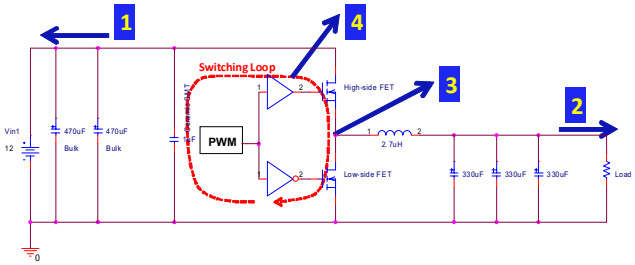

Figure 9. Four Major Possible Coupling Paths

The two conducted paths through DC input and output can be significantly important unless they are properly filtered. The conducted noise through the DC rails can be seen as glitches and ringing on the DC rail. The third coupling path, electric coupling from the phase voltage, is due to the high dv/dt switching voltage waveform on the phase node. Finally, the magnetic coupling from the switching loop is due to the high noise current from the parasitic LC resonance in the switching loop.

The first coupling path is the DC input side. If the power plane is not properly decoupled, the switching frequency harmonics can be conducted out through the DC input side. In general, the bulk capacitors can reduce the switching harmonics to an acceptable level. However, the high-frequency noise from the switching loop resonance can also be conducted through or couple to the DC input side. Figure 10 shows the measured 12V rail voltage at the DC input connector.

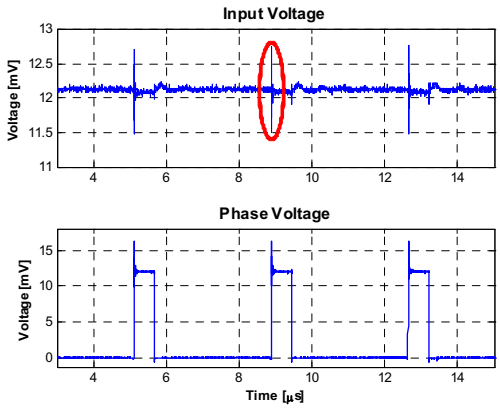

Figure 10. High Frequency Noise on the 12V Rail

Taking care to setup a measurement that is not affected by inductive coupling, the high-frequency noise on the 12V rail shown in Figure 10 has a peak value of up to ±600mV. It also shows that the noise on the 12V input rail is synchronous to the phase voltage waveform indicating that the switching of voltage at the phase node is causing this noise on the rail. The noise on this rail can be prevented from conducting out the DC input cable by adding a filter before the DC input connector. Figure 11 shows the pi-filter implemented on the input side of the synchronous buck converter.

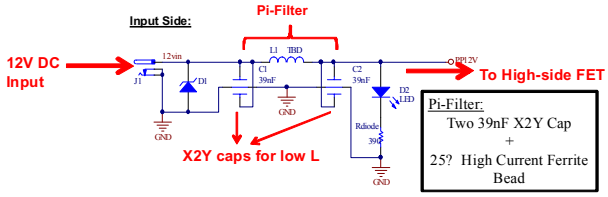

Figure 11. Input Pi-filter for Filtering High-frequency Noise on the DC Input Rail

Figure 12 shows the impact of adding the input filter on the radiated broadband noise.

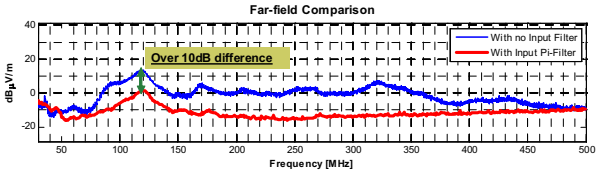

Figure 12. Impact of Adding an Input Filter on Far-field Broadband Noise

Figure 12 shows that by adding the input pi-filter, the radiated noise was decreased by up to 10dB. This shows that adding an input filter is very effective in reducing the radiated broadband noise from the converter, if the dominating noise coupling path is the conducted path through the input side.

The next possible coupling path is the DC output side. Due to the impedance of the main inductor and heavy capacitive loading one the output side, there was not significant noise observed on the DC output rail. However, as the resonant frequency is shifted up higher, care must be taken into designing output filters which is effective at higher frequencies.

The third possible coupling path is the electric coupling from the phase voltage plane. The phase voltage plane contains a high dv/dt waveform which could couple to the surroundings through capacitive (electric) coupling. The following example illustrates this coupling path. If the phase voltage switches from 0 to 12V in 5ns, and a stray capacitance of 100 fF exits between the phase voltage area on the PCB and the chassis, a peak current of 240μA will flow from the chassis to the PCB. The displacement current than create a common mode voltage driving the antenna structure. Figure 13 shows a situation where the electric coupling from the phase voltage plane could be relevant.

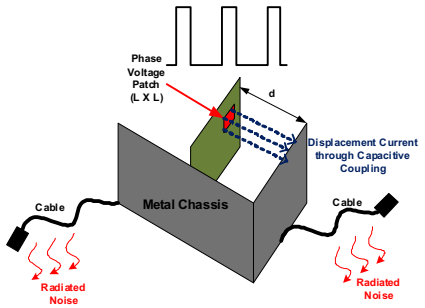

Figure 13. Electric Coupling from Exposed Phase Voltage Plane

As this coupling is predominantly capacitive, reducing the size of the exposed phase voltage plane can reduce the mutual capacitance responsible for the coupling. Figure 14 shows the possible change in the real PCB layout to reduce the size of the exposed phase voltage plane

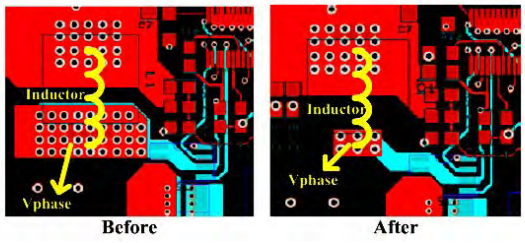

Figure 14. Reducing the Size of the Exposed Phase Voltage Plane

The change in electric coupling from this reduction of the exposed phase voltage plane area can be measured using a TEM cell [4][5].

The last coupling path is the magnetic coupling from the switching loop. As explained in the earlier section, the parasitic LC resonance in the switching loop causes large noise current in the switching loop. This noise current in the switching loop can magnetically couple to other structures or drive an antenna structure. Figure 15 shows the result of near-field scanning around the switching loop using magnetic loop probe.

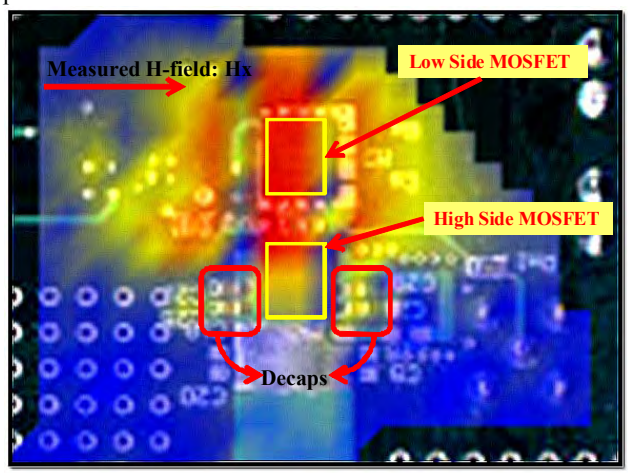

Figure 15. Magnetic Field around Switching Loop
(Help of Amber Precision Instruments – www.amberpi.com)

Minimizing the size of the switching loop can reduce the mutual inductance between the loop and the radiating element which is responsible for the magnetic coupling.

As explained in the earlier section, the switching loop size can be minimized by good input decoupling capacitor placement and a solid ground plane as close as possible to the switching loop.

If the switching loop size was practically minimized and the parasitic LC resonance in the switching is still problematic, then one can consider the option for adding a snubber circuit to provide attenuation of the resonance.

VII. RL SNUBBER

Typically, the most popular choice of the snubber for the phase voltage ringing of the synchronous buck converter is the series RC snubber. A series combination of a small resistor and a capacitor is placed in parallel to the low-side MOSFET to add losses in the switching loop. The details of the theory of operation and design method for RC snubber are published in many literatures [8] [9], so it will not be explained in further detail in this paper.

One of the drawbacks of the RC snubber is that the parasitic inductance associated with the RC branch can reduce the effectiveness of the snubber. This is especially true if the inductance of the switching loop has already been minimized. Also, choosing the value of the resistor and capacitor for the RC snubber is not very trivial, and could require many iterations and measurements.

Another way of adding a loss in the switching loop is to add a parallel combination of a small resistor and an inductor in series to the switching loop. By adding losses in the switching loop, the parasitic LC resonance in the switching loop will be damped. Figure 16 shows how the RL snubber can be implemented in schematic.

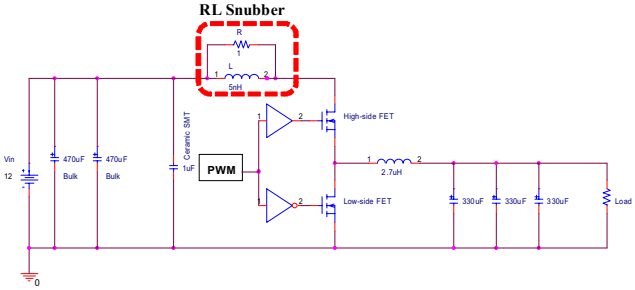

Figure 13. RL Snubber

The advantage of the RL snubber is its simplicity. The R and L values can be simply designed based on the resonant frequency. As an example, let us consider the system which has parasitic switching loop resonance at 120 MHz. The RL snubber should be designed such that it is lossy at 120 MHz. Typical natural losses in the switching loop is in the order of hundreds of mΩ. That means, adding another 1Ω loss in the system at resonance can show 6 to 10dB suppression of ringing. So after choosing the value of resistor to be 1Ω, the inductor value can be chosen such that the cut-off of this RL snubber is below 120 MHz, for instance, 60MHz. Then, the inductor value necessary can be calculated to be about 2.5nH.

The RL snubber with 2.5nH and 1Ω was implemented on the synchronous buck converter test board. Figure 17 shows the measured phase voltage waveform showing the significant damping of the phase voltage ringing with RL snubber.

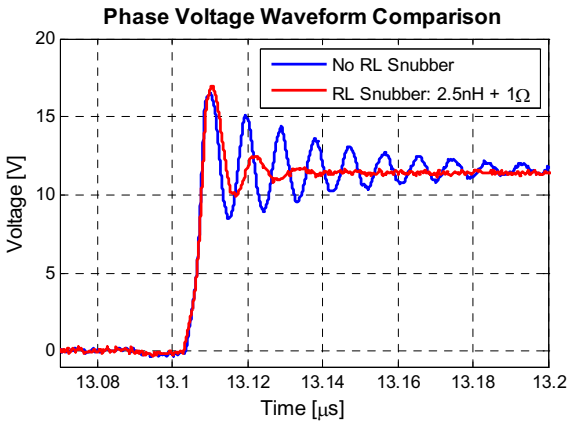

Figure 14. Phase Voltage Comparison with RL Snubber

The significant damping on the phase voltage ringing indicates that the switching loop resonance has been attenuated significantly. This translates to the decrease in far-field broadband noise as shown in Figure 18.

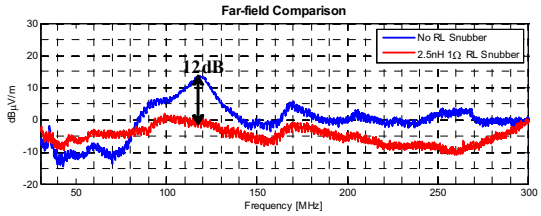

Figure 15. Far-field Noise Comparison with RL Snubber

VIII. CONCLUSION

It was shown that the root cause of the 50 – 300 MHz broadband noise from the synchronous buck converter is the parasitic LC resonance in the switching loop formed by the decoupling capacitor and the switching MOSFETs. The two important aspects about the parasitic LC resonance in the switching loop are the resonant frequency and the loss at resonant frequency. The design goal should be to push the resonant frequency up. In order to do so, the loop inductance of the switching loop must be minimized. The loop inductance can be minimized by proper placing of all components, minimizing the switching loop size, and having a solid ground plane under the switching loop with minimum dielectric thickness.

The four main possible noise coupling paths from the synchronous buck converter were:

1. Conducted path through the DC input side
2. Conducted path through the DC output side
3. Electric coupling from the phase voltage
4. Magnetic coupling from the switching loop

It was shown that by adding an input filtering at the DC input side, the radiated noise was decreased by up to 10dB. This shows that it is critical to provide a good isolation between the DC input side and the switching loop. To reduce the electric coupling from the phase voltage, the exposed phase voltage plane area must be minimized. Lastly, to reduce the magnetic coupling from the switching loop, the switching loop size should be minimized.

An effective snubber strategy using a parallel combination of a resistor and an inductor was introduced. The advantage of the RL snubber over the conventional RC snubber is its simplicity for design and implementation. It was shown that by adding an RL snubber, the ringing on the phase voltage waveform was significantly reduced, and also this translated to 13dB reduction in radiated broadband noise.

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