Does Position Matter? Locating Bypass Capacitors for Effective Power Distribution

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  - Advanced Printed Circuit Design
  - 3D Electromagnetic Modeling
  - Measurement Based Ibis Modeling
  - Package Design and Characterization
  - Power Analysis
  - FPGA Application Architecture & Development
  - Professional Training

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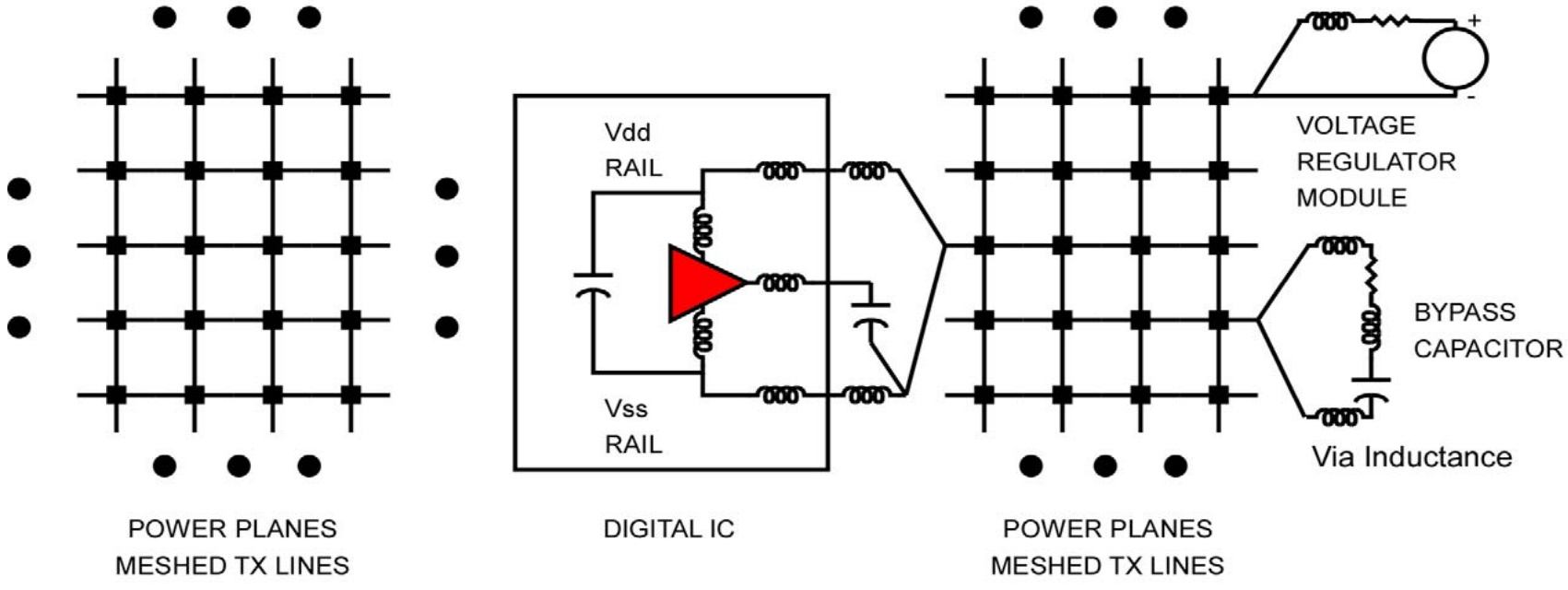
PDS w/ Bypass Capacitors

- Capacitors shunt nodes of meshed Tx lines formed by planes



HIGH-SPEED PWB POWER DISTRIBUTION SYSTEM

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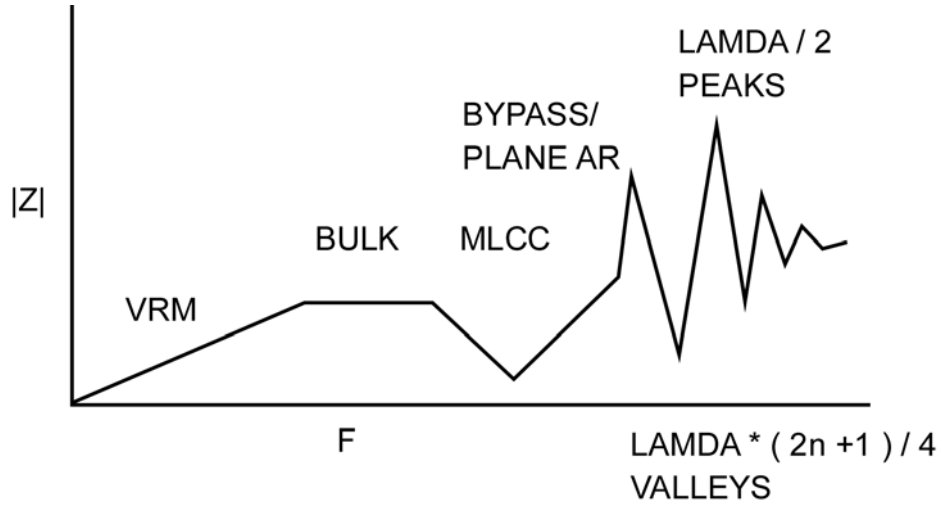
Shunt Functions

Bypass capacitor shunts-

- Core power.
- I/O power.
- I/O return current.
  - Sprectrum passes through bypass / plane AR as well as plane ¼ λ modes
- Energy injected into cavities by via traversals

PDS Plane |Z|

- Plane impedance modulates heavily from bypass network / plane AR on up.
- Signals that rely on plane⇔plane coupling see significantly higher SSO above 100MHz.



Bypassed Power / Ground Plane |Z| vs. Frequency

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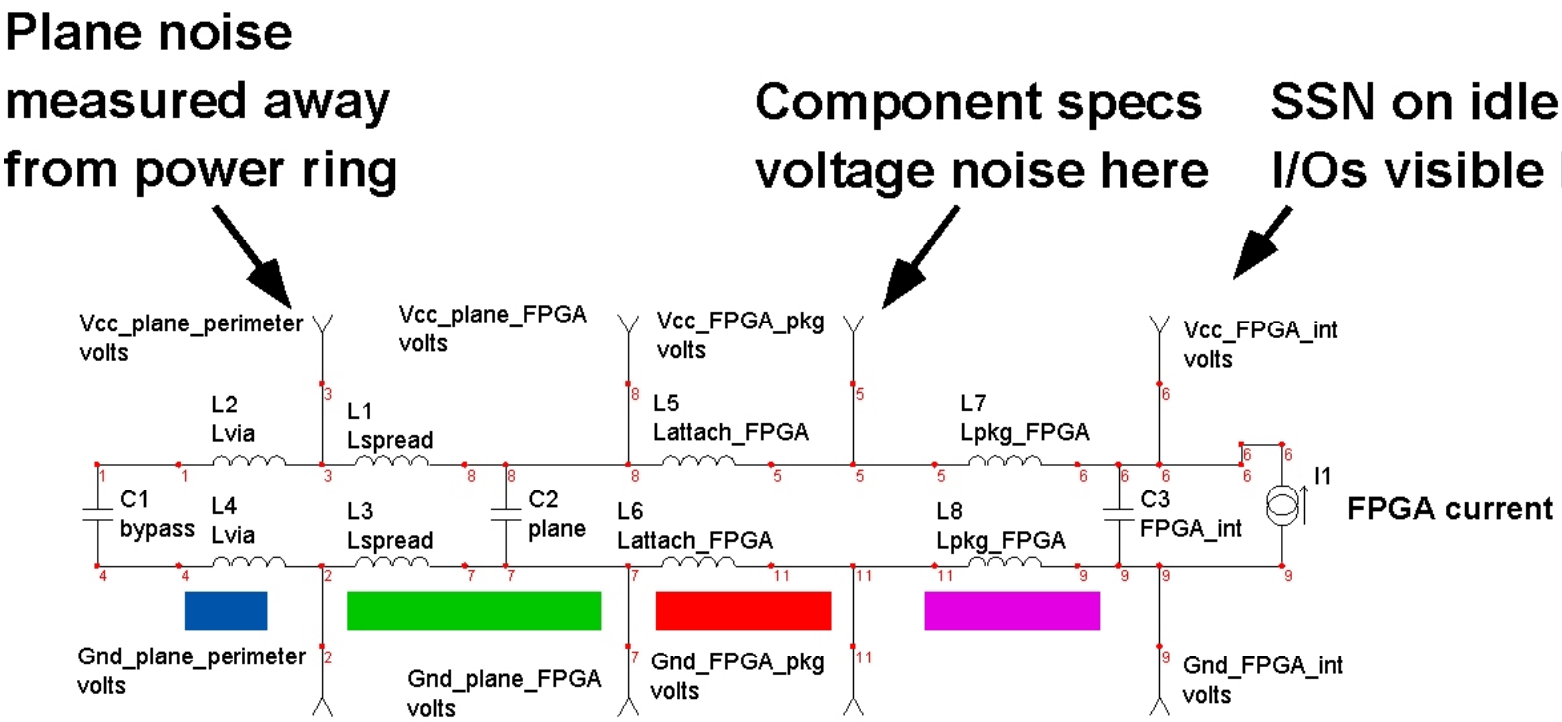
Core Voltage Bypass Path Model



FPGA attachment, plane spreading, and capacitor attachment via inductance all work to decouple the bypass capacitors from the FPGA.

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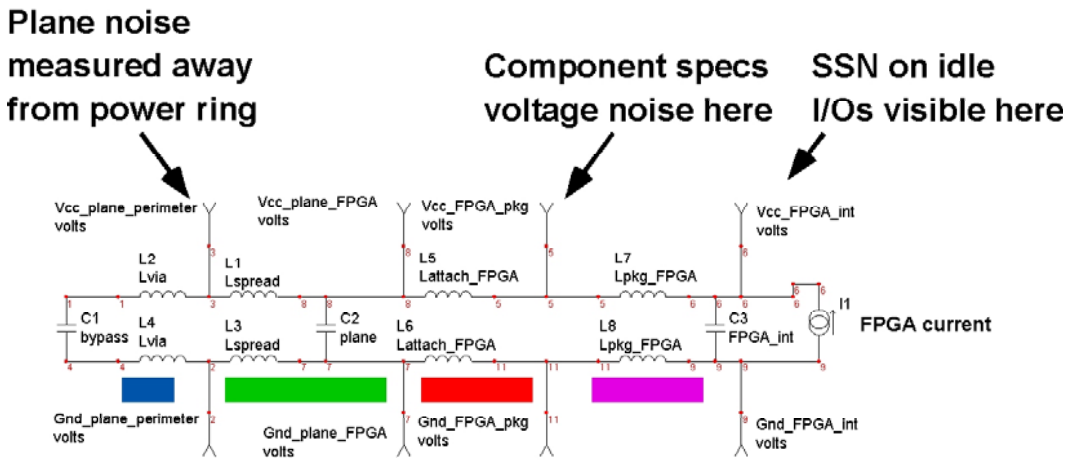
Core Voltage Bypass Path Model



FPGA attachment, plane spreading, and capacitor attachment via inductance all work to decouple the bypass capacitors from the FPGA.

- Major elements from left to right:
  - Mounted bypass capacitor inductance
  - Plane spreading inductance
  - IC attachment vias
  - Package inductance w/in-package / on-die capacitance

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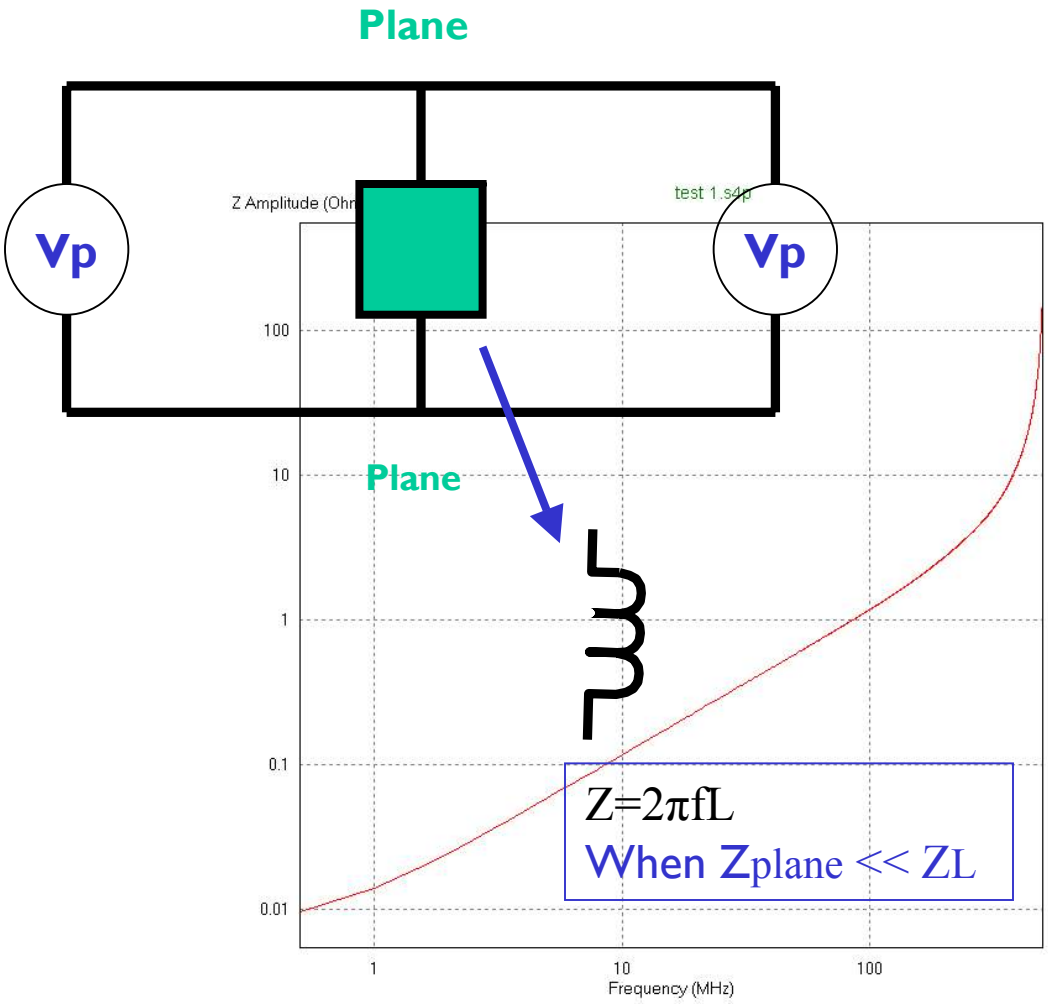
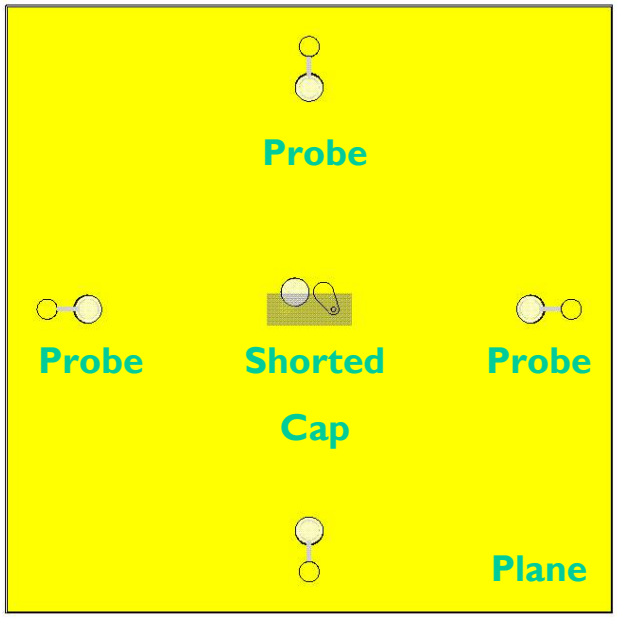
Mounting Inductance Extraction with Transfer Impedance





Same method used with VNA for measurement of PCB impedance.

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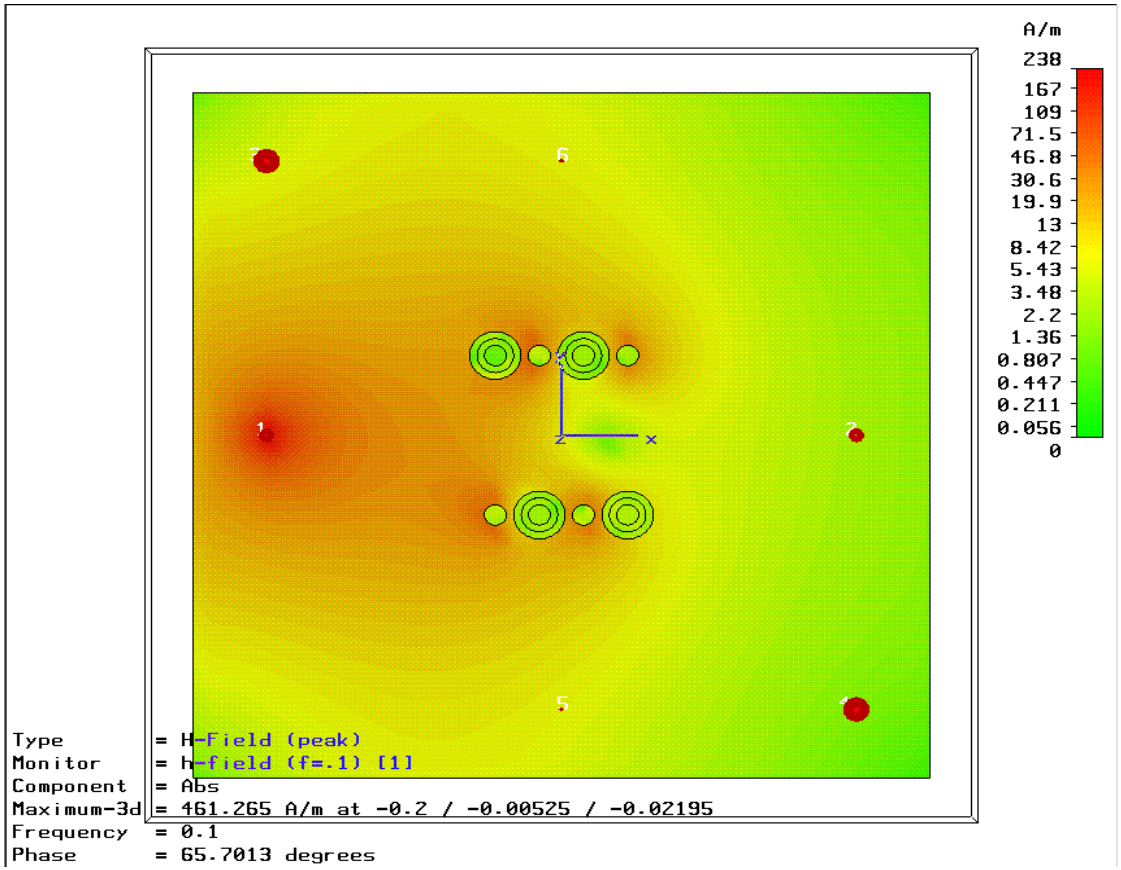
Example H-field Distribution Port 1 Driven 100 MHz

- Significant B well beyond the capacitor and port



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Via Partial Inductance

- Two components:
  - Between the planes, this is the entire cavity
    - Varies as $\ln(2/K_1)$
  - Above the top most plane in the cavity
    - Greater than linear sensitivity to via diameter versus separation
    - Square sensitivity to height

$$5.08nH * ((H_1^2 * (2 - K_1) / (S * K_1)) + (2 * H_2 * \ln(2 / K_1))$$

H_1	Via length above the uppermost plane
H_2	Plane to plane separation
D	Via diameter
S	Via separation, on centers

$$K_1 = D/S$$

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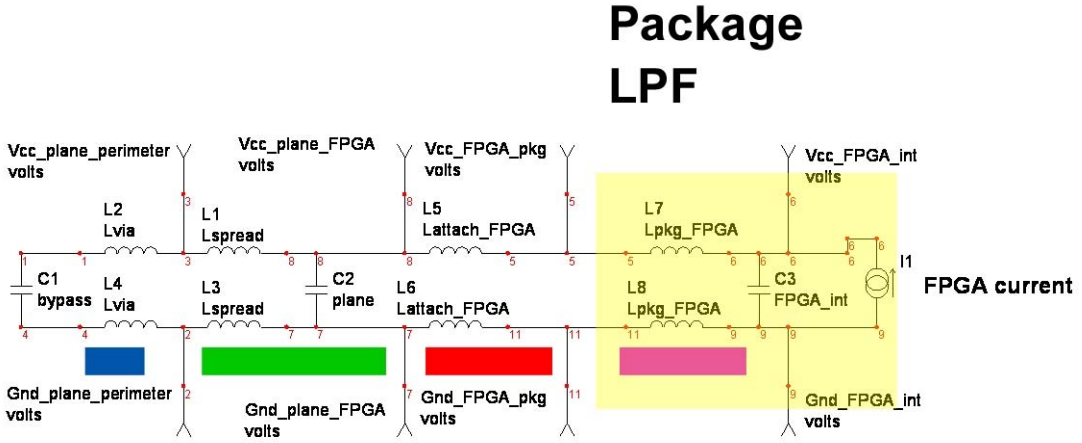
Plane Spreading Inductance

- Plane spreading inductance:
  - $L_{PLANE\_CAVITY} = u0 / 2\pi * H * ((\ln(R2/R1) * K_{PERF}) + \ln(R3/R2))$
  - u_0 = 31.9nH/square
  - H = cavity height
  - R3 = radius from die center to bypass cap ring
  - R2 = radius from die center to via field edge
  - R1 = radius from die center to pkg power / ground attachments.
  - K_{PERF} scaling factor for perforation in via field
    - For perforations small compared to wavelength area ratio

IC Package Low Pass Filter

- IC package power / ground interconnect inserts substantial inductance between the device attachment and the die.
- Discrete in-package capacitors or on-die capacitance provides high frequency bypass.



FPGA attachment, plane spreading, and capacitor attachment via inductance all work to decouple the bypass capacitors from the FPGA.

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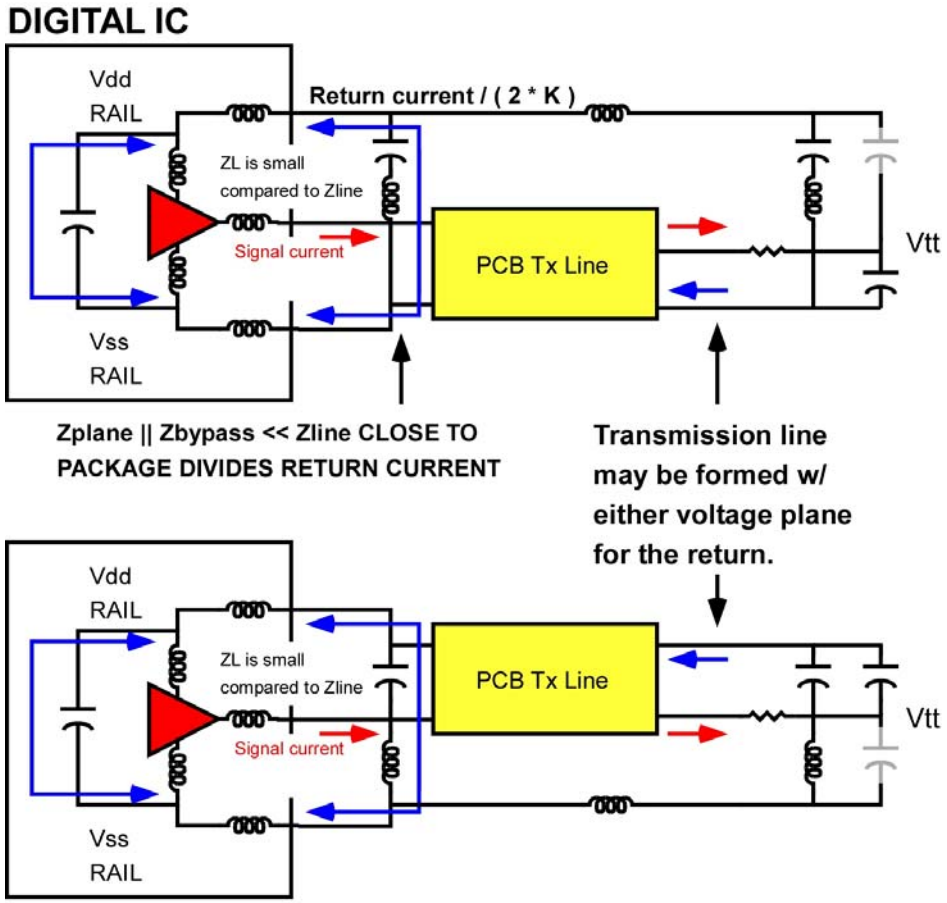
Microstrip Transmission Path



Microstrip Model w/ Parallel Termination

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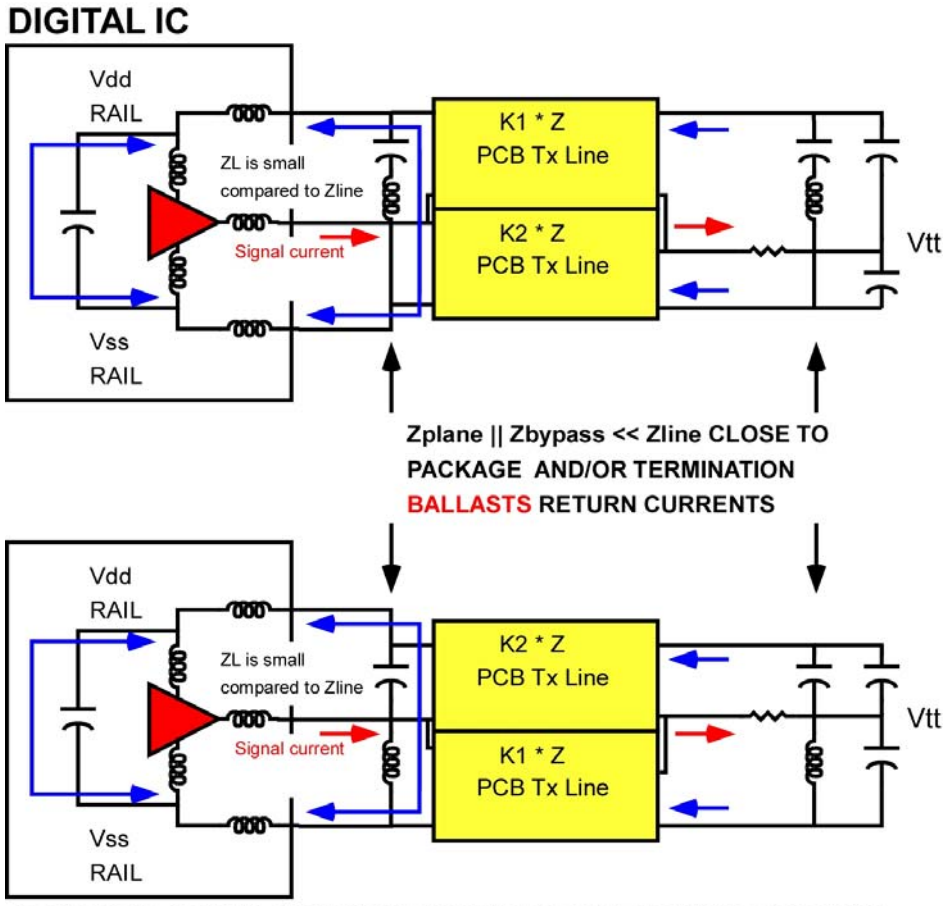
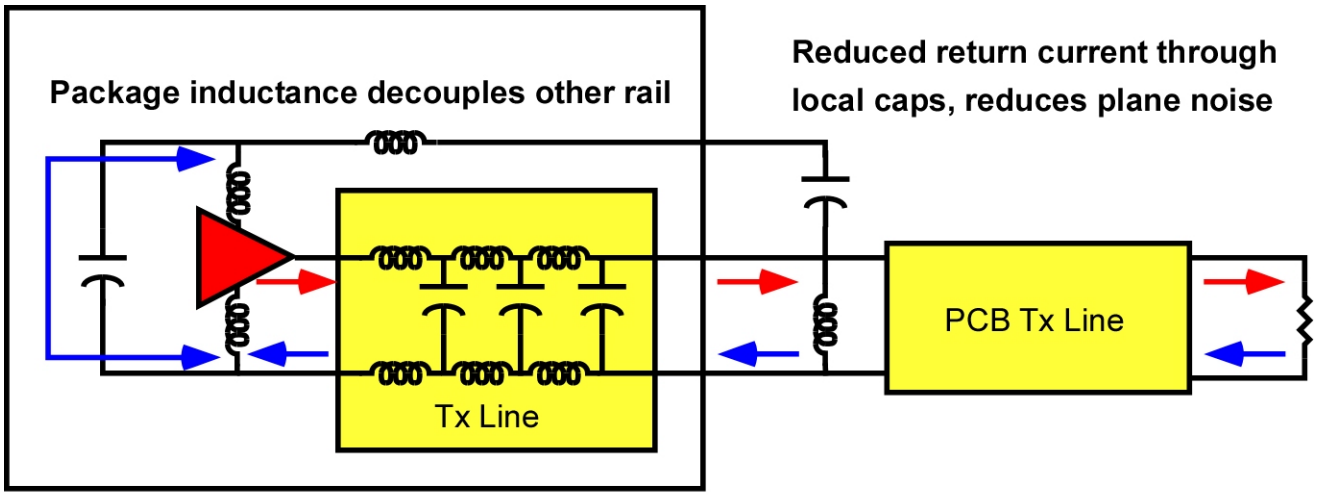
Stripline Transmission Path with Vdd / Vss Voltage Cavity



Offset Stripline Model w/ Parallel Termination

High Speed Transmission Path



In package / on die capacitance still supports switching current

Contiguous transmission line formed from pad through package to PCB to receiver.

High Speed Model w/ Parallel Termination

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Does the Bypass Capacitor Position Really Matter?

For Core Power It depends-

- For $L_{SPREAD} + L_{ATTACH} < 0.5\ L_{CAP}$,within reason, cap position sensitivity is low.
  - Up to 0.5" from BGA perimeter typically < 10% capacitor count impact for like |Z|.
- For $L_{SPREAD} + L_{ATTACH} >= 0.5\ L_{CAP}$ cap position sensitivity rises exponentially.
  - 1" from BGA can double req'd capacitor count
  - Most sensitive on layers closest to IC

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Example Vccint, Conventional MLCC Capacitors

fco	5.00E+07
cap ESL	500
cap via space	0.05
cap vias	2
cap mtd L	982
attach L	10
Lspread 1"	27
Lspread 5"	46

Virtex2/Pro Core Power

S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
...	

Ztarget mohms	100	50	40	30	25	20	18	16
Lbudget pH	318	159	127	95	80	64	57	51
Radius "								
1	4	9	11	17	23	37	48	70
1.2	4	9	12	18	25	40	54	82
1.5	4	9	12	19	26	45	63	105
2	4	9	12	20	29	53	80	163
3	4	9	13	22	33	71	129	781
5	4	10	14	25	42	124	613	9999
Lattach+Lspread	12%	23%	29%	38%	46%	58%	64%	72%
Cap increase	0%	11%	27%	47%	83%	235%	1177%	14184%

- @ Low performance, capacitor position does not matter.
- As performance increases, position becomes increasingly sensitive.
- Near 50% Lattach + Lspread, 1"-1.5" yields only 10% penalty.

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Example Vccint w/Low ESL Caps

fco	5.00E+07
cap ESL	100
cap via space	0.03
cap vias	6
cap mtd L	225
attach L	10
Lspread 1"	27
Lspread 5"	46

Virtex2/Pro Core Power

S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
…	

Ztarget mohms	100	50	40	30	25	20	18	16
Lbudget pH	318	159	127	95	80	64	57	51
Radius "								
1	1	2	3	4	6	9	11	16
1.2	1	2	3	4	6	10	13	19
1.5	1	2	3	5	6	11	15	24
2	1	2	3	5	7	12	19	38
3	1	3	3	5	8	17	30	179
5	1	3	4	6	10	29	141	9999
Lattach+Lspread	12%	23%	29%	38%	46%	58%	64%	72%
Cap increase	0%	50%	33%	50%	67%	222%	1182%	62394%

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Example Vcco

fco	5.00E+07
cap ESL	500
cap via space	0.05
cap vias	2
cap mtd L	1361
attach L	70
Lspread 1"	54
Lspread 5"	73

Virtex2/Pro I/O Power	
S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
...	

Ztarget mohms	100	90	85	80	75	70	60	55
Lbudget pH	318	286	271	255	239	223	191	175
Radius "								
1	8	9	10	11	12	14	21	27
1.2	8	9	10	11	13	15	22	30
1.5	8	9	10	12	13	16	24	33
2	8	10	11	12	14	17	27	40
3	9	10	12	13	16	19	34	54
5	9	11	13	15	18	23	47	104
Lattach+Lspread	39%	43%	46%	49%	52%	56%	65%	71%
Cap increase	13%	22%	30%	36%	50%	64%	124%	285%

- **Half-plane and deeper plane positions, greatly limit practical |Z|.**
- **One capacitor / Vcco power pin is about right for practical upper performance.**
- **Eight Vcco would require almost 100 capacitors for modest 75mohms.**

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Example Vcco w/Low ESL Caps

fco	5.00E+07
cap ESL	100
cap via space	0.03
cap vias	6
cap mtd L	323
attach L	70
Lspread 1"	54
Lspread 5"	73

Virtex2/Pro I/O Power	
S	1.4 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vccint	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
Vcco	1.4 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
S	0.7 Cu / 3.0 dielectric
GND	1.4 Cu / 3.0 dielectric
...	

Ztarget mohms	100	90	85	80	75	65	60	55
Lbudget pH	318	286	271	255	239	207	191	175
Radius "								
1	2	2	3	3	3	4	5	7
1.2	2	3	3	3	3	5	6	7
1.5	2	3	3	3	4	5	6	8
2	2	3	3	3	4	5	7	10
3	2	3	3	4	4	6	8	13
5	3	3	3	4	5	8	12	25
Lattach+Lspread	39%	43%	46%	49%	52%	60%	65%	71%
Cap increase	50%	50%	0%	33%	67%	100%	140%	257%

- **Low ESL caps reduce capacitor count to far more acceptable values.**

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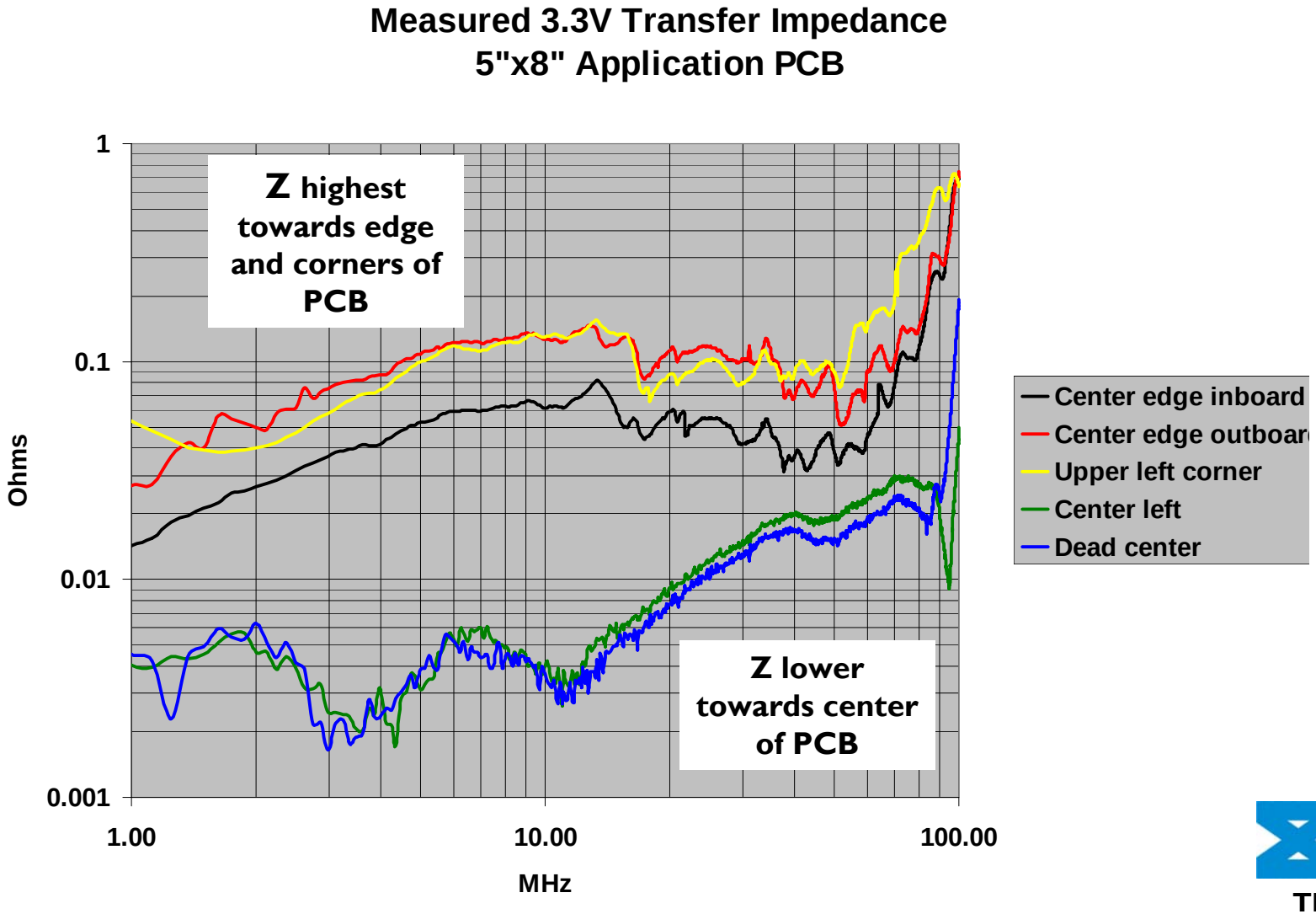
Example Measured |Z| Variation



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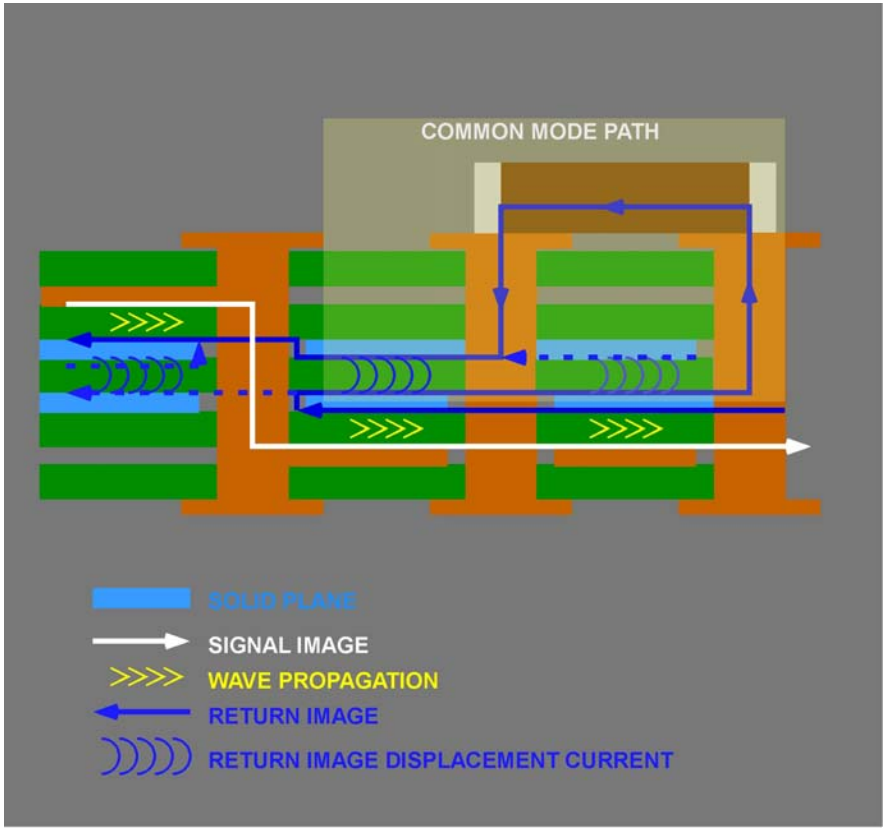
Does Position Matter for EMC?

- Cavity characteristic |Z| in FR4:
  - 188 mohms / mil, ie .57ohms @ 3mils
  - Capacitor inductance limits effectiveness
- As shunt for return currents when changing return planes:
  - Some common mode current will flow on outer surfaces of capacitor planes.
    - If either surface is not buried within another plane cavity radiation results
  - Capacitors closer to signal transition vias limits cavity displacement current area

Does Position Matter for EMC?

- Bypass capacitors provided for signal returns are subject to the same effects as ground vias.
  - Location within a moderate radius to signal vias helps raise cavity SRF.
    - Referencing high speed signals to multiple or poorly chosen returns is a bad idea that capacitors can't fix.
  - Benefit is strongest for planes close to capacitor surface.
- Small devices relatively ineffective due to high |Z| at all frequencies
  - Archambeault et-al

Does Position Matter for EMC?



•Signals that change reference plane voltages, have large CM paths through bypass caps.

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Does Position Matter for EMC?

- Some signal energy couples into cavity, even when signal does not reference surface within the cavity
- This remaining energy propagates towards the board edges
- Via fences and/or bypass capacitors reflect the energy back into the board
  - Limited by via and/or capacitor inductance

Does Position Matter for EMC?

- Cavity excitation may be limited by proper signal return referencing.
  - All planes are not equal!
- Outer ground planes reduces benefit of edge stitching capacitors
- A lossy, non reactive solution to terminate planes would be nice

Summary

- For core power, capacitor position becomes significant as performance rises, but for realizable systems is still not critical within 0.5” of a typical BGA perimeter.
- For EMC, capacitor position is significant to common mode current reduction where signals transition from one plane to another where the planes are different voltage rails.

Summary

- Good design practice limits the strain placed on capacitor position for EMC:
  - Pick the right return plane
  - Run highest frequency signals E/W – N/S on opposite sides of the same plane, or planes of the same voltage with matching stitch vias for the return currents.
- A purely resistive "plane edge termination" would be nice, but does not exist today.

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