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Presented by: Dale L. Sanders

Reducing Switching Transients from ICs in Power Distribution Systems (PDS) on PCBs

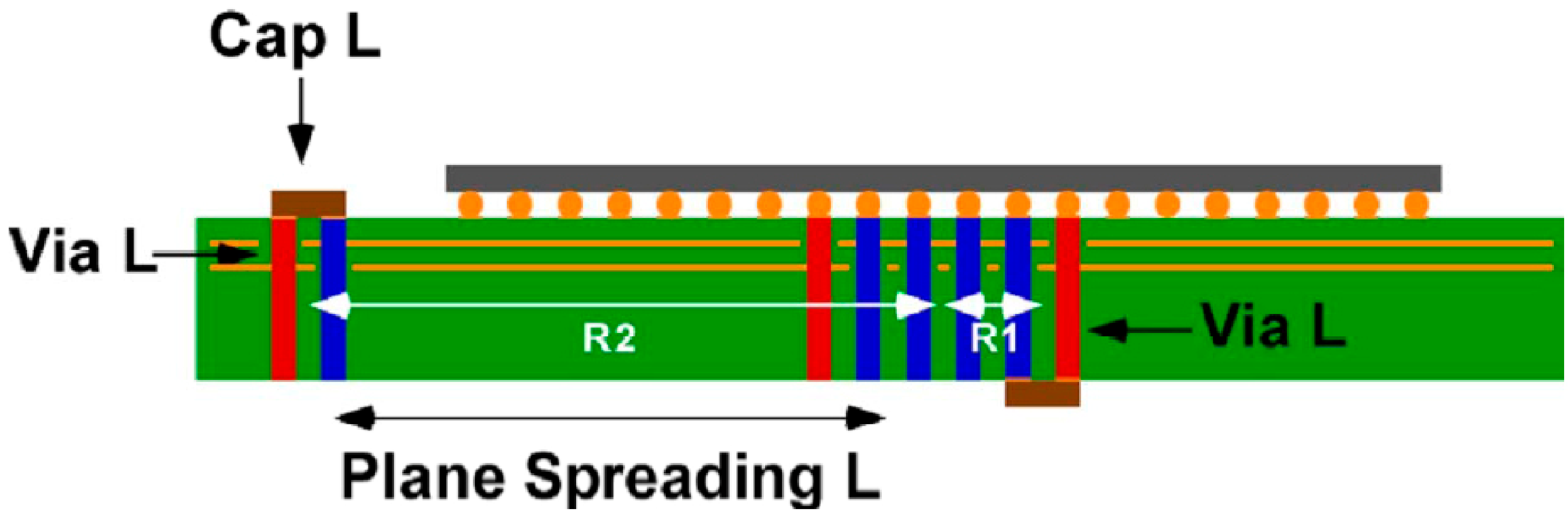
Basic PDS Model – Source, Path, Receiver

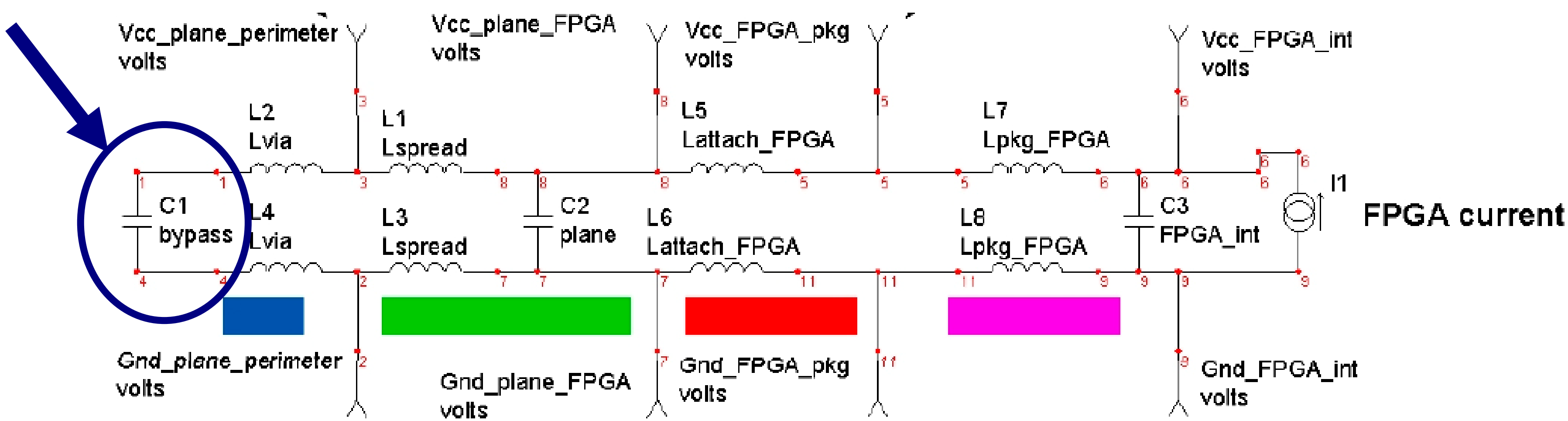
- Source – power supplied to PCB
- Path – PCB planes
- Receiver – ICs
- Ensure "clean" power
  - Supply instantaneous current for switching IC
  - Filter high frequency transients
  - Capacitors
    - Large value Caps – supply energy
    - High Freq. Caps – Filter

What are PDS design issues?

- Inductance
  - Caps
  - Vias
  - Component mounting
  - PCB plane
  - Package
- PCB real-estate
  - Number of caps & vias
  - Location/effectiveness
  - Placement cost
  - Multiple power planes
- Signal Integrity (SI)
  - Number of vias (routing)
  - Manufacturing cost (multiple plane PCBs)
  - Functionality

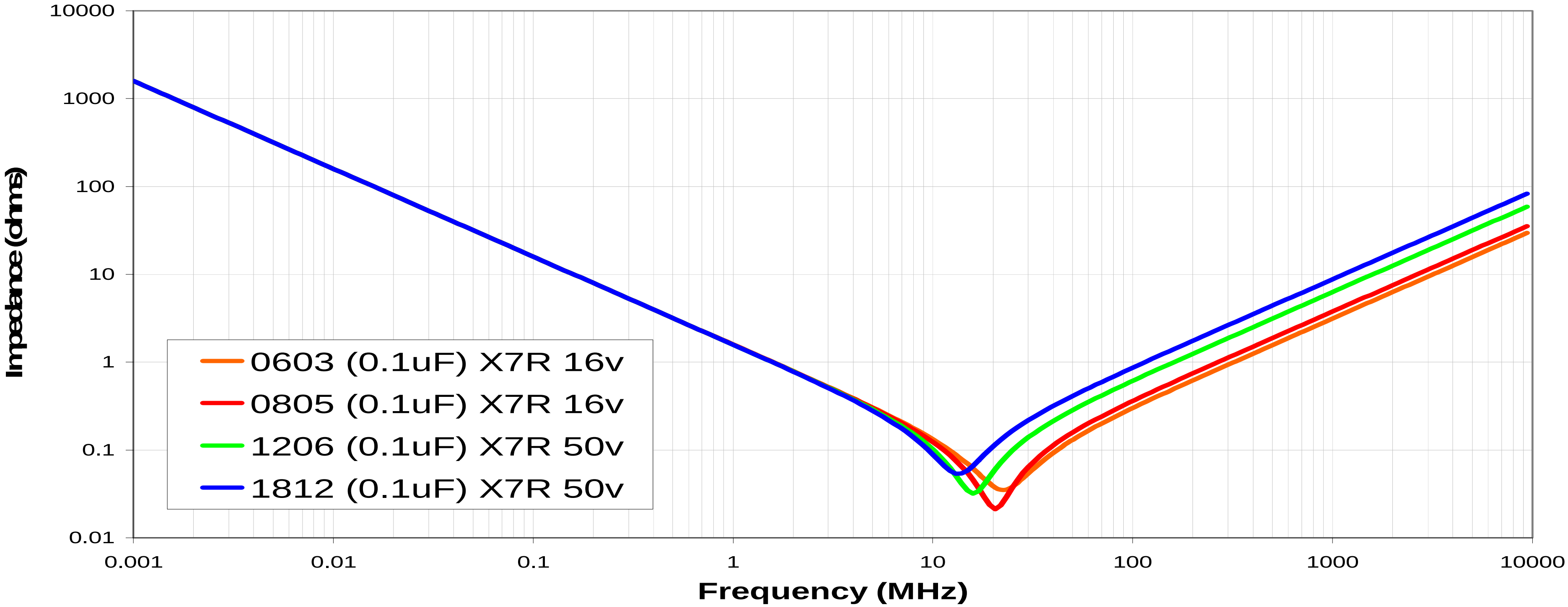
Power Distribution System (PDS) [EXAMPLE]





Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, “High Performance FPGA Bypass Filter Networks,” DesignCon 2005, Santa Clara, CA, February 2005.

Inductance – Typical Cap Approach

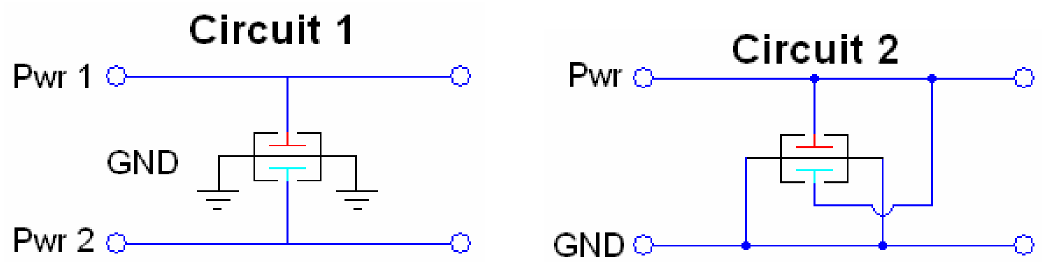


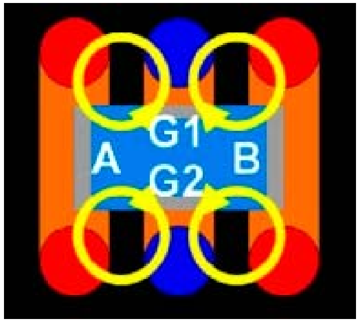
- Smaller is better – 0603 has less inductance than 0805, 1206, 1812.
- To meet total capacitance requirements typically small caps increase the number of caps needed. (Package size limits number of layers.)
- Larger number of caps require more vias & greater distance from IC. (More PCB space)

D.L. Sanders, J.P. Muccioli, A.A. Anthony, and D.J. Anthony, "X2Y® Technology Used for Decoupling," Published by the IEE, New EMC issues in Design: Techniques, Tools and Components Event Symposium, April 28, 2004.

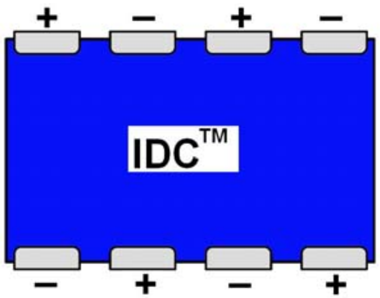
Integrated Passive Device (IPD)

- **X2Y® Technology**
  - Capacitive Circuit
    - Circuit 1 – 3 conductor
    - Circuit 2 – 2 conductor
  - 4 terminal device
  - Layout attachment is inter-digitated
  - Unless noted, X2Y® is Circuit 2 for this presentation





- **IDC™**
  - 8 terminal device
  - Terminals are inter-digitated

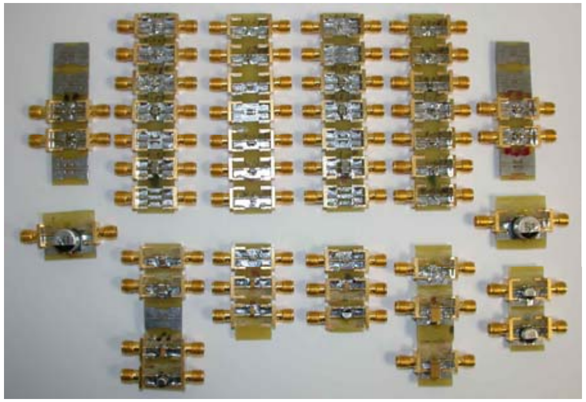


Technology In Balance
WHERE SIGNAL INTEGRITY MEETS EMC

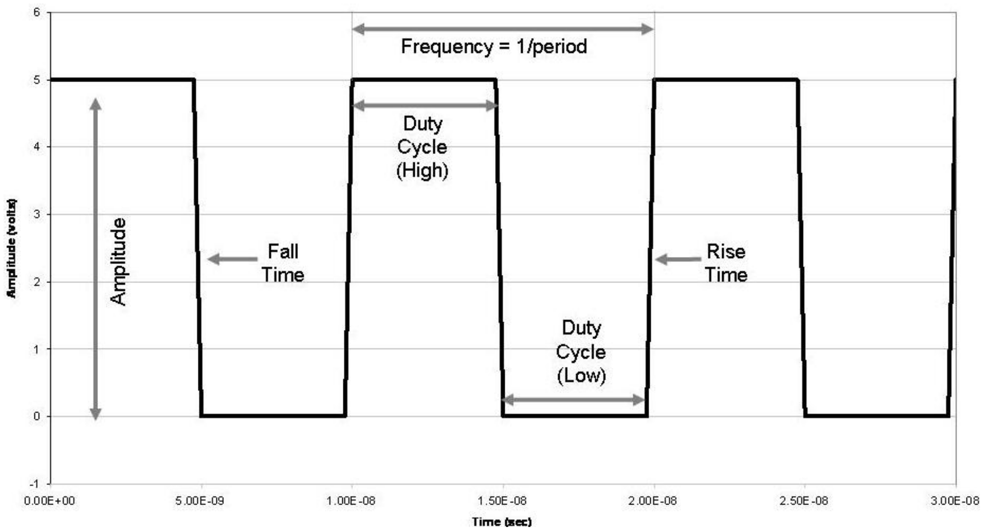
Cap-only Performance Test Set-up

- Caps mounted to 50 ohm coplanar PCB.
- Shunt-through measurements
- Input waveform below

Duty Cycle	Frequency
➢ 50/50	➢ 100 kHz
➢ 80/20	➢ 1 MHz
	➢ 10 MHz
Rise/Fall time	**Amplitude**
➢ 1 ns	➢ 5 V
➢ 5 ns	➢ 2.2 V

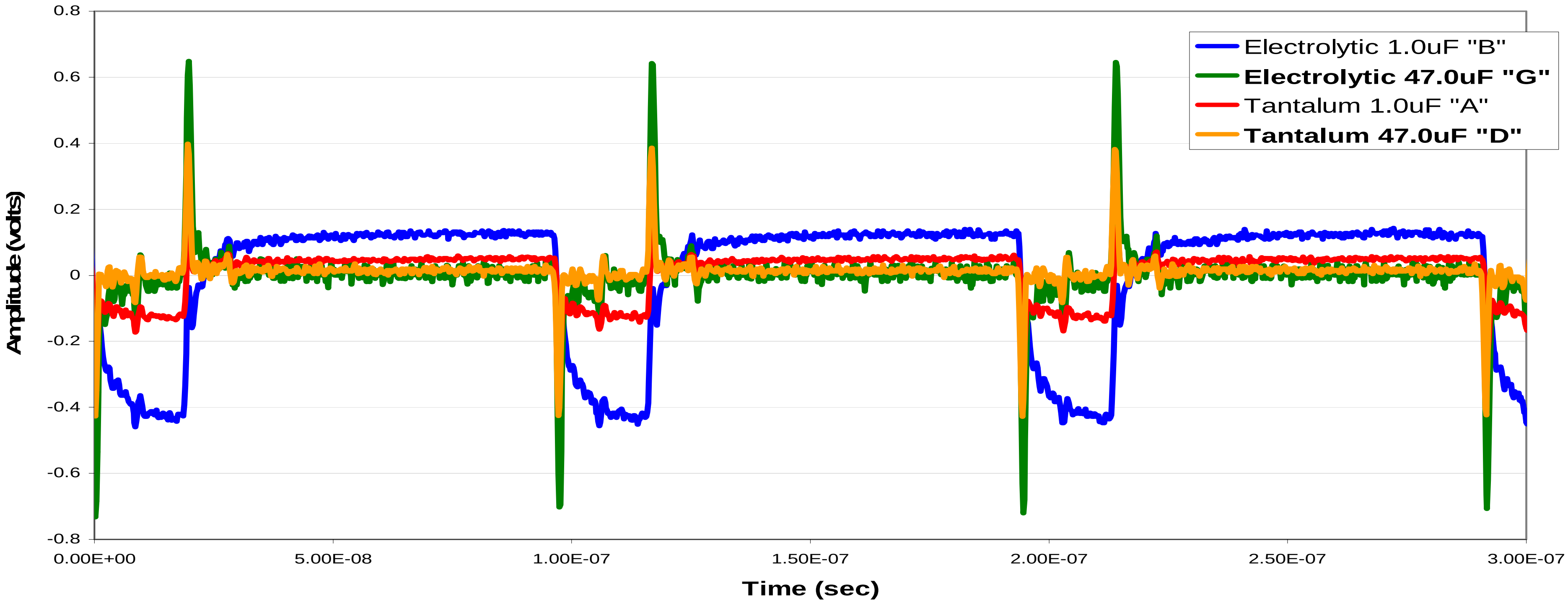


DUTs					
Type	Cap. Value (uF)		Volt. Rating (VDC)	Dielectric	Package
Aluminum electrolytic Capacitor	1.0		50	AL EL	B
Aluminum electrolytic Capacitor	2.2		50	AL EL	B
Aluminum electrolytic Capacitor	4.7		50	AL EL	C
Aluminum electrolytic Capacitor	10		50	AL EL	D
Aluminum electrolytic Capacitor	47		50	AL EL	G
Aluminum electrolytic Capacitor	100		50	AL EL	G
Tantalum Chip Capacitor	1.0		16	Tan	A
Tantalum Chip Capacitor	2.2		16	Tan	A
Tantalum Chip Capacitor	4.7		16	Tan	A
Tantalum Chip Capacitor	10		16	Tan	B
Tantalum Chip Capacitor	47		16	Tan	D
Tantalum Chip Capacitor	100		16	Tan	D
MLCC	1.0		10	Y5V	0603
MLCC	2.2		16	Y5V	0805
MLCC	4.7		10	Y5V	0805
MLCC	10		10	Y5V	1206
MLCC	47		6.3	X5R	1210
MLCC	100		6.3	X5R	1812
MLCC	0.1		16	X7R	0603
InterDigitated Capacitors (IDC) MLCC	1.0		10	Y5V	0612
InterDigitated Capacitors (IDC) MLCC	2.2		10	X5R	0612
Reverse Aspect Ratio, MLCC (Low-inductance)	0.22		10	Y5V	0306
Reverse Aspect Ratio, MLCC (Low-inductance)	1.0		10	X5R	0508
Reverse Aspect Ratio, MLCC (Low-inductance)	1.0		16	X5R	0612
	Rated	Total			
X2Y MLCC	0.47	0.94	16	X7R	1206
X2Y MLCC	0.56	1.12	25	X7R	1210
X2Y MLCC	0.47	0.94	63	X7R	1812
X2Y MLCC	0.82	1.64	10	X7R	1206
X2Y MLCC	0.82	1.64	16	X7R	1210
X2Y MLCC	1.0	2.0	25	X7R	1812
X2Y MLCC	5.0	10	10	Y5V	1210
X2Y MLCC	6.5	13	16	Y5V	1210



Sanders, Muccioli, North, and Slattery, " The Quantitative Measurement of the Effectiveness of Decoupling Capacitors in Controlling Switching Transients from Microprocessors," CARTS 2005 USA, Palm Springs, CA, March 2005.

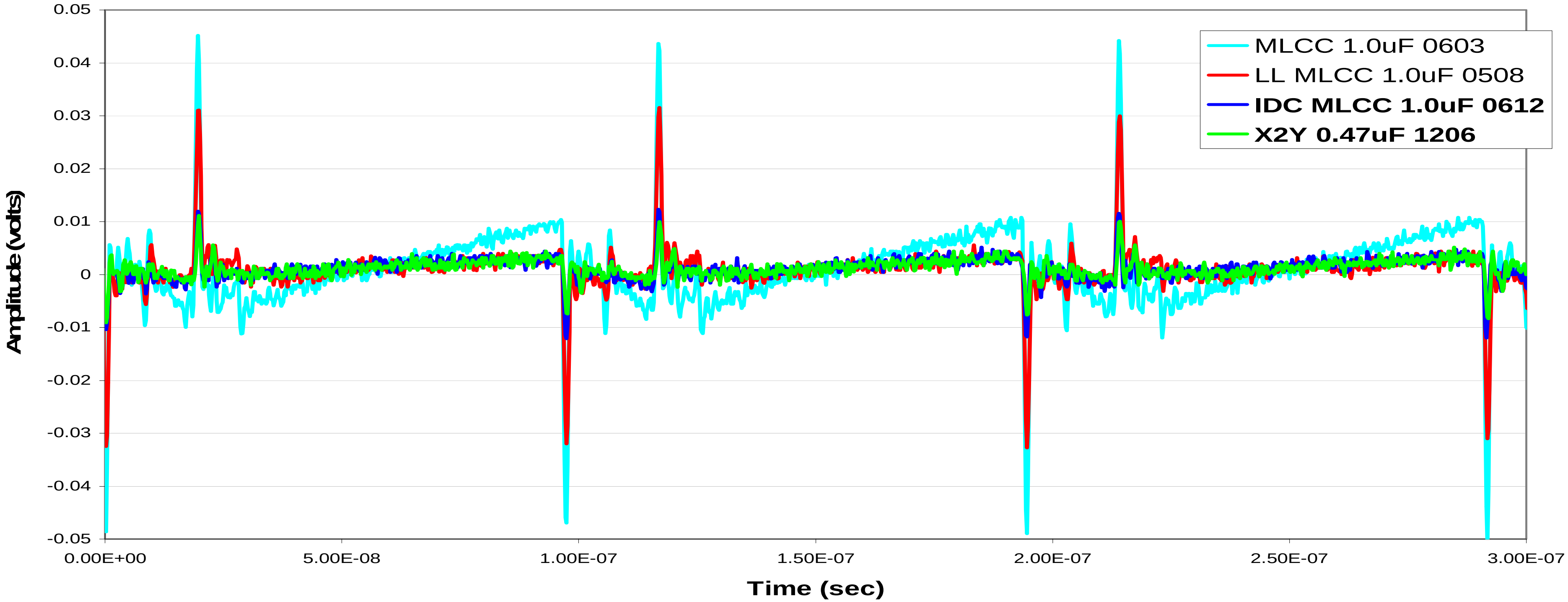
Electrolytic & Tantalum Capacitors



- 80/20 duty cycle, 10 MHz, 1 ns rise/fall time, 5 V amplitude
- 47 uF needed to “smooth” ripple
- Minimal HF transient suppression.

Sanders, Muccioli, North, and Slattery, “ The Quantitative Measurement of the Effectiveness of Decoupling Capacitors in Controlling Switching Transients from Microprocessors,” CARTS 2005 USA, Palm Springs, CA, March 2005.

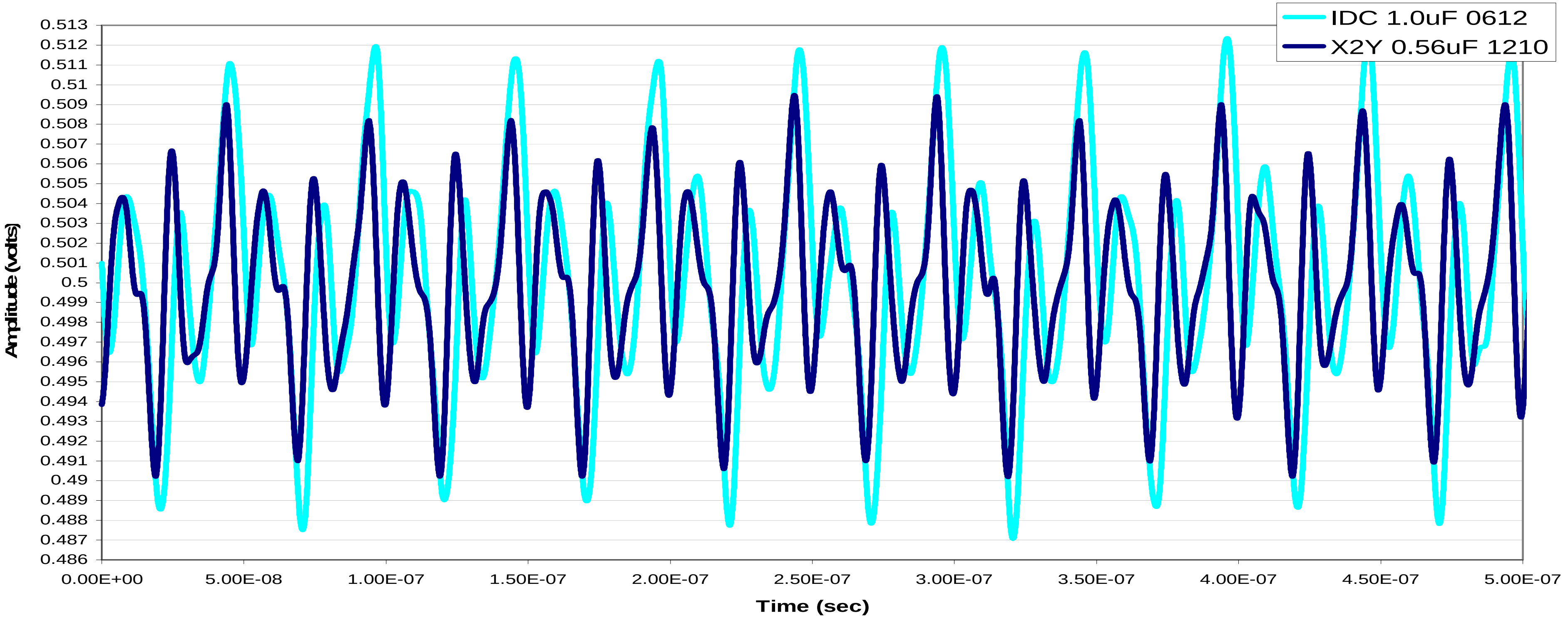
Std. MLCC, Reverse-Aspect-Ratio (LL), IDC™ , X2Y®



- 80/20 duty cycle, 10 MHz, 1 ns rise/fall time, 5 V amplitude
- 1 uF needed to "smooth" ripple
- X2Y® & IDC™ suppress HF transients.
- Note: X2Y total capacitance value = 0.94uF
- Note: Amplitude scale – order of magnitude smaller than previous slide

Sanders, Muccioli, North, and Slattery, " The Quantitative Measurement of the Effectiveness of Decoupling Capacitors in Controlling Switching Transients from Microprocessors," CARTS 2005 USA, Palm Springs, CA, March 2005.

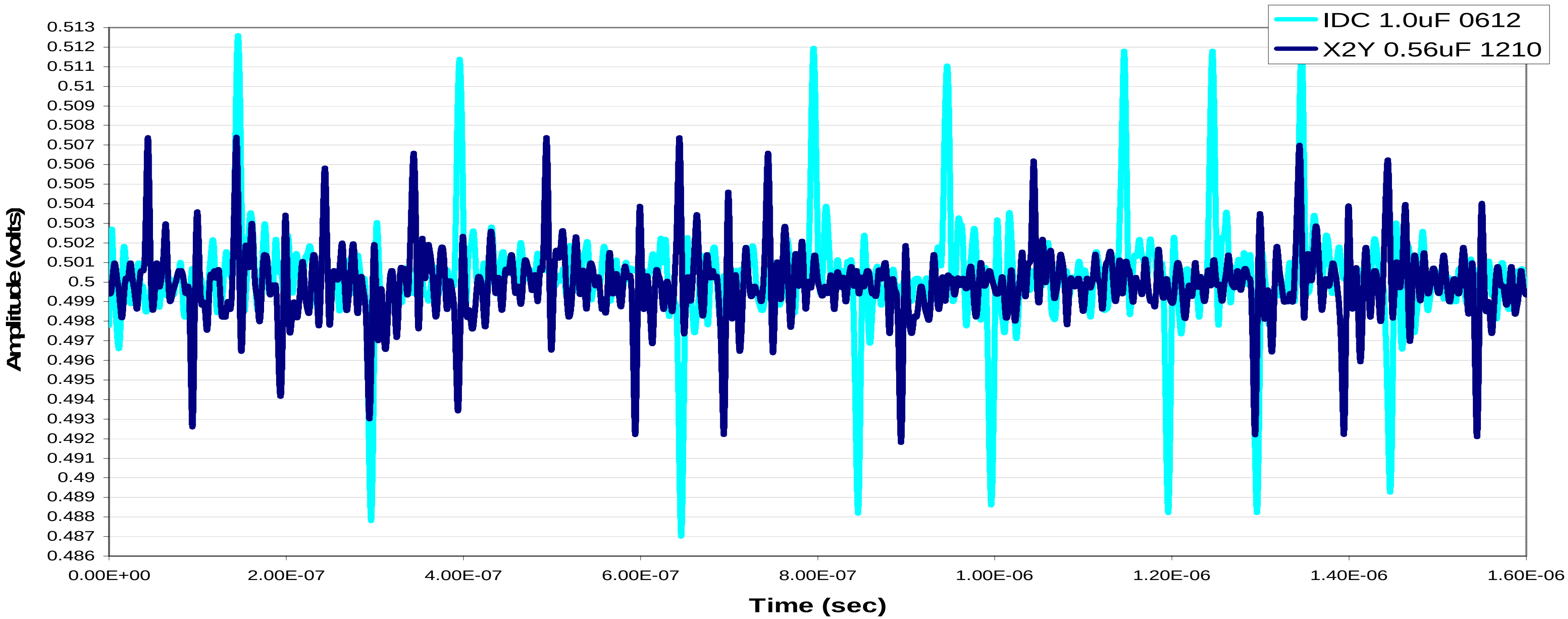
Additional High Frequency Test #1 – 50/50 Clock



- 50/50 duty cycle, 1 GHz, 70 ps rise/fall time
- Note: X2Y total capacitance value = 1.12uF
- Note: Amplitude scale – order of magnitude smaller than previous slide

Data courtesy of Kevin Slattery, Intel Corporation.

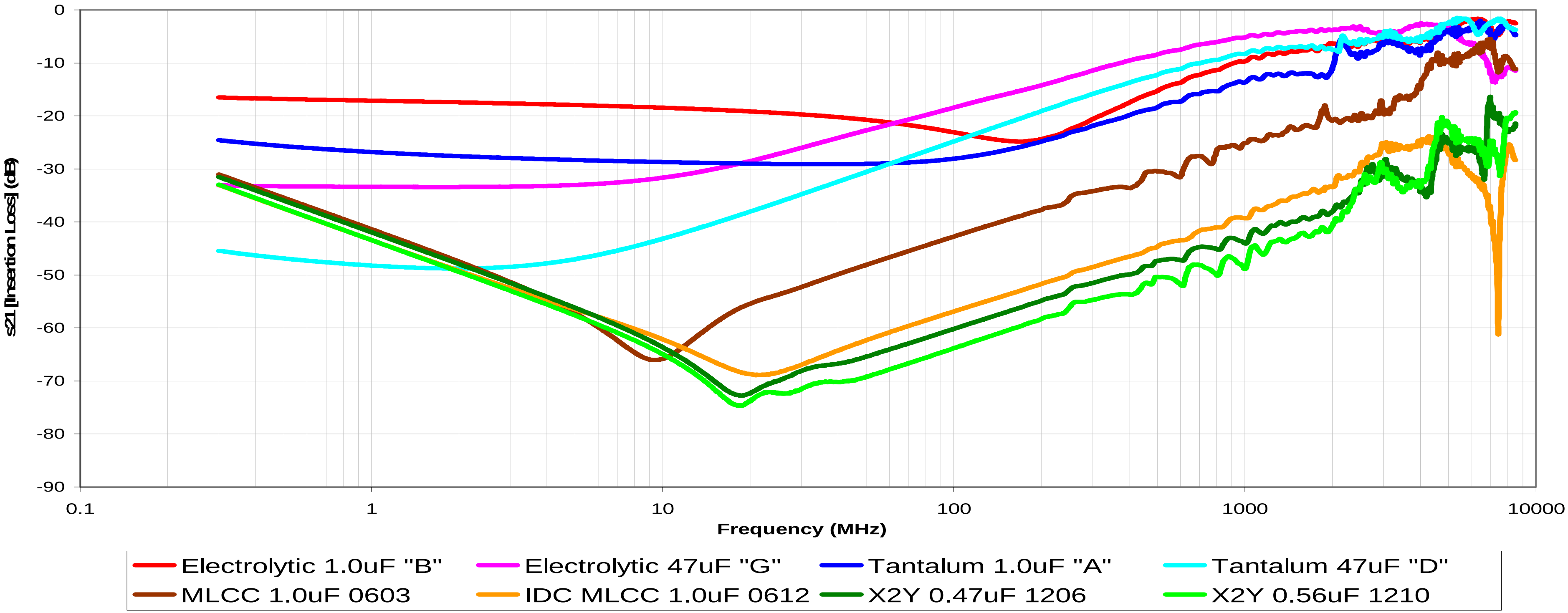
Additional High Frequency Test #2 - Random



- Random duty cycle, 1 GHz, 70 ps rise/fall time
- Note: X2Y total capacitance value = 1.12uF

Data courtesy of Kevin Slattery, Intel Corporation.

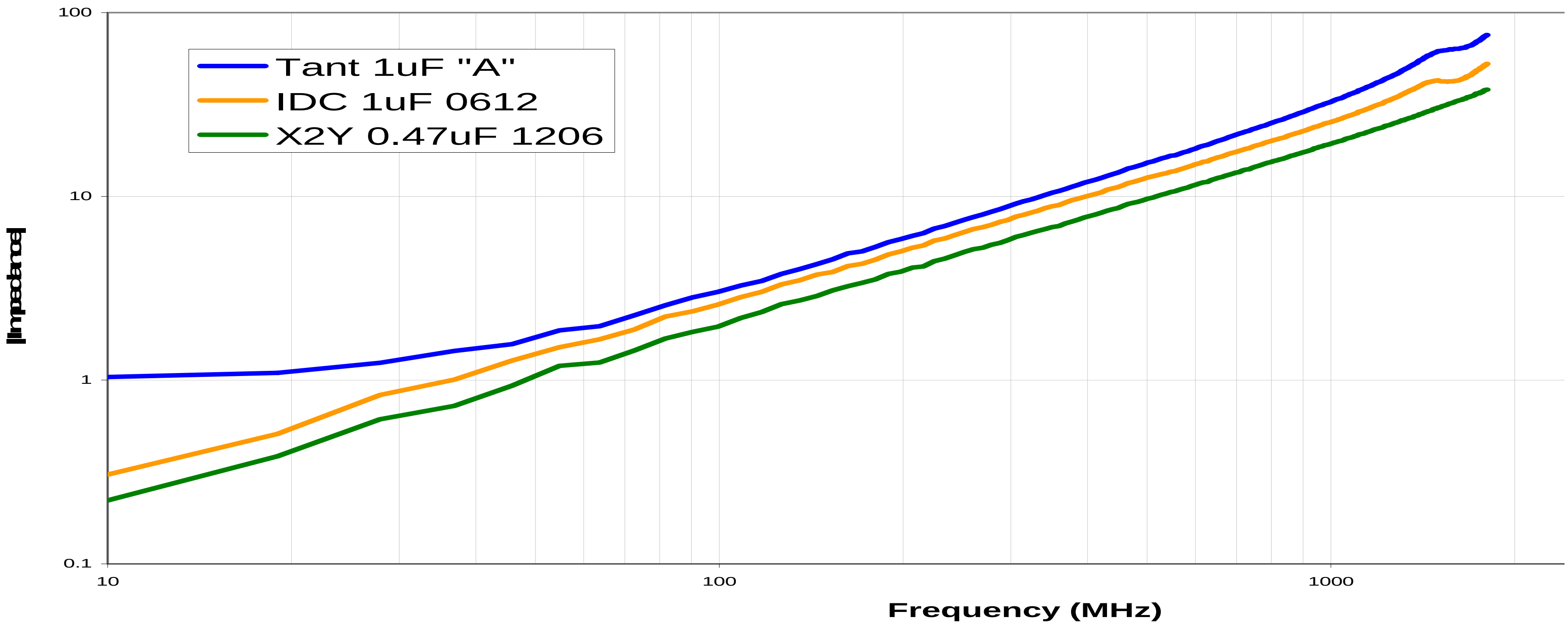
Insertion Loss Measurements



- Insertion Loss (dB) [S21] taken on Agilent ENA 5071A Network Analyzer
- Note: X2Y total capacitance value = 0.94uF & 1.12uF respectively

Sanders, Muccioli, North, and Slattery, " The Quantitative Measurement of the Effectiveness of Decoupling Capacitors in Controlling Switching Transients from Microprocessors," CARTS 2005 USA, Palm Springs, CA, March 2005.

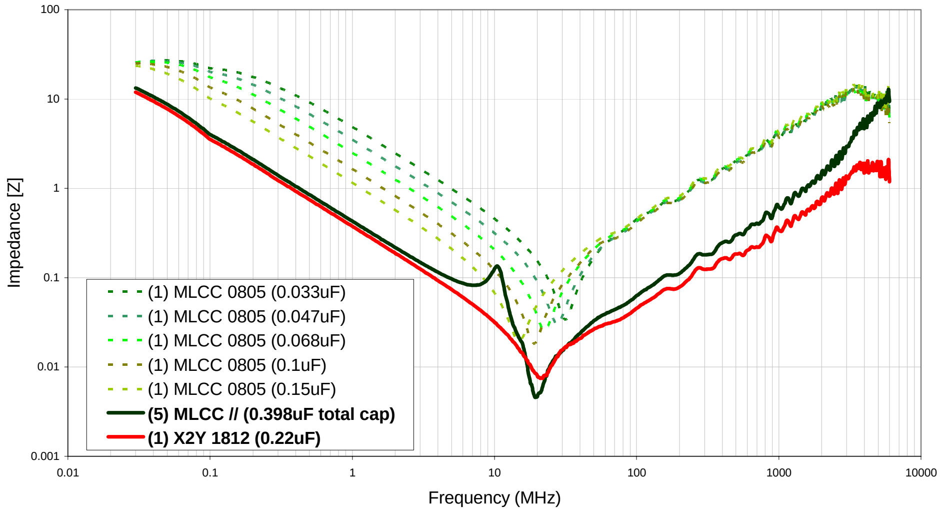
Impedance Measurements

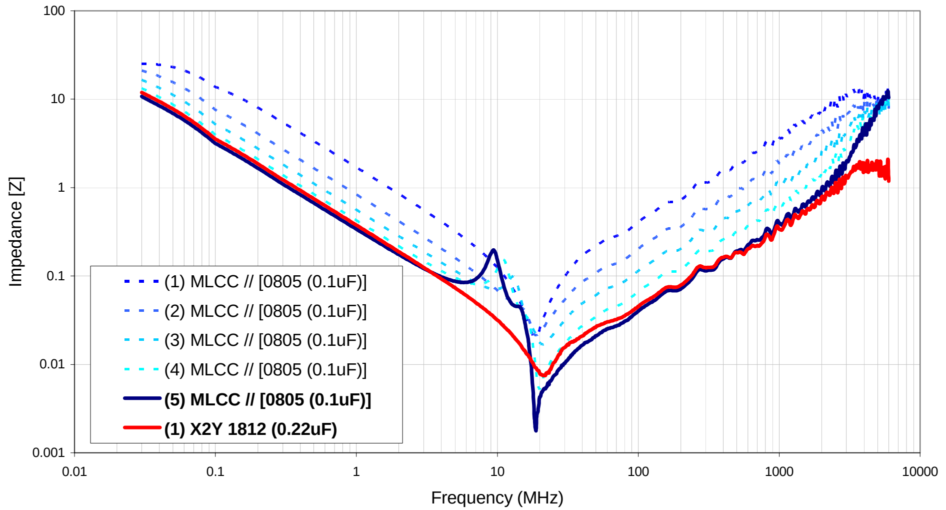


- Impedance measurement taken on Agilent 4396B Impedance Analyzer
- Note: X2Y total capacitance value = 0.94uF

Data courtesy of Kevin Slattery, Intel Corporation.

What is the Performance benefit of Low-Inductive Caps?

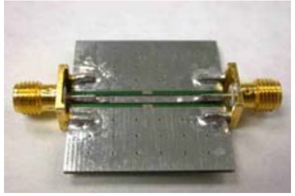




- Each MLCC measured individually
- Total (5) MLCC = 0.398uF
- X2Y total capacitance value = 0.44uF

- MLCC cumulative measured
- Total (5) MLCC = 0.5uF
- X2Y total capacitance value = 0.44uF

- Measurements made on 50ohm Coplanar PCB with Ground Plane.



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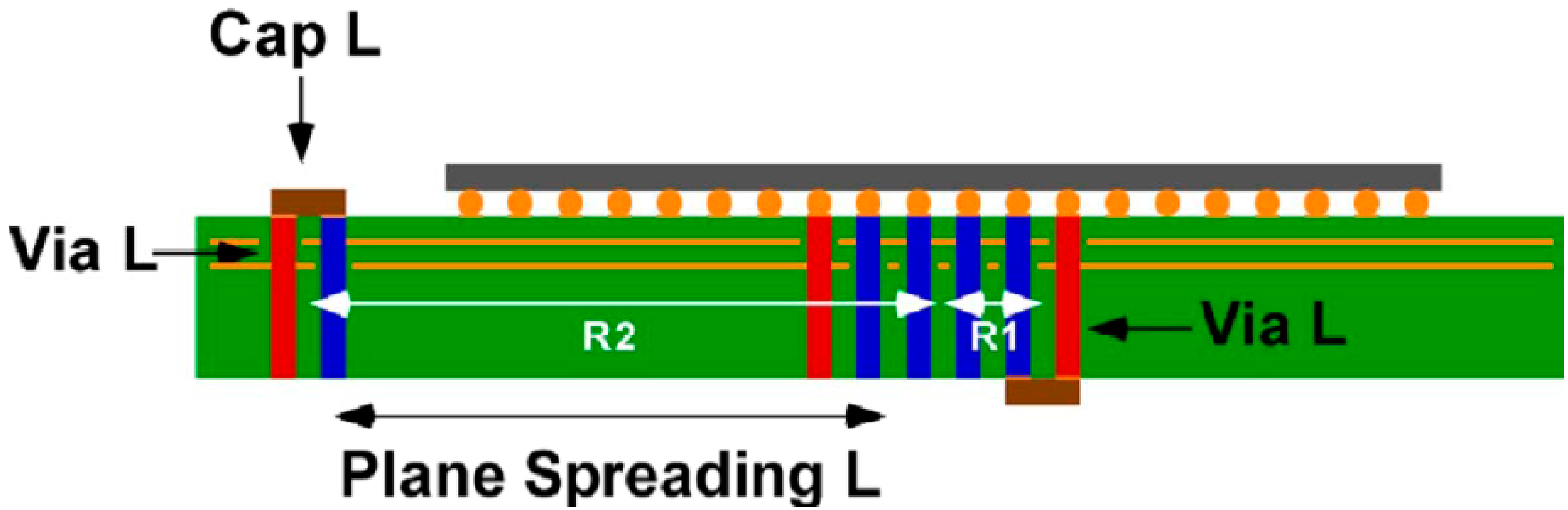
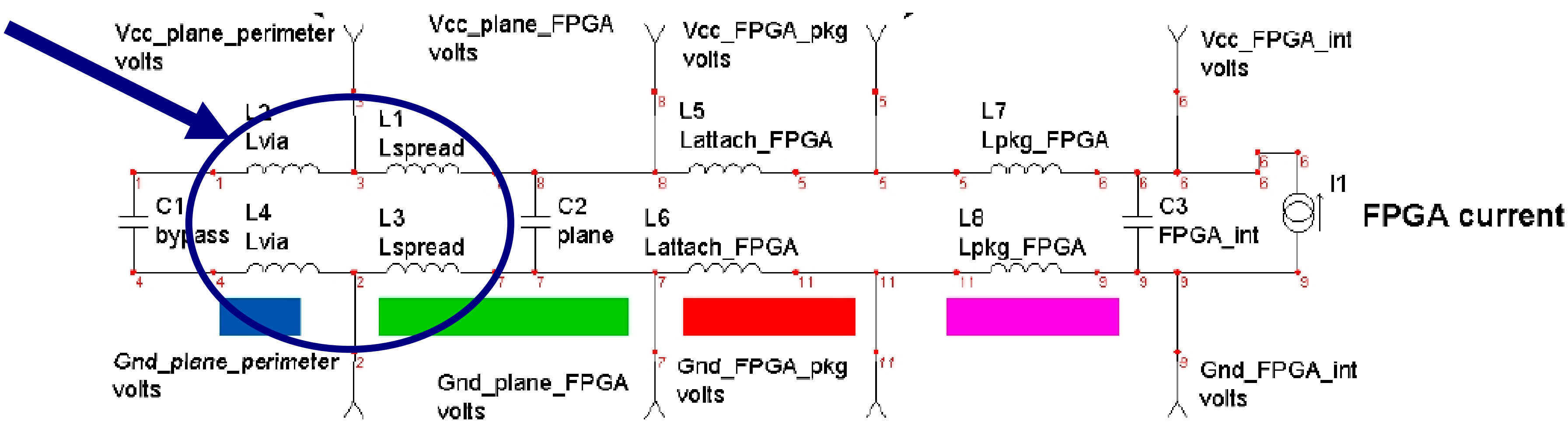
Power Distribution System (PDS) [EXAMPLE]

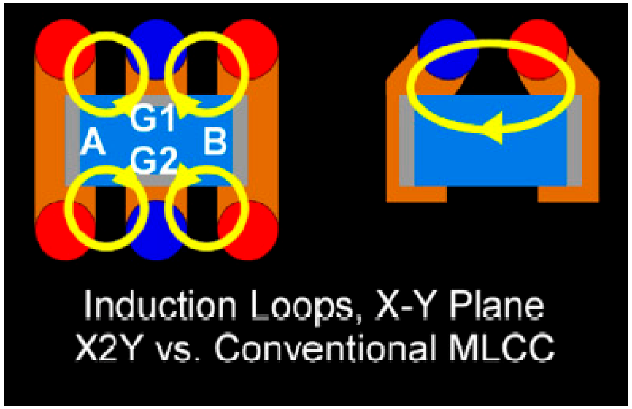




Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

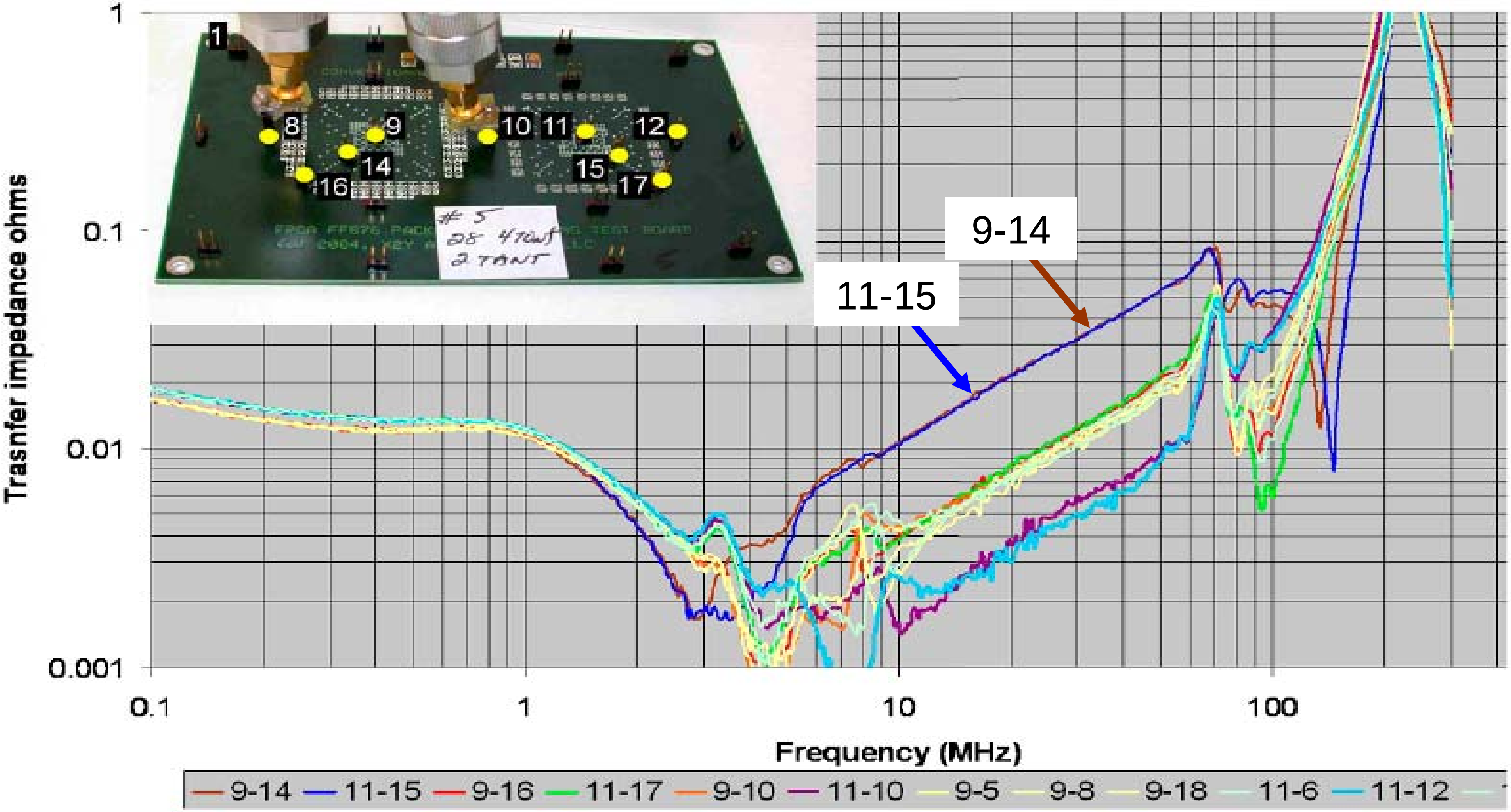
How to Take Advantage of Low-Inductance Caps?

- Lower Via/mounting Inductance
  - Multiple parallel vias
  - Mutual inductance cancellation between vias
  - Reduce trace length from cap to via
- Spreading Inductance
  - Fewer low-inductance caps are required, therefore caps can be located closer to ICs.



Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

What Does Low-Inductance Caps Do for PDS?



- Std. MLCC vs. X2Y® on Xilinx FPGA PCB.

Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

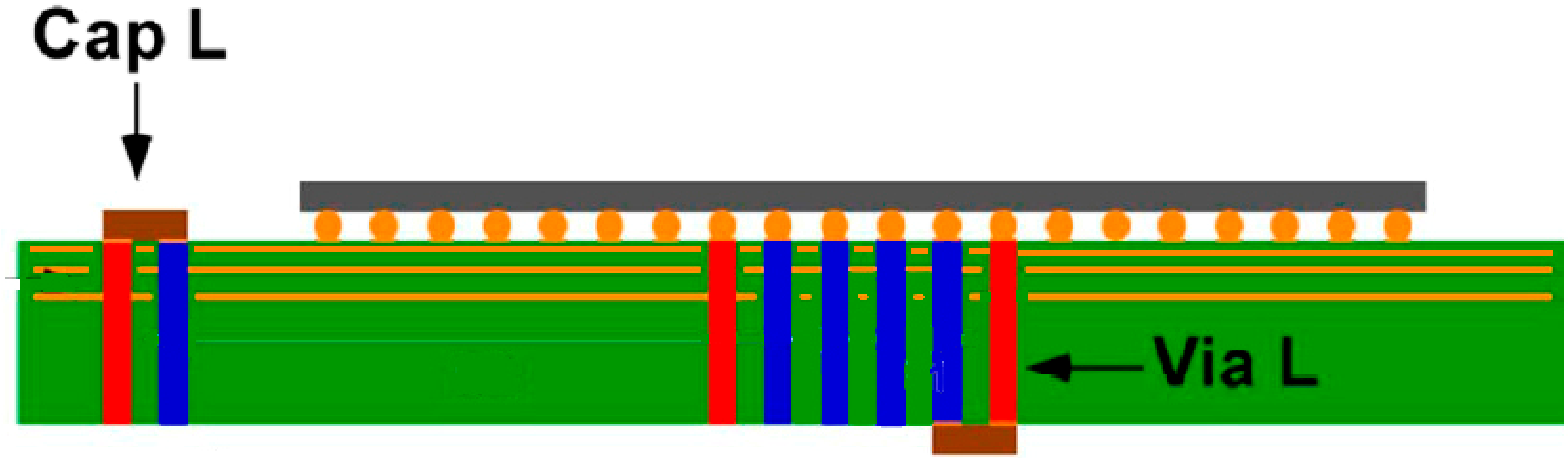
Xilinx FPGA PDS Result

Table 1, Mounted Inductance, Comparative Conventional and X2Y[3]

	Capacitors on Component Side							Capacitors on Back side[4]		
H1	0.005	0.020	0.005	0.020	0.005	0.012	0.012	0.005	0.005	0.005
H2	0.014	0.003	0.003	0.001	0.001	0.038	0.038	0.014	0.003	0.001
S	0.03	0.03	0.03	0.03	0.03	0.032	0.044	0.03	0.03	0.03
D	0.01	0.01	0.01	0.01	0.01	0.02	0.02	0.01	0.01	0.01
K1 D/S	0.33	0.33	0.33	0.33	0.33	0.63	0.45	0.33	0.33	0.33
L / via pH	318	393	76	217	40	590	629	1580	1530	1540
L 0603	1052	1290	662	935	579	1500[5]	1760	3670	3560	3590
L 0402	952	1190	552	835	479	1400	1660	3570	3460	3490
L X2Y	267	355	117	223	90	435	531[6]	1250	1210	1220
Caps req'd 0603	3.9	3.6	5.6	4.2	6.5	3.4	3.3	2.9	2.9	2.9
Caps req'd 0402	3.6	3.3	4.7	3.7	5.3	3.2	3.1	2.9	2.9	2.9
Caps req'd X2Y	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

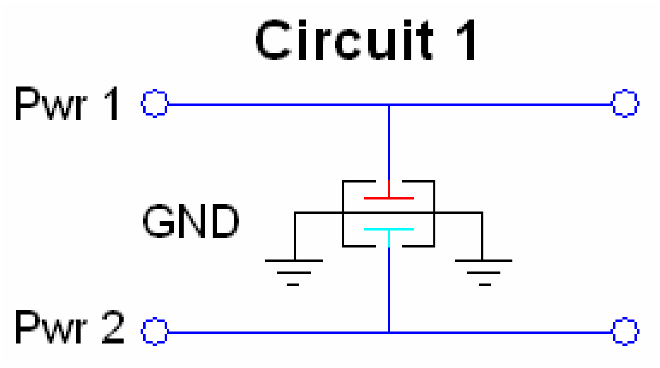
Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.

Multi-Plane PDS Decoupling

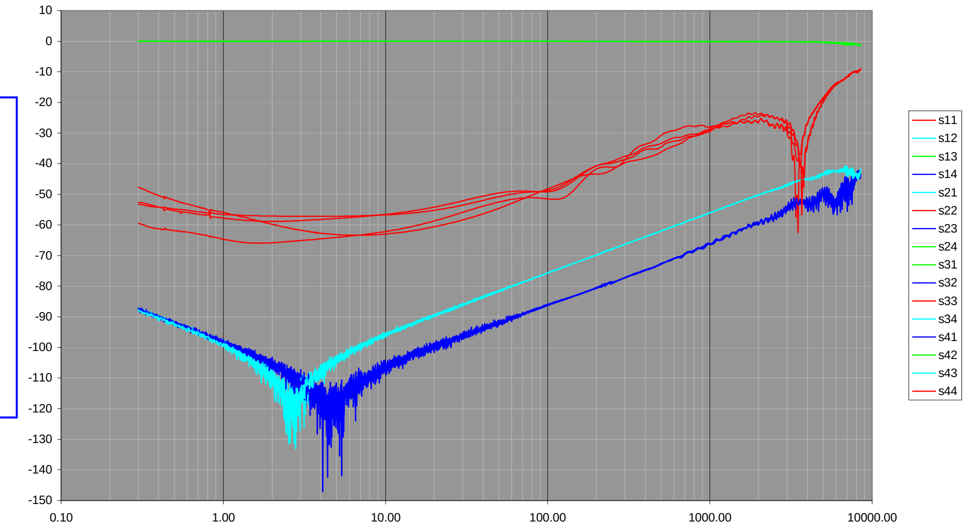


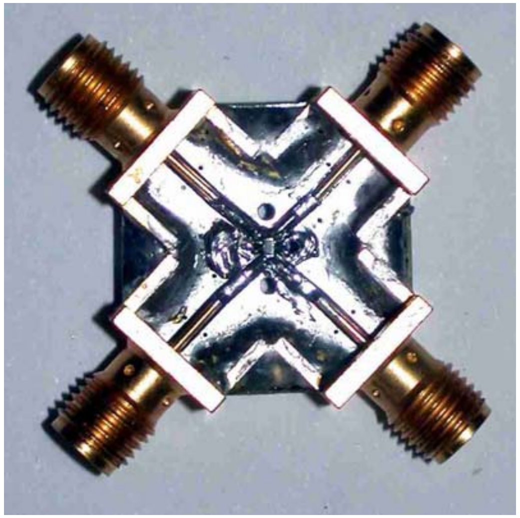
- Decoupling multiple power planes on PCB increases the number of standard caps needed.

Multi-Plane Test Fixture Insertion Loss

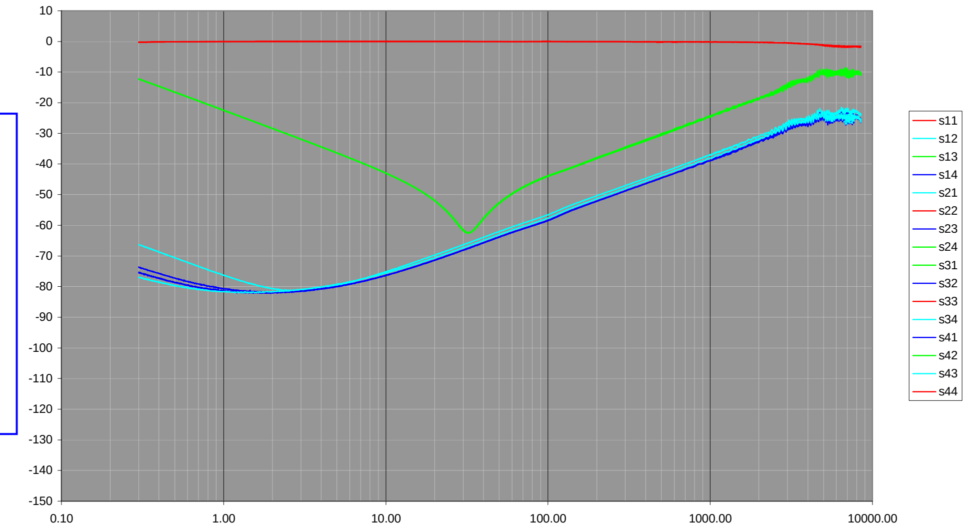


PCB Fixture

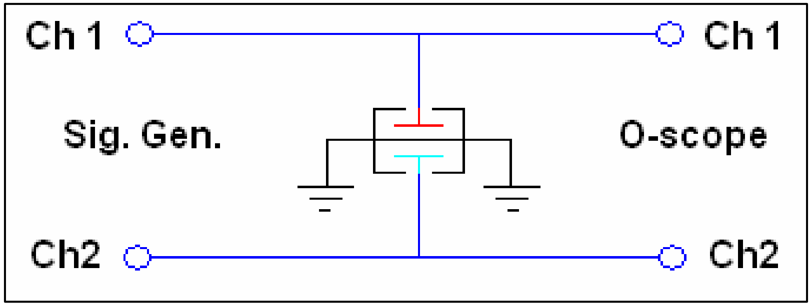


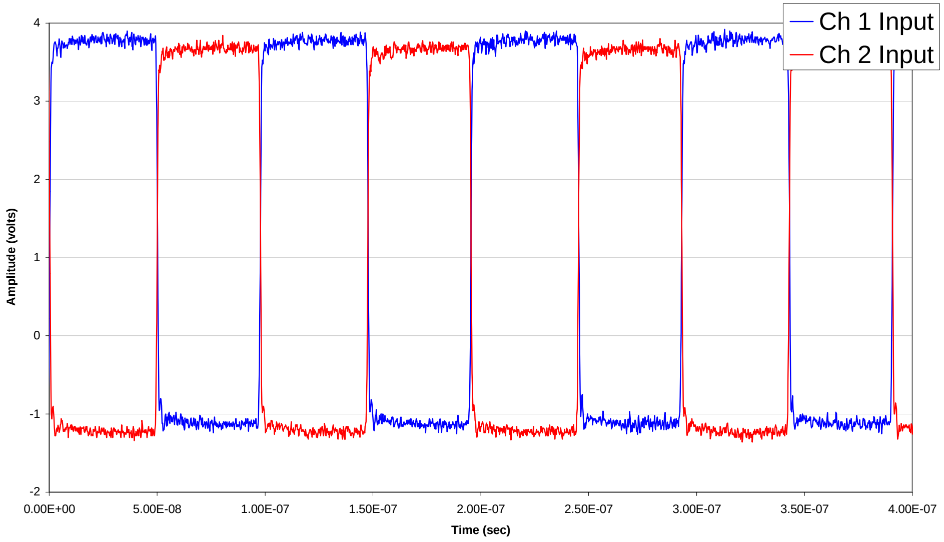


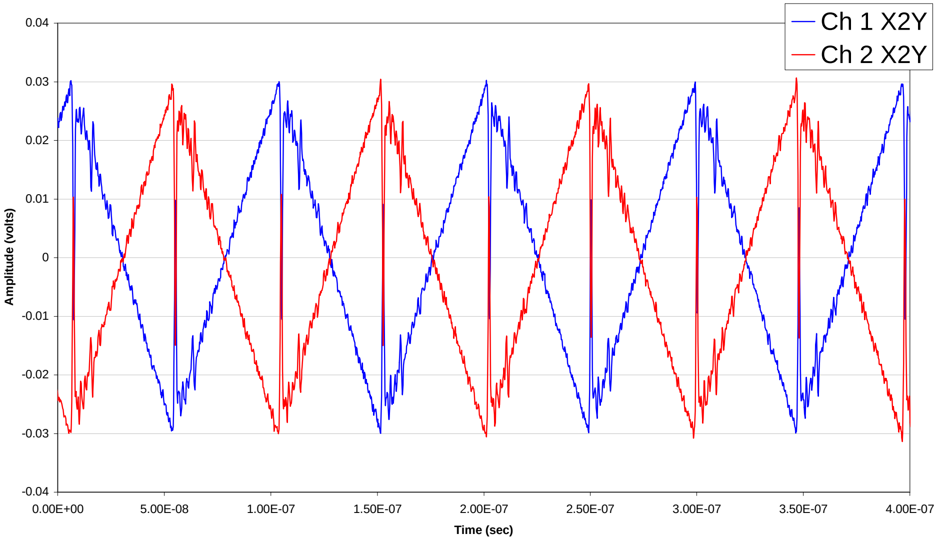
X2Y 0603 100nF



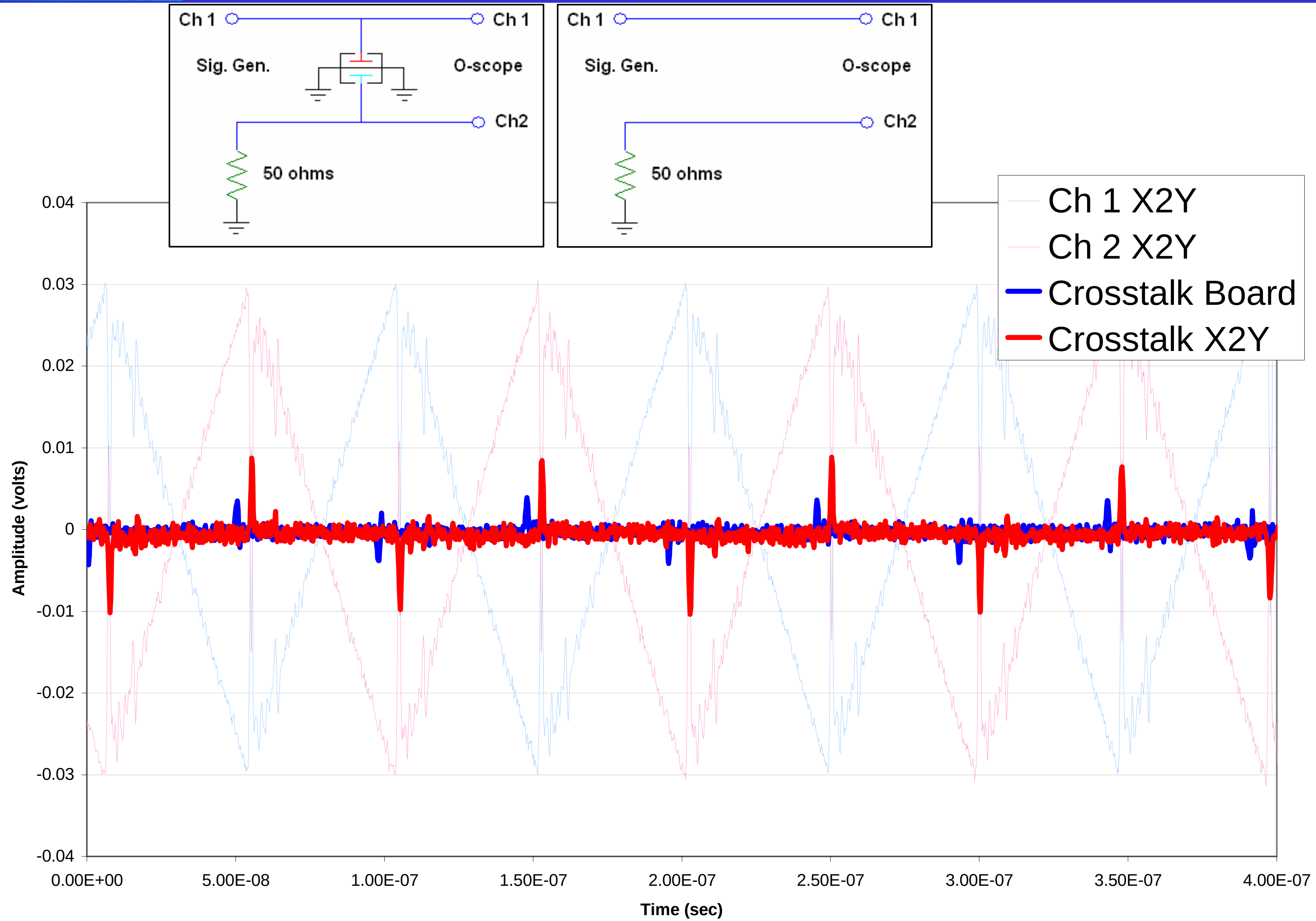
X2Y® Circuit 1 --- Multi-Plane Decoupling







X2Y® Circuit 1 - Multi-Plane Decoupling (crosstalk)



Conclusion

- IPDs are the foremost capacitor technology that can supply the instantaneous current needs and HF transient filtering for ICs.
- NEMI Roadmap shows IPDs offer cost advantages to OEMs by 2005.
- BOM considerations for IPDs
  - Fewer vias
  - Fewer solder joints
  - Saves PCB space
    - Allows for smaller, more dense designs
    - More room for signal routing
    - Functionality – plane integrity
- IPDs are the future for decoupling

Questions?

Please Contact:

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Resources

- Sanders, Muccioli, North, and Slattery, " The Quantitative Measurement of the Effectiveness of Decoupling Capacitors in Controlling Switching Transients from Microprocessors," CARTS 2005 USA, Palm Springs, CA, March 2005.
- Steve Weir, Scott McMorrow, Teraspeed® Consulting Group LLC, "High Performance FPGA Bypass Filter Networks," DesignCon 2005, Santa Clara, CA, February 2005.
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- Steve Wier, " Considerations for Capacitor Selection in FPGA Designs," CARTS 2005 USA, Palm Springs, CA, March 2005.
- Joseph Dougherty, John Galvagni, Larry Marcanti, Rob Sheffield, Peter Sandborn, and Richard Ulrich, "The NEMI Roadmap: Integrated Passives Technology and Economics," CARTS 2003, Scottsdale, AZ, April 2003.
- Steve Weir, Teraspeed® Consulting Group LLC, "Does position matter? Locating bypass capacitors for effective power distribution and EMC control", Santa Clara Valley Chapter of the IEEE-EMC Society, January 2005.