Using a Spatial View to Understand and Solve Common Power Bypass Problems

Why Is Space So Important?

- Power delivery is a process of propagating E/M fields with a minimum disturbance in E.
- Field propagation is fundamentally limited by spatial effects: inductance and wave modes.

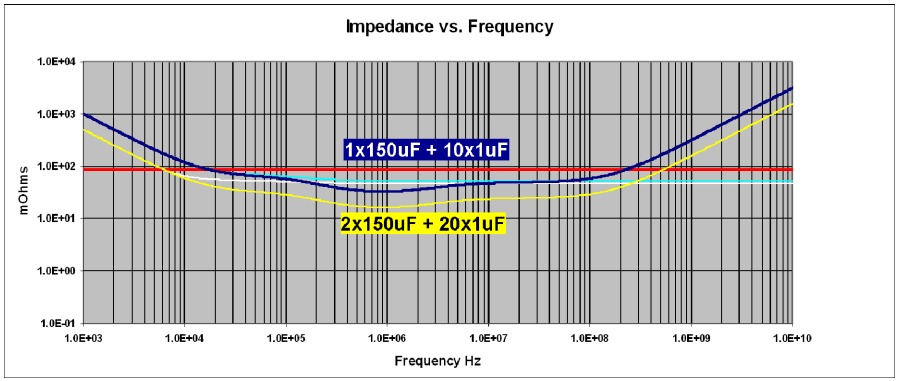
1D Networks Good to ???

- 1 dimensional SPICE networks are often used to design power delivery networks.
- Accuracy falls off rapidly with frequency
- Cut-off varies w/ cavity thickness.
  - Figure of merit: 80MHz * H in mils
  - A typical 4 mil cavity becomes inductive at 80MHz / 4 = 20MHz
  - A thin 0.4 mil cavity becomes inductive near 200MHz

Example

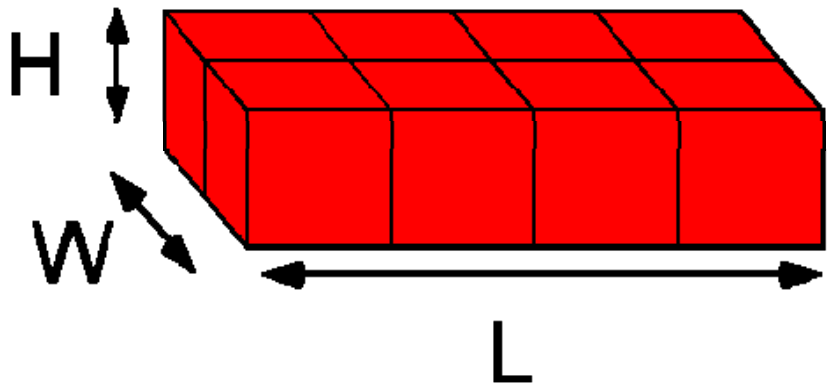
- Using high ESR, constant L caps target impedance scales by capacitor count up to F_{CUTOFF}
  - F_{CUTOFF} = 0.707 * ESR / (2pi * ESL)
  - For 500mOhm / 500pH capacitors = 112MHz
- # of caps for 50mOhms: 500mOhms / 50mOhms = 10
- # of caps for 25mOhms: 500mOhms / 25mOhms = 20

Example 1D Network Responses
150uF 70mOhm 3nH Tantalum
1uF 500mOhm 500pH MLCCs



ID Falls Apart Due to Interconnects

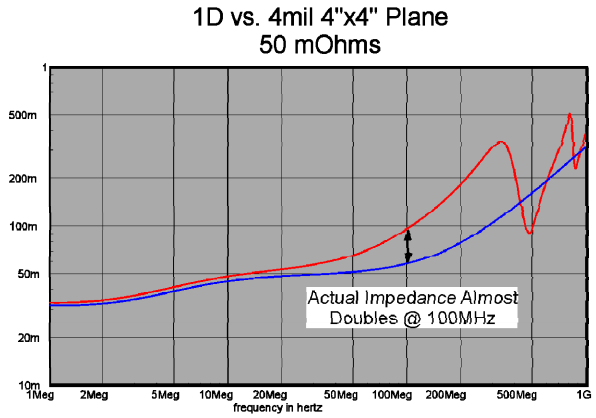
- Interconnects are fundamentally inductive at any appreciable frequency
- Inductance of a rectangular section:

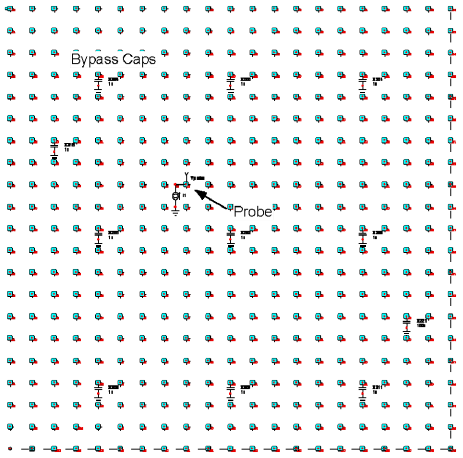


Inductance = 31.9nH * H(inches) * L/W

Our 50mOhm Network on a Plane

- Even at a pedestrian 50mOhms, a 4mil plane cavity limits performance below 100MHz.
- We can improve w/ thinner planes
  - Expensive
  - BellCore requires 4mils, w/ waiver for BC2000 (2 mils)





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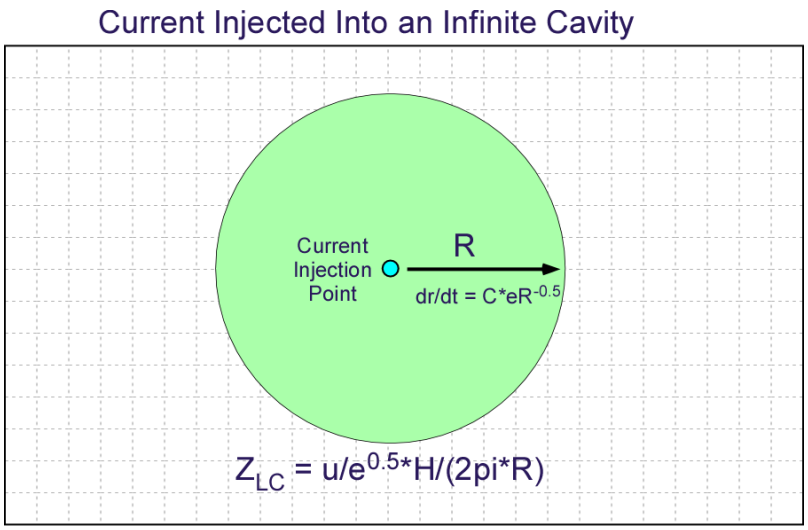
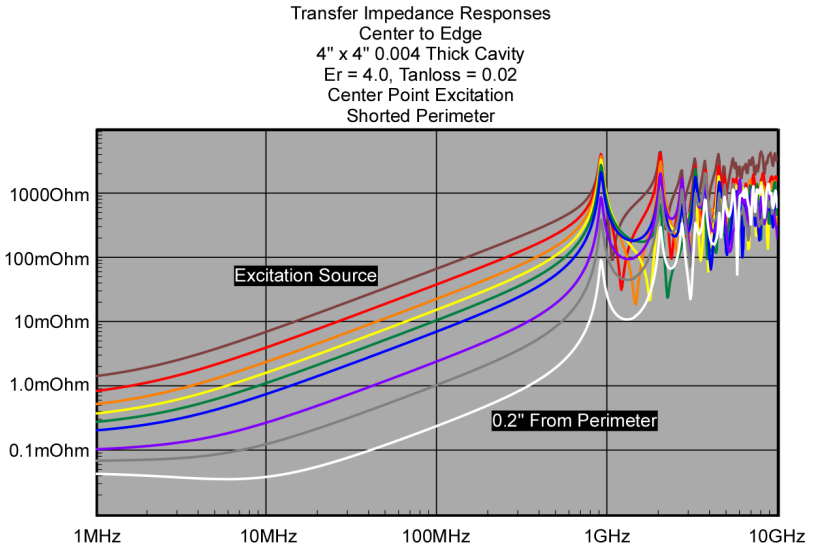
Power Cavity LC Behavior

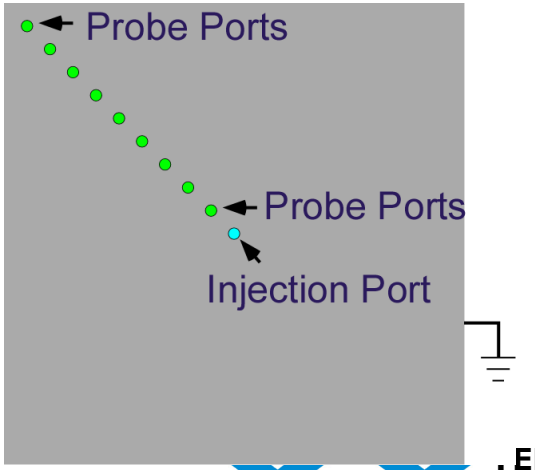
- The parallel plates of a plane cavity form a plate capacitor
- But to current impulses that are electrically short compared to he plane extents the current / voltage transfer function is ***inductive***



Shorted Boundary Response

- The lowest impedance the circuit elements of a PDN can present is a virtual short.
- Limiting response of a power cavity section may be determined by modeling with the edges shorted.
- Wave effects introduce impedance peaks and valleys to the frequency response





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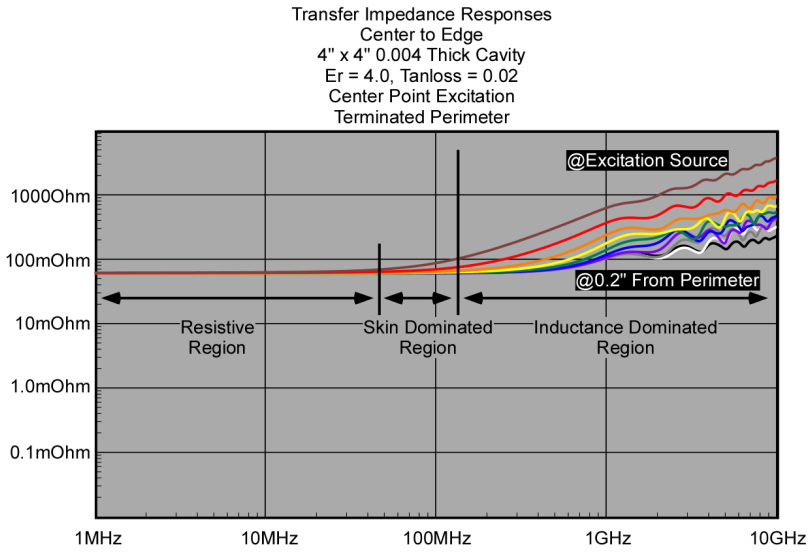
Terminated Boundary Response

- A perfect boundary termination eliminates reflections.
- Plane response is inductive to all electrically short events.



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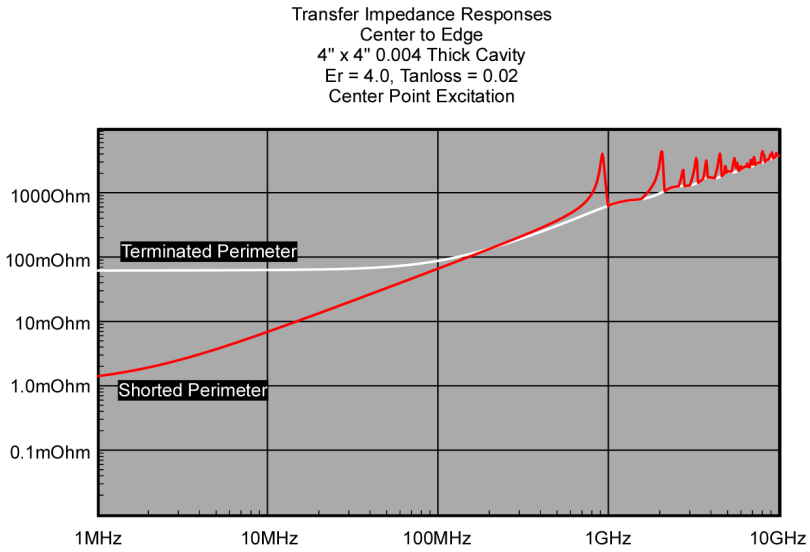
Composite Response for Convolution

- Worst-case impedance is what we want to evaluate
- Ignore impedance valleys from standing waves as they rely on signal history
- Include impedance peaks as depending on signal history they can be encountered



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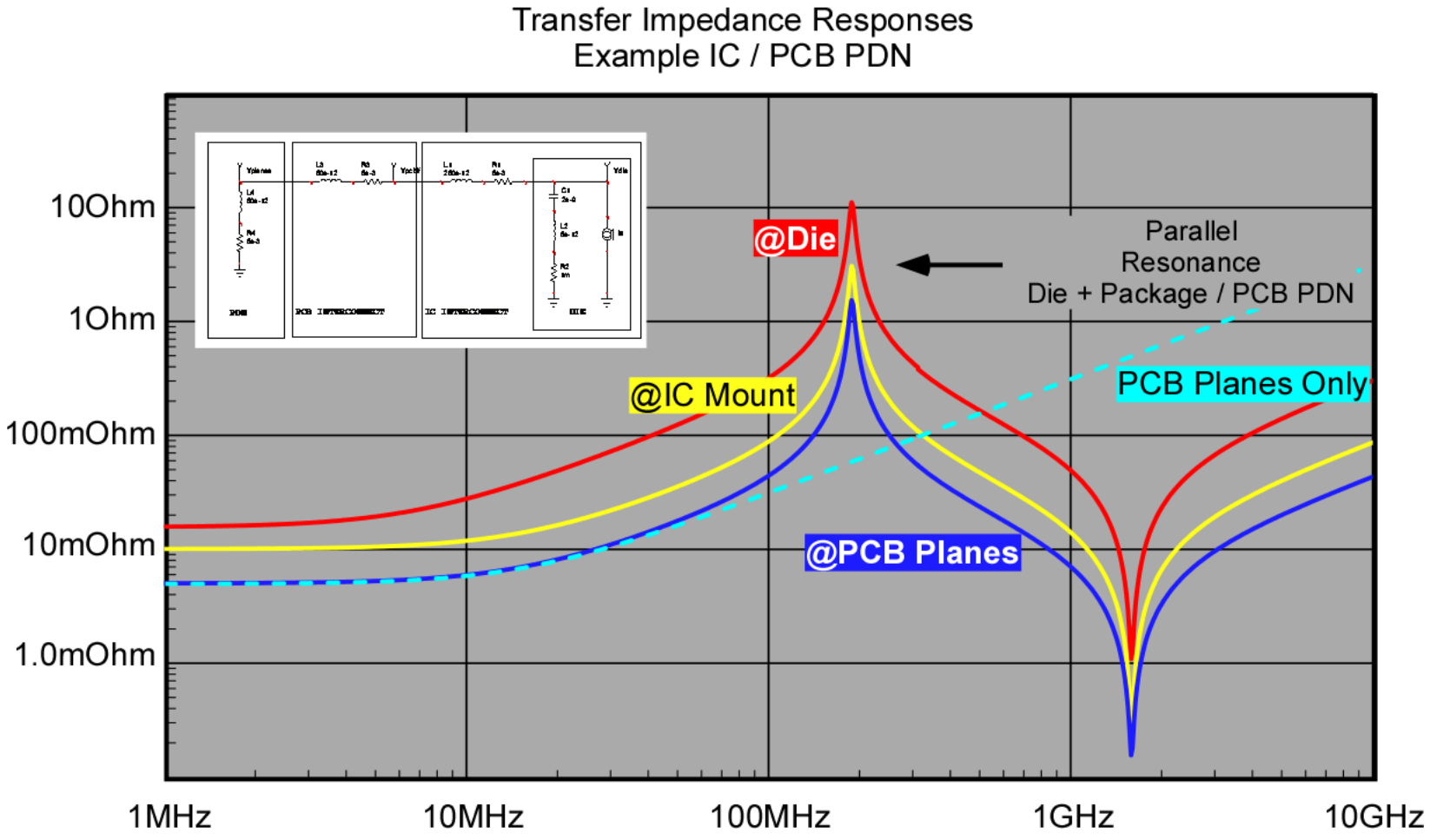
IC Die / Package ⇔ PCB PDN Resonance

- IC die and/or on substrate capacitance reacts w/ PCB PDN response
  - Interconnect drives inductive behavior
- Total effective resistance of the PCB PDN, and the IC PDN combined w/ net inductance drive circuit Q

IC / PCB PDN Resonance



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Calculating Resonance

- First order approximation usually good to about 10% in frequency:
  - $F_{RES} = 0.16*(p*H/(ESL_{CAP}*E*eR))^{0.5}$

Where:

p is the number of capacitors / square inch

H is the plane cavity height in mils

ESL is the mounted inductance of a single capacitor

E is 225E-15pF/Inch

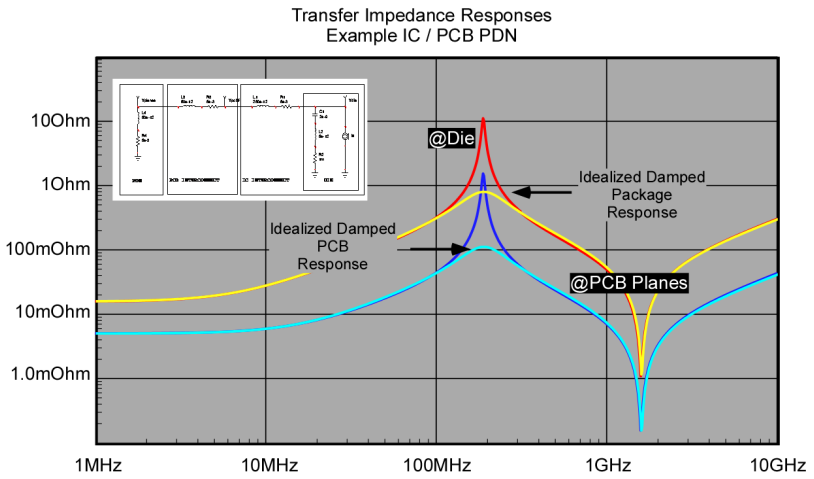
eR is the material relative permitivity

What the Formula Tells Us

- Thinner dielectrics require a greater capacitor density to maintain a given F_{RES}
- Higher eRs also require a higher capacitor density for a given F_{RES}
- Trying to drive F_{RES} beyond the signal band with sheer capacitor density is ***very expensive***, # of caps increases as square of F_{RES}

Controlling Resonance

- Resonance control requires damping
- Damping can be provided as a series ESR in the PCB PDN or by a series and/or shunt ESR in the IC package



Z Axis Dominance

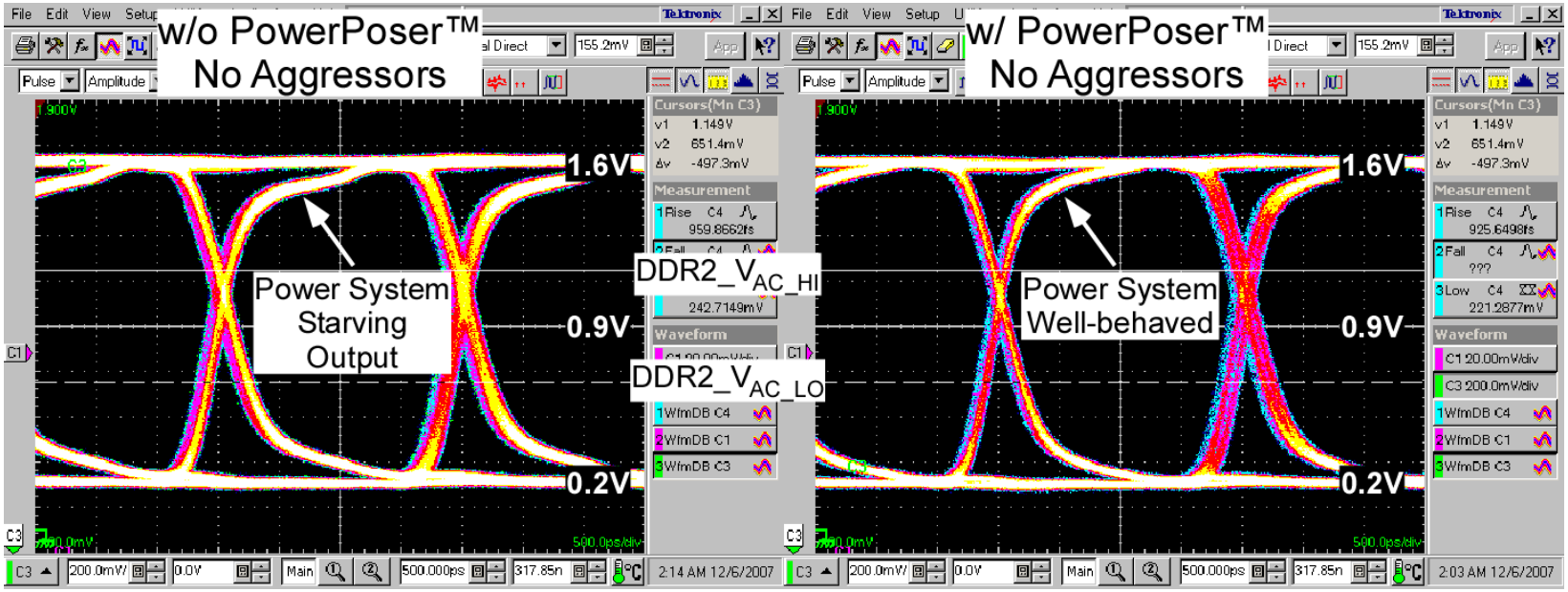
- Z Axis Inductance often much worse than X/Y
- Virtex®5 VCCIO about 9.7pH / mil supporting 40 I/Os
- Stratix® 3 VCCIO about 2.3pH / mil supporting 92 I/Os

Examples

- Samtec PowerPoser™
  - Thin dielectrics and low inductance caps
  - Dramatic improvements in SERDES, and single ended signaling

Comparative Performance Idle

Virtex®4 500Mbps SSTL1.8 No DCI



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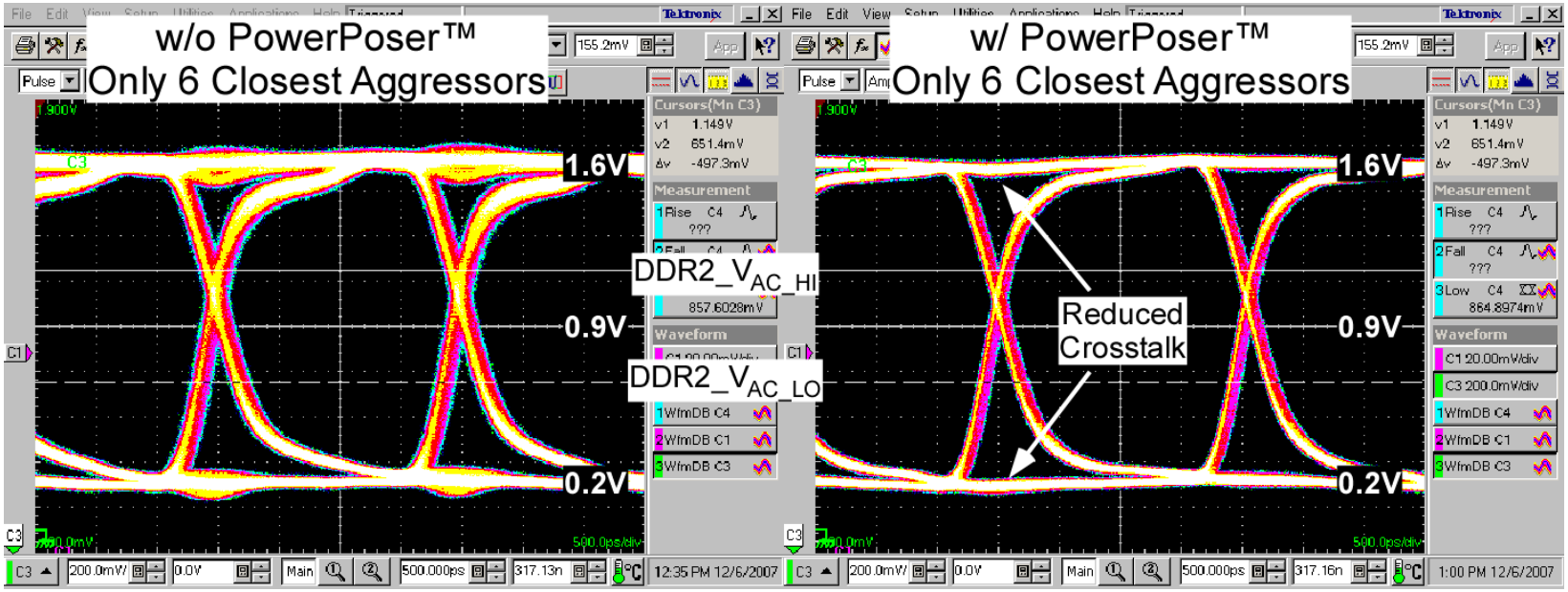
Comparative Performance Local Aggressors Only



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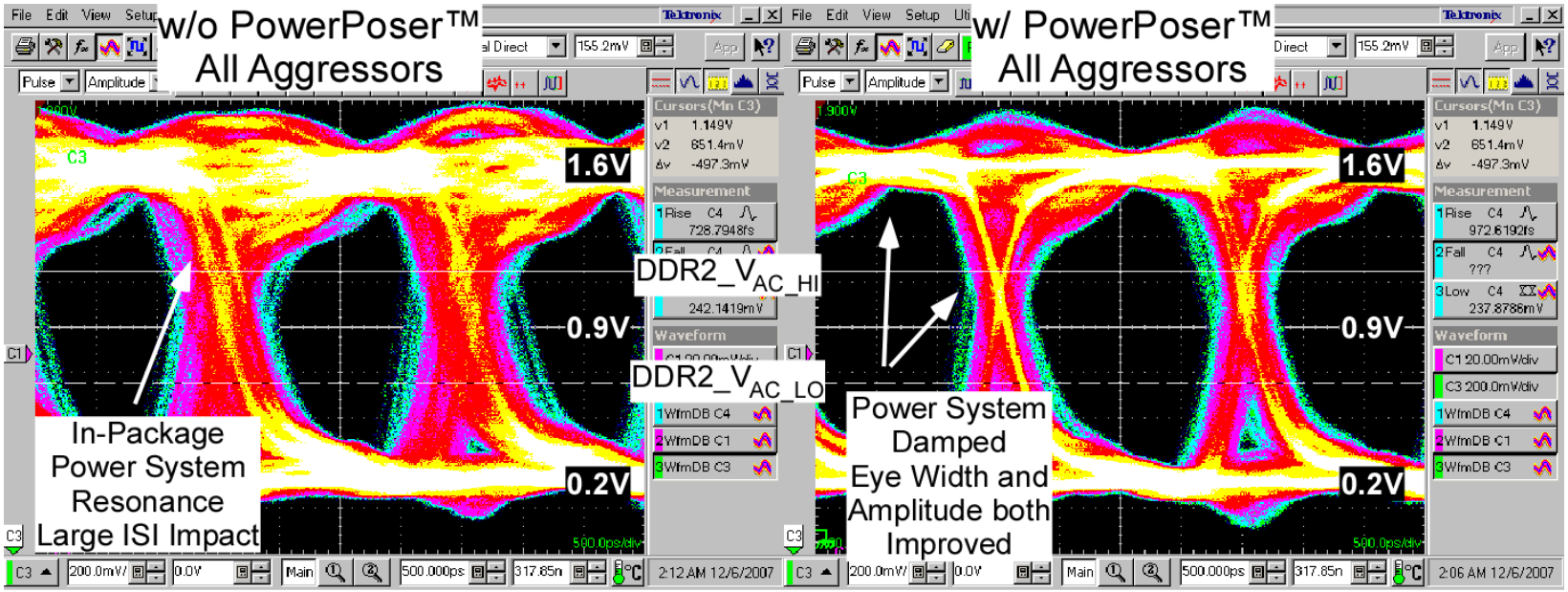
Comparative Performance All Aggressors



I/Os Configured for SSTL1.8 w/o DCI
500Mbps

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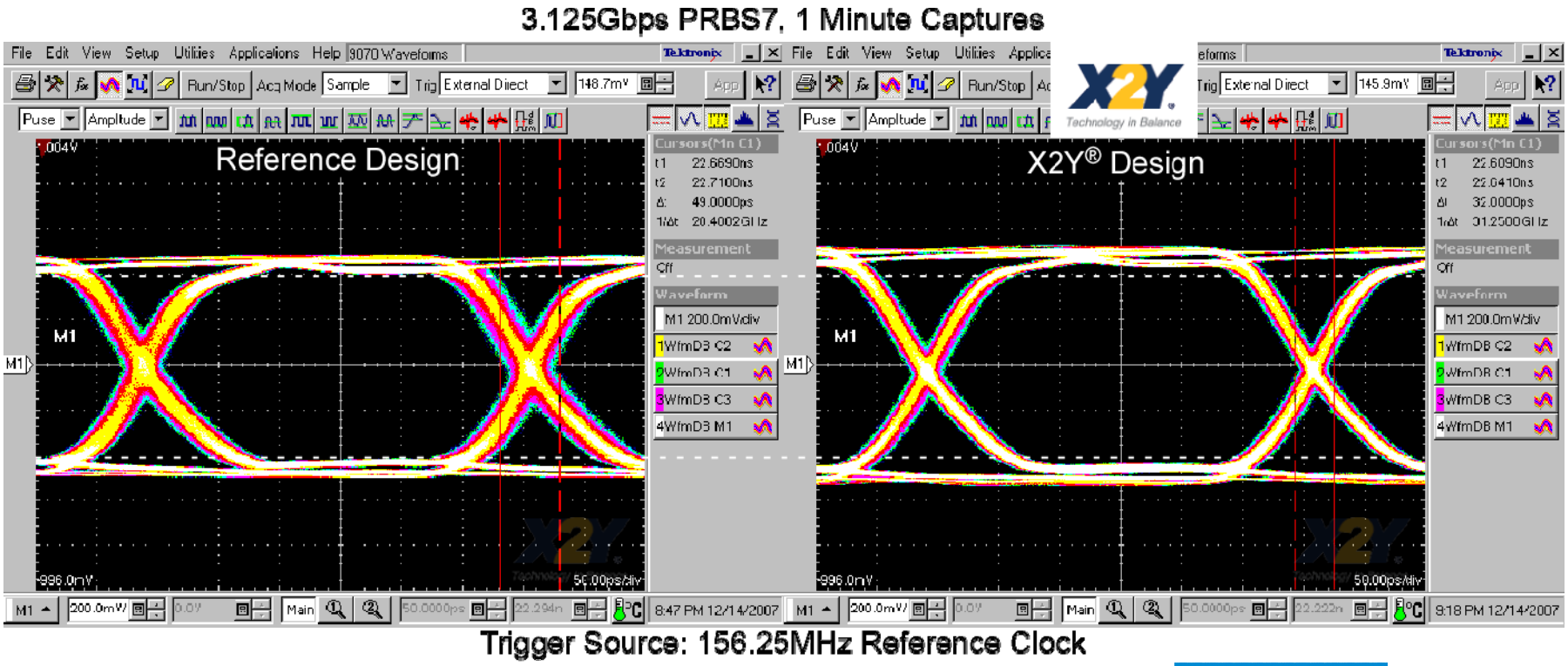
X2Y® Improvements to Altera SerDes

- Replaced bypass network on existing reference design.
- Applied spatial methods to raise F_{RES} and damp
- Substantially improved Dj while reducing total capacitor count by 70%

3.125Gbps Performance PRBS7

- Measurements Taken w/ Tektronix CSA8200
- 80E03 20GHz sampling heads



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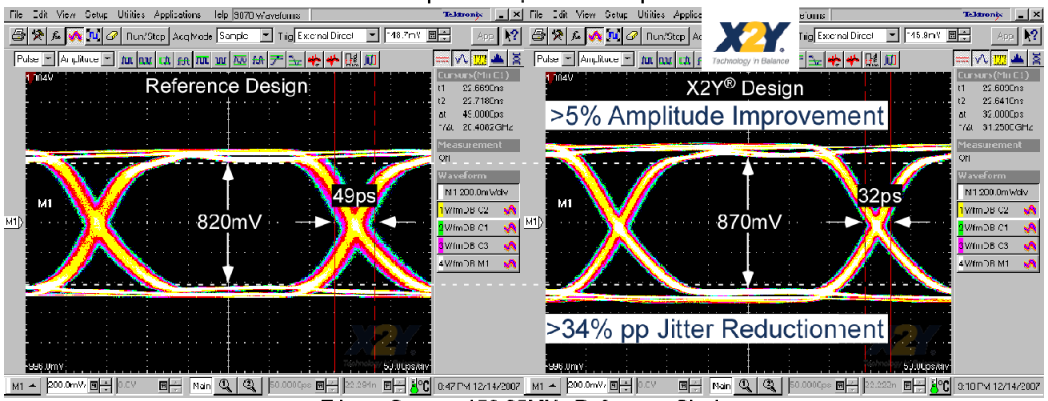
3.125Gbps Performance PRBS7/PRBS23

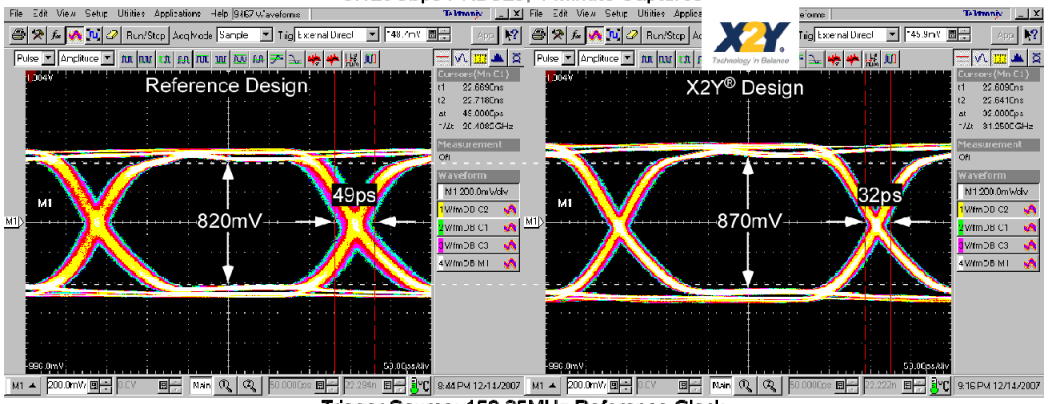
- X2Y® Reduces jitter to 32ps p-p PRBS7 & PRBS23
  - vs 49ps in reference design

3.125Gbps PRBS7, 1 Minute Captures



Trigger Source: 156.25MHz Reference Clock

3.125Gbps PRBS23, 1 Minute Captures



Trigger Source: 156.25MHz Reference Clock

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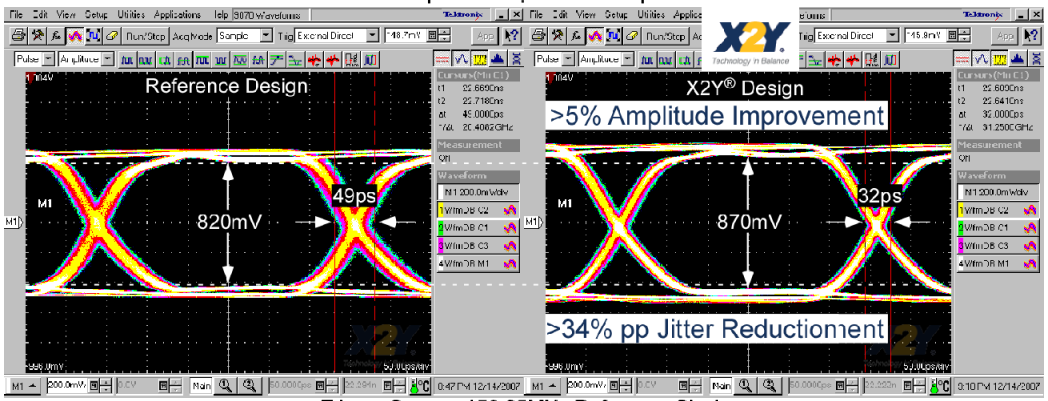
3.125Gbps Performance PRBS7/PRBS23

- X2Y® improves eye amplitude >5%
  - 870mV pp @ sample point vs 820mV pp reference

3.125Gbps PRBS7, 1 Minute Captures



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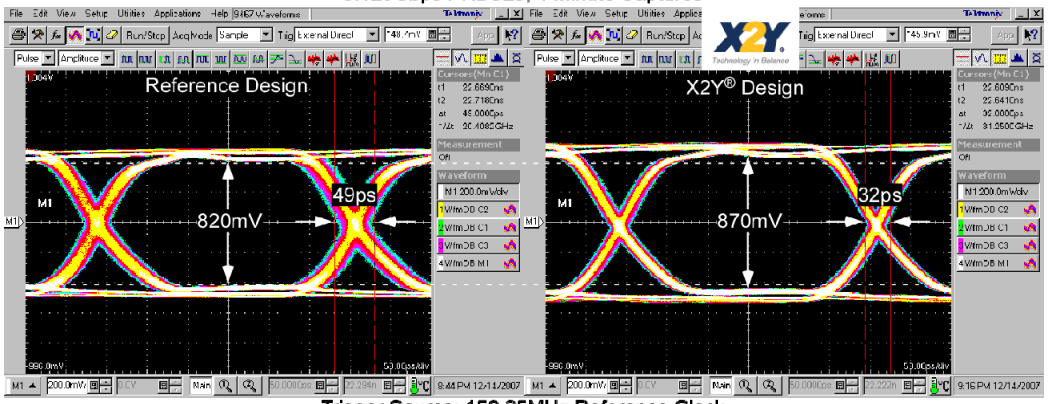
3.125Gbps PRBS23, 1 Minute Captures



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Conclusions

- PDN performance is limited by the performance of interconnects, which are spatial.
- To high frequency signals planes always appear ***inductive***
- Paradoxically, the distributed capacitance of planes resonates with mounted bypass networks

Conclusions

- Ultimately, inductance and resonances (driven by inductance) are the evils we need to manage in a PDN
- Thin and high eR dielectrics reduce PDN impedance, but require greater bypass capacitor density for a given F_{RES}
- Careful PDN implementations that take spatial effects into account can result in dramatic performance improvements and decreased component counts.

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