X2Y® Capacitors in IC Back-Side Mounting Applications

Summary

Bypass capacitors are often located on the far side of a printed circuit board from the IC mounting surface. This application note details how to obtain the best performance possible when using X2Y® capacitors on the PCB back-side. This note identifies how properly applied, X2Y® capacitors result in lower power system impedance than possible with conventional capacitors while drastically reducing component count.

Introduction

Bypass capacitors support power system impedance both to the IC and the PCB as a whole. When capacitors are located on the back-side of the PCB Z axis via array inductance through the PCB becomes a crucial factor in performance seen at the IC. Optimizing via utilization results in optimal power system performance.

Determining PCB Via Inductance

When using capacitors attached to the PCB back-side, a significant interconnect inductance separates these capacitors from the IC die. The inductance is a combination of:

- IC in package plane configuration, and die break-out
- IC Z axis power interconnect, including BGA balls
- PCB vias from the IC mounting surface to the capacitor mounting surface (PCB back-side)

To find PCB via array inductance we can: use a 3D full wave solver for the most accurate results, a 3D quasi-static solver for fairly accurate results, or we can estimate to reasonable accuracy using closed form solutions. In each case we treat the top and bottom planes in the PCB as shorts. Procedural descriptions using 3D solvers are beyond the scope of this document. A free 3D static solver is FastHenry[1] developed by MIT and front-end GUI is available at www.fastfieldsolvers.com. FastHenry is the engine used by Cadence Design Systems® Allegro® Power Integrity tool.

High frequency currents track the ***outside skin*** of PCB vias. So, it is important to know the outside diameter of the via hole, i.e., the drill size, not the finished hole size. Given:

- Via **drill** diameter (do not confuse this with finished hole diameter), D in mils
- PCB height, H in mils

- Vdd / Vss via pair separation, S mils

We can obtain the Z axis inductance for a single, isolated via pair:

$$L_{VIA\_PAIR} = 10.2pH * H * \ln(2S / D)$$

Given certain assumptions, we can extend this formula to arrays of vias:

1. The current distribution within the via array is close to uniform.
2. The spacing of Vdd to Vdd, and Vss to Vss vias is no closer than the spacing of Vdd to Vss vias.

Under these conditions, the total inductance is:

$$L_{VIA\_ARRAY} = K_{COUPLE\_ADJUST} / (SUM_{N=1toM} (1 / (L_{VIA\_PAIR\_N})))$$

K_{COUPLE_ADJUST} is a correction factor for Vdd to Vdd, and Vss to Vss via coupling in the array. It generally tends between 1.05 and 1.20, 1.15 being a relatively common value with 1 – 1.27 mm pitch.

For via arrays where the Vdd to Vss spacing is fixed this reduces to:

$$L_{VIA\_ARRAY} = K_{COUPLE\_ADJUST} * 10.2pH * (H / N) * \ln(2S / D)$$

Via Inductance Analysis for 1mm BGAs

The following analysis illustrates the various trade-offs when designing a low inductance bypass network on the PCB back-side for 1mm BGAs.

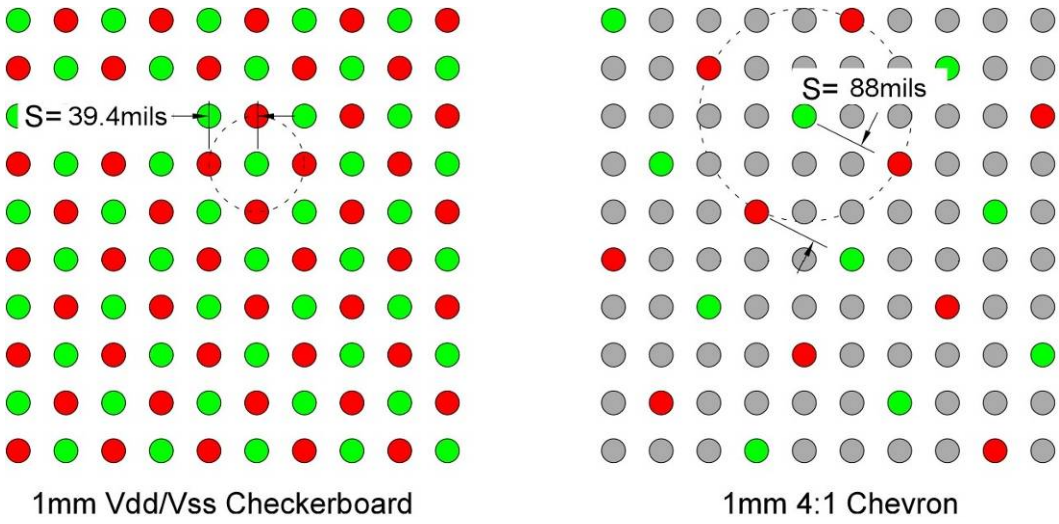

Figure 1. Example Via Arrays

Via Spacing and Via Diameter

The logarithmic impact of spacing to via diameter ratio restricts diameter influence on inductance, particularly for Vdd / Vss pairs that are widely spaced. For example, in packages that use 1mm pairs in a Vdd/Vss checkerboard pattern, going from a 10mil to 14mil drill reduces inductance by only 16%. For Vdd / Vss pairs on a sparse 4:1 chevron such as used by Xilinx Virtex 4 I/O supplies, the difference drops to under 12%.

S mils	D mils	$L_{0\%}$	$L_{5\%}$	$L_{10\%}$	$L_{15\%}$	$L_{20\%}$
39.4	**10**	21.0 pH/mil	22.0 pH/mil	23.1 pH/mil	24.1 pH/mil	25.2 ph/mil
39.4	**12**	19.1 pH/mil	20.1 pH/mil	21.1 pH/mil	22.0 pH/mil	22.9 pH/mil
39.4	**14**	17.6 pH/mil	18.4 pH/mil	19.3 pH/mil	20.2 pH/mil	21.1 pH/mil
50	**10**	23.4 pH/mil	24.6 pH/mil	25.8 pH/mil	26.9 pH/mil	28.1 pH/mil
50	**12**	21.5 pH/mil	22.6 pH/mil	23.7 pH/mil	24.8 pH/mil	25.9 pH/mil
50	**14**	20.0 pH/mil	21.0 pH/mil	22.0 pH/mil	23.0 pH/mil	24.0 pH/mil
88	**10**	29.1 pH/mil	30.6 pH/mil	32.1 pH/mil	33.5 pH/mil	35.0 pH/mil
88	**12**	27.3 pH/mil	28.6 pH/mil	30.0 pH/mil	31.4 pH/mil	32.7 pH/mil
88	**14**	25.7 pH/mil	27.7 pH/mil	28.3 pH/mil	29.6 pH/mil	30.9 pH/mil

Table 1. Typical Via Pair Inductances

Table 1 illustrates some typical via pair inductances based on via diameters and spacing. 39.4mils corresponds to adjacent Vdd / Vss vias in 1mm packages. 88mils reflects separation in an alternating 4:1 chevron as occurs in the I/O fields of Xilinx® Virtex 4® FPGAs.

Larger diameter vias yield lower inductances, and they are easier to drill. The trade-off is that they demand larger capture and antipads on unconnected layers. Those larger clearances conflict with BGA escape routing. As a result, thinner boards usually employ smaller drills. Typically, 10 mil drills are used with boards up to 62mils thick for low cost process, and up to 100mils for high performance product. Table 2 summarizes inductances for common via configurations in low-cost constructions.

S (mils)	D (mils)	PCB thickness (mils)	$L_{0\%}$	$L_{10\%}$	$L_{20\%}$
39.4	**10**	62	1300pH	1430pH	1560pH
39.4	**12**	93	1780pH	1960pH	2130pH
39.4	**14**	120	2110pH	2320pH	2530pH
50	**10**	62	1450pH	1600pH	1740pH
50	**12**	93	2000pH	2200pH	2400pH
50	**14**	120	2400pH	2640pH	2880pH
88	**10**	62	1810pH	1990pH	2170pH
88	**12**	93	2540pH	2790pH	3050pH
88	**14**	120	3090pH	3390pH	3700pH

Table 2. Typical Via Pair Inductances, Shorted Plate PCB Top / Bottom

As can be seen from Table 2, via pair inductance is much greater than the inductance values reported for common MLCC capacitors. Consequently, attaching capacitors to each possible via pair approximates shorting the vias to the bottom PCB surface.

Inductance Comparaisons, Via Pair vs. MLCC

To get an accurate picture, we can compare via inductances to the contribution of capacitors. X2Y® uses a very accurate test fixture to obtain inductance measurements for both X2Y® and conventional capacitors connected to power cavities at various subsurface depths.[2,3]

Upper Dielectric Height	Capacitor	C	ESR	ESL			
				LF < 100MHz		HF > 100MHz	
				Value	%	Value	%
3 mils	X2Y® 0603	176nF	10.5mΩ	146pH	1.00	118pH	100
	0402 2 Via	188nF	23.0mΩ	658pH	4.51	452pH	3.83
12 mils	X2Y® 0603	166nF	10.9mΩ	188pH	1.00	154pH	1.00
	0402 2 Via	201nF	19.6mΩ	807pH	4.29	626pH	4.07

Table 3. Summary of de-embedded mounted capacitor inductances for 3 and12 mil upper dielectric cavities, from Understanding Capacitor Inductance and Measurement in Power Bypass Applications", 2006 X2Y®.

Table 4 combines results from Tables 2 and 3 to highlight the disparity between via and capacitor inductances:

S mils	D mils	PCB thickness (mils)	$L_{10\%}$ Single Via Pair	0402 Single Via Pair Attach 3mil UD		$L_{10\%}$ Three Via Pair	X2Y Three Via Pair 3mil UD	
				LF	HF		LF	HF
39.4	**10**	62	1430pH			477pH		
39.4	**12**	93	1960pH			653pH		
39.4	**14**	120	2320pH			773pH		
50	**10**	62	1600pH			533pH		
50	**12**	93	2200pH	658pH	452pH	733pH	146pH	118pH
50	**14**	120	2640pH			680pH		
88	**10**	62	1990pH			663pH		
88	**12**	93	2790pH			930pH		
88	**14**	120	3390pH			1130pH		

Table 4. Comparative Via and Bypass Capacitor Inductances

Table 4 illustrates that when capacitors connect to vias 1:1, via inductance strongly dominates and capacitors are greatly underutilized.

Bypass Network Inductance

Using the inductance analysis of the individual elements as a basis, we now combine same elements to form a bypass capacitor network that judiciously uses capacitors to yield the lowest system inductance.

For example if we attach a BGA with 50 via pairs to a 93mil thick PCB, the total inductance associated with the via array is:

1960pH / 50 = 39.2pH, (use in Table 5)

If we could share those vias uniformly across a capacitor array, then with various numbers of 0402 capacitors in the array, we see rapidly diminishing returns once the capacitor array inductance matches the via array inductance.

Qty 0402 Capacitors	Capacitor Array L Cap L / Cap Qty	Total L Cap Array L + Via Array L	Percent Total L vs. Matched
9	73.1 pH	112.3 pH	144%
17	**38.7 pH**	**77.9 pH**	**100%**
25	26.3 pH	65.5 pH	84%
34	19.4 pH	58.6 pH	75%
42	15.7 pH	54.9 pH	70%
50	13.2 pH	52.4 pH	67%

Table 5. Inductance for 93mil PCB, w/50 1mm Via Pairs and 0402 Caps

MLCC Selection

As can be seen from Table 5, going from 9 to 17 capacitors drops the inductance by more than a third. However, the next eight capacitors reduce the total inductance of the bypass network by less than one sixth.

If we select a given via pitch and geometry, we can readily establish estimated number of capacitors of a given type needed to match the via array inductance:

$$N_{CAP} = N_{VIA\_PAIRS} * L_{CAP} / (H_{PCB} * K_{LVIA\_PAIR})$$

Where:

N_{CAP} is the number of capacitors required.

N_{VIA_PAIRS} is the number of V_{DD} / V_{SS} via pairs

L_{CAP} is the mounted inductance of a single capacitor

H_{PCB} is the PCB thickness

K_{LVIA_PAIR} is the inductance per unit PCB height in the same dimensions as H_{PCB}.

Clearly, the lower the mounted inductance per capacitor, L_{CAP}, the fewer capacitors needed to optimize a given bypass network.

Back-side Puddle Method

The back-side "puddle" concept provides a means to pool vias through a PCB to gain maximum capacitor utilization. Figure 2 illustrates the "puddle" concept.

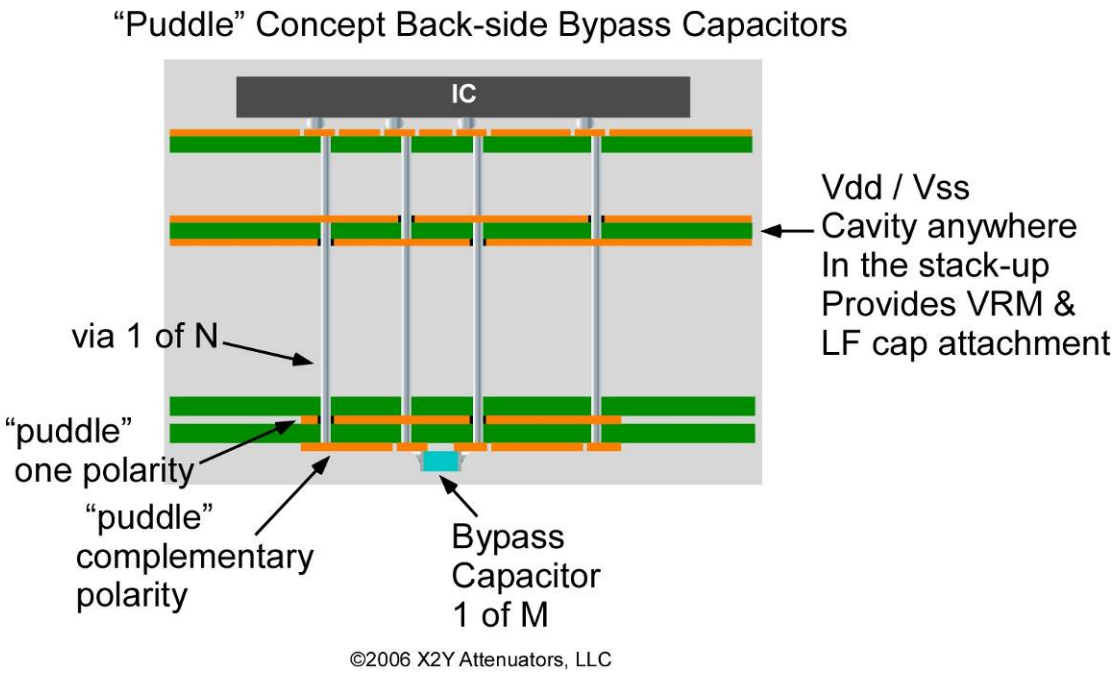

Figure 2. Back-side capacitors attached to Vdd/Vss "puddle"

The back-side "puddle" concept places a Vdd/Vss cavity underneath the BGA that is at least large enough to capture all of the Vdd/Vss via pairs for a particular power rail at or near the bottom of the PCB. The puddle can be made larger. Back-side capacitors attach to this small cavity that resembles a small pool, or puddle.

Often the "puddle" cavity is formed from the bottom surface, and the next layer up in the stack-up, layers N, and N-1 of an N layer PCB. Using modest cavity height in the puddle affords very good sharing of vias between attached bypass capacitors. The puddle method makes it possible to greatly reduce the number of bypass capacitors with little impact on total inductance. The puddle method also provides solutions to some potentially thorny manufacturing issues.

As illustrated in Figure 2, the PCB layers used for the back-side capacitor Vdd/Vss puddle can, but does not need to be the same layers as those used to attach the **V**oltage **R**egulator **M**odule (VRM), and any bulk capacitors.

Through-Hole PCB Constructions

The most common and low-cost PCB constructions are through hole drilled. In these constructions, via holes extend through the entire thickness of the PCB. Blind and buried constructions are more expensive and less common. The most common blind / buried construction for an N layer PCB consists of drilled through vias from layers 2 to N-1, and blind microvias from layer 1 to 2, and N to N-1.

Any back-side components compete with via patterns. 1mm BGAs create something of a challenge for back-side capacitors.

Puddle Method w/X2Y®

The super low inductance of X2Y® capacitors means that just a few X2Y® devices attached to a close-by puddle matches or bests the Z axis inductance of the via array.

Distance to Puddle (Distance from capacitor mounting surface to closer of two planes in puddle cavity)	**Typical Inductance**	
	< 100MHz	**> 100MHz**
Surface	126pH	98pH
1mil	130pH	102pH
2mils	134pH	106pH
3mils	138pH	110pH
4mils	142pH	114pH
5mils	146pH	118pH
6mils	150pH	122pH
7mils	154pH	126pH
8mils	158pH	130pH
9mils	162pH	134pH
10mils	166pH	138pH
11mils	170pH	142pH
12mils	174pH	146pH
13mils	178pH	150pH
14mils	182pH	154pH
15mils	186pH	158pH

Table 6. X2Y 0402/0603 Inductance Attached to Puddle

As can be seen in Table 2, a single X2Y® capacitor attached to a surface puddle yields inductance equivalent to more than nine 1mm via pairs through a 62mil thick PCB ≈1400pH / pair, and more than nineteen through a 0.120" PCB, ≈2400pH / pair.[4]

Example, 200 Via Pair Array

Figures 3-5 compares system inductance for conventional and X2Y capacitor arrays, w/10mil via drills on board thicknesses of 62 and 14mil via drills on 120mil thick boards using a bottom dielectric layer of 4mils:

1. Conventional Bypass Capacitor Network I (Figure 3);

    a. uses an array of 80-0402s capacitors in parallel to yield an inductance value of **6pH**.

    b. removes 160 of the 400 vias to accommodate conventional capacitor mounting. The inductance for the array of parallel vias on PCBs 62mils and 120mils thick is **12pH,** and **19pH** respectively.

c. exhibits a total inductance of the combined capacitor array and via array is **18pH,** and **25pH** for the 62mil and 120mil board thicknesses respectively

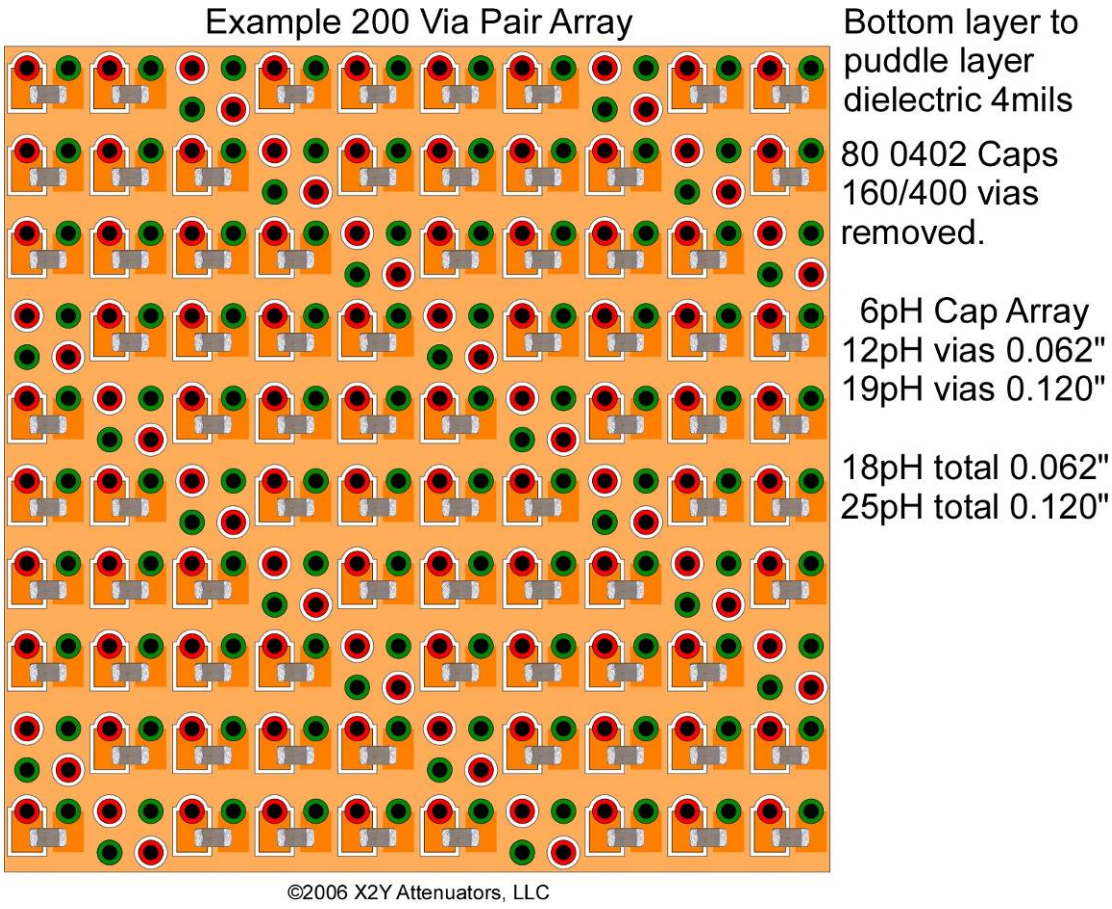

Figure 3. Conventional Bypass Capacitor Network I

2. X2Y® Bypass Capacitor Network (Figure 4);

   a. uses an array of 24 X2Y-0603s capacitors in parallel to yield an inductance value of **6pH**.

   b. removes 72 of the 400 vias to accommodate X2Y® capacitor mounting. The inductance for the array of parallel vias on PCBs 62mils and 120mils thick is **9pH, 14pH** respectively.

   c. exhibits a total inductance of **15pH,** and **20pH** for 62mil and 120mil board thicknesses respectively.

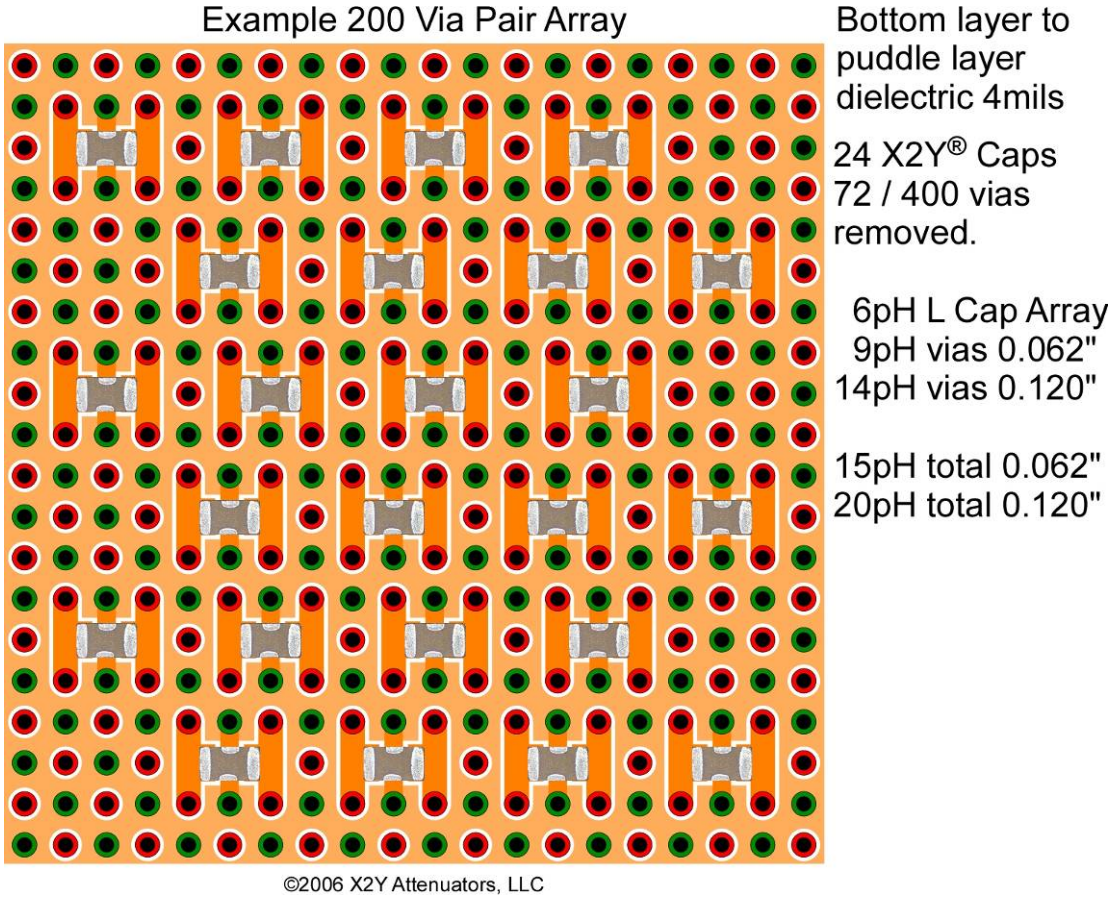

Figure 4. X2Y® Bypass Network

Table 5 shows the ineffectiveness of adding more capacitors once the capacitor array inductance falls below the inductance of the via array. To illustrate this point, Conventional Bypass Network II adds 20 more 0402 capacitors.

3. Conventional Bypass Network II (Figure 5)

    a. uses an array of 100-0402s capacitors in parallel to yield an inductance value of **5pH**.

    b. removes 200 of the 400 vias to accommodate conventional capacitor mounting. The inductance for the array of parallel vias on PCBs 62mils and 120mils thick is **14pH, 23pH** respectively.

    c. The total inductance of via and capacitor arrays in this system is **19pH, 28pH** for respective board thicknesses, ***worse*** than Conventional Array I, with 18pH and 25pH respectively using fewer capacitors. This is a direct result of the number of vias sacrificed in order to mount the additional capacitors.

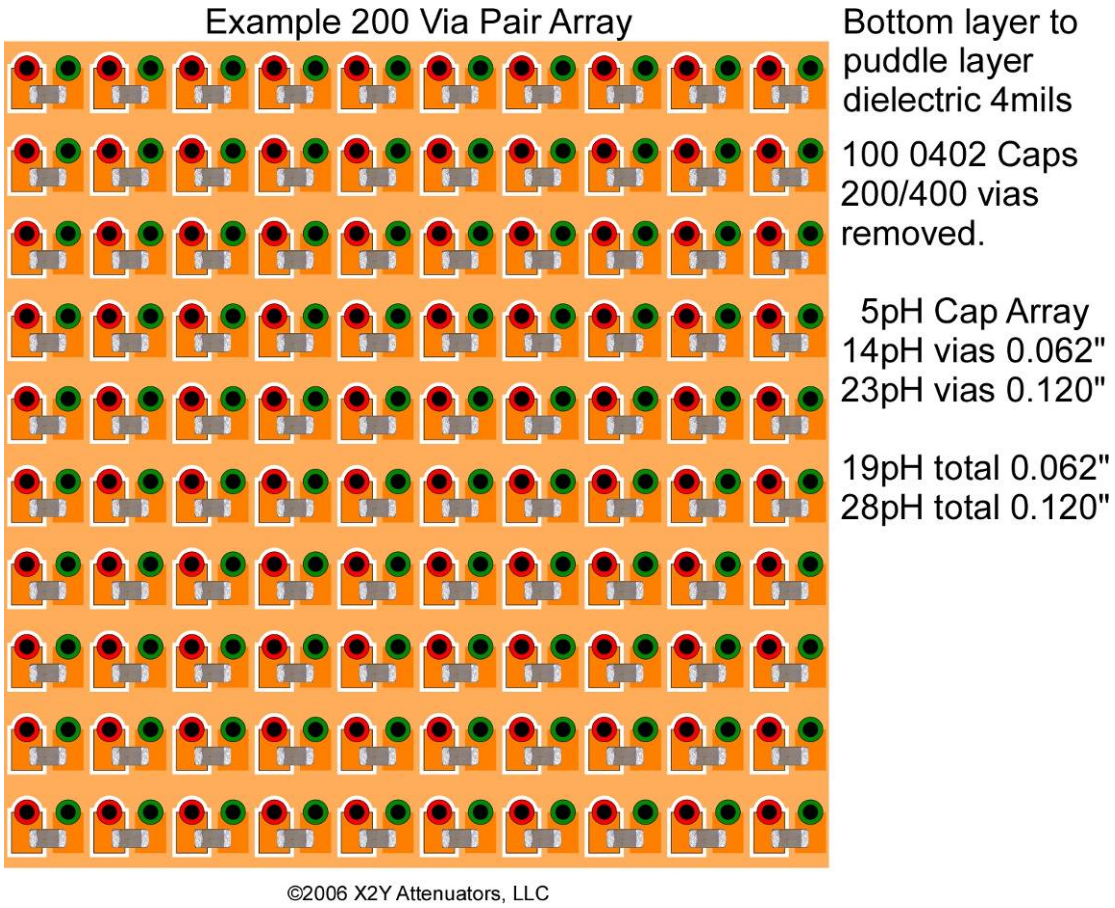

Figure 5. Conventional Bypass Network II

Since vias dominate the total inductance, in back-side mounting where array vias are traded off for bypass capacitors, optimized networks using the "puddle" concept remove a minimum of vias, and add just enough capacitors to balance match the via array inductance.

Conclusion

Back-side bypass capacitors can provide high performance when used with ICs that support sufficient Vdd/Vss pairs. Analysis of the individual elements that make up total via pair and MLCC inductances is required for proper design of bypass capacitor networks used for back-side applications. By utilizing the "puddle" concept, back-side capacitor utilization can be optimized. X2Y® capacitors excel in applications that utilize the back-side capacitors and the "puddle" concept. The methods published in this paper for designing a *back-side* bypass network can be used in combination with a previously published *Bypass Network Synthesis Procedure*[5] that provides like analysis for a bypass capacitor network that *surrounds* the IC to deliver best system performance on an IC by IC basis.

Author Acknowledgement

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Steve Weir has more than 20 years of experience in the Electronics Industry, holds 17 U.S. patents, and has architected a number of packet and TDM switching products. As a recognized expert on design strategies for Power Distribution Networks (PDN), Steve has participated as TecPanelist at multiple DesignCon Symposiums on the subjects of both bypass capacitor characterization and Power Integrity design methods for ICs.

Steve is a frequent contributor to the Si-List, a technically oriented reflector dedicated to the discussion and interchange of information on all topics related to signal integrity.

Contact Information

Direct inquiries and questions about this application note or X2Y® products to x2y@x2y.com or telephone:

X2Y® Attenuators, LLC
2730B West 21st Street
Erie, PA 16506-2972

Phone: 814.835.8180
Fax: 814.835.9047

To visit us on the web, go to http://www.x2y.com.

References

[1] FastHenry: A Multipole-Accelerated 3-D Inductance Extraction Program, M. Kamom, M.J. Tsuk, J. White

[2] "TF-MP2 Inductance of Bypass Capacitors, How to Define, How to Measure, How to Simulate", "Bypass Capacitor Inductance, Data Sheet Simplicity to Practical Reality" DesignCon East 2005, Steve Weir

[3] "Understanding Capacitor Inductance and Measurement in Power Bypass Applications", Steve Weir http://www.x2y.com/bypass.htm

[4] Attached capacitor inductance goes down with frequency; see "Get the Most from X2Y® Capacitors with Proper Attachment Techniques". Steve Weir http://www.x2y.com/bypass.htm

[5] High Performance FPGA Bypass Networks, Steve Weir, Scott McMorrow, Teraspeed Consulting Group, DesignCon 2005