X2Y®

Technology In Balance

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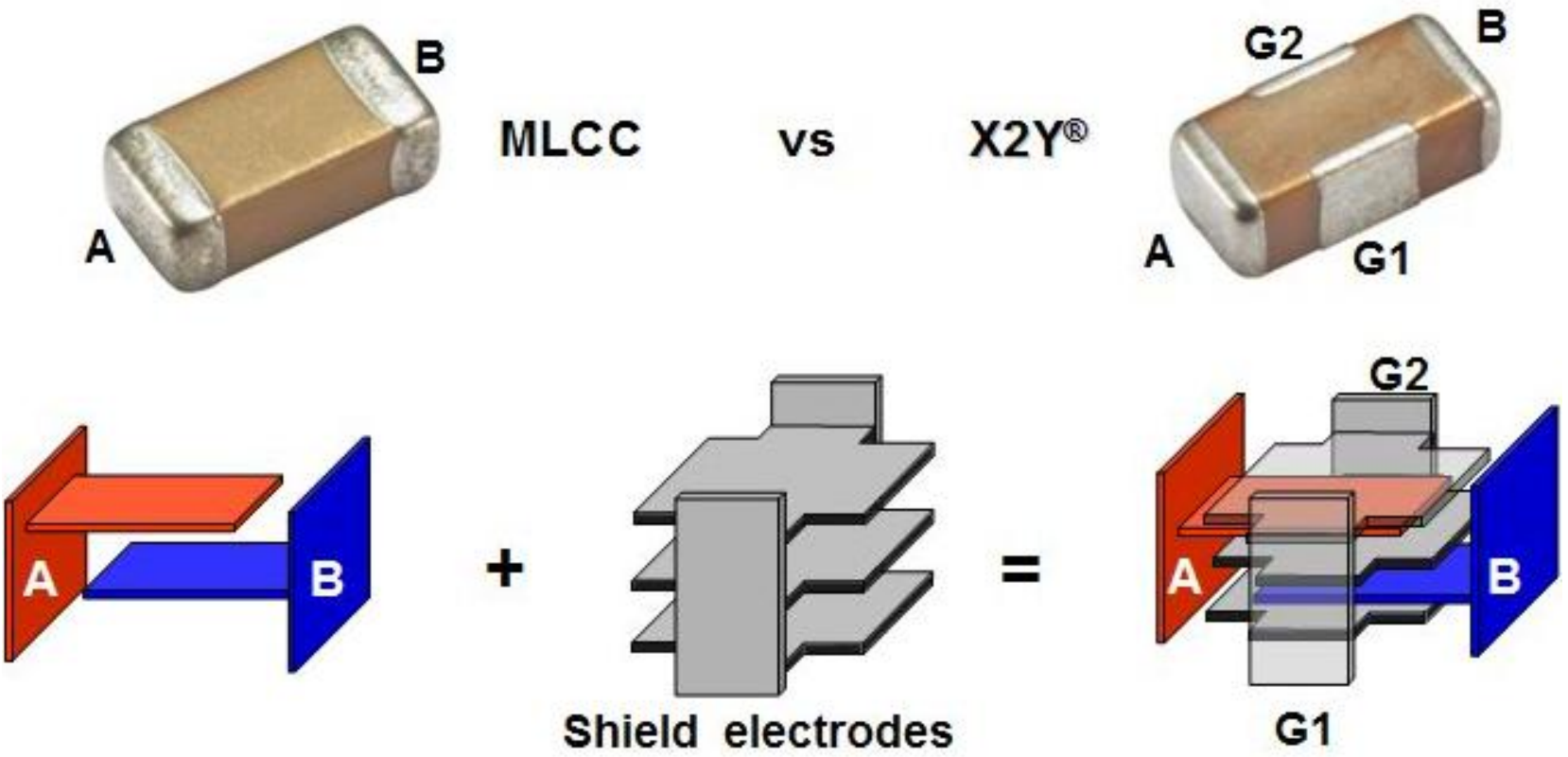
X2Y® Overview

Internal Design



Standard two terminal MLCCs contain opposing electrode sets, labeled A and B while the X2Y design adds shield or ground electrodes surrounding each A and B electrode set. These shield electrodes connect at the center termination bands of the device, labeled G1 and G2. (Click here for an audio version)

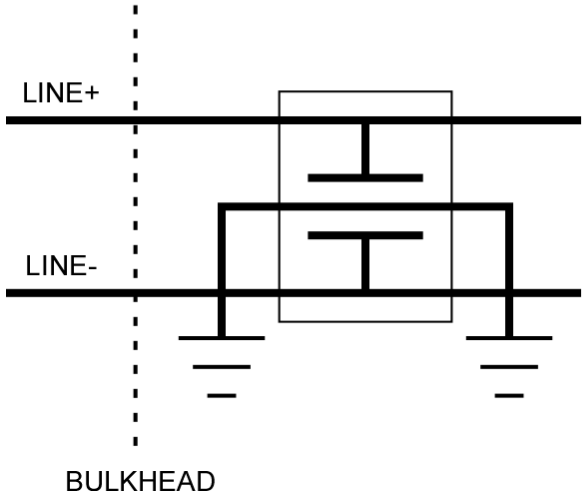
X2Y® Overview

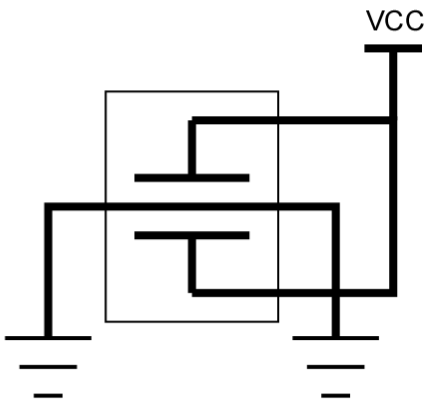
Technology in Balance

Unique Three Node, Four Terminal Component

CIRCUIT 1
RFI FILTER
SMALL, LOW-COST,
VERY EFFECTIVE

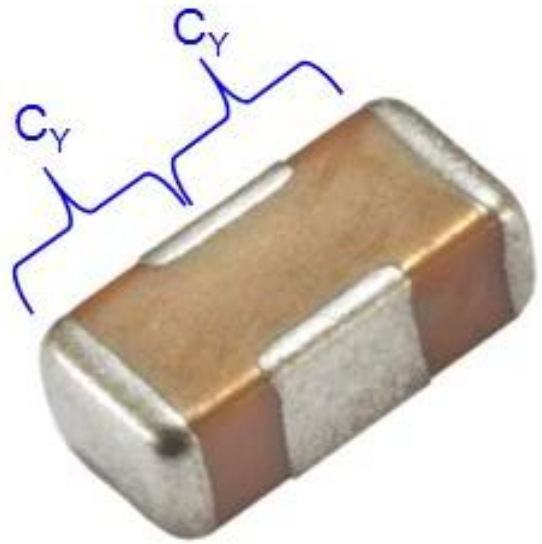
CIRCUIT 2
BYPASS CAPACITOR
TYPICALLY
REPLACES 4 MLCC CAPS





X2Y® Overview

Balance by Design

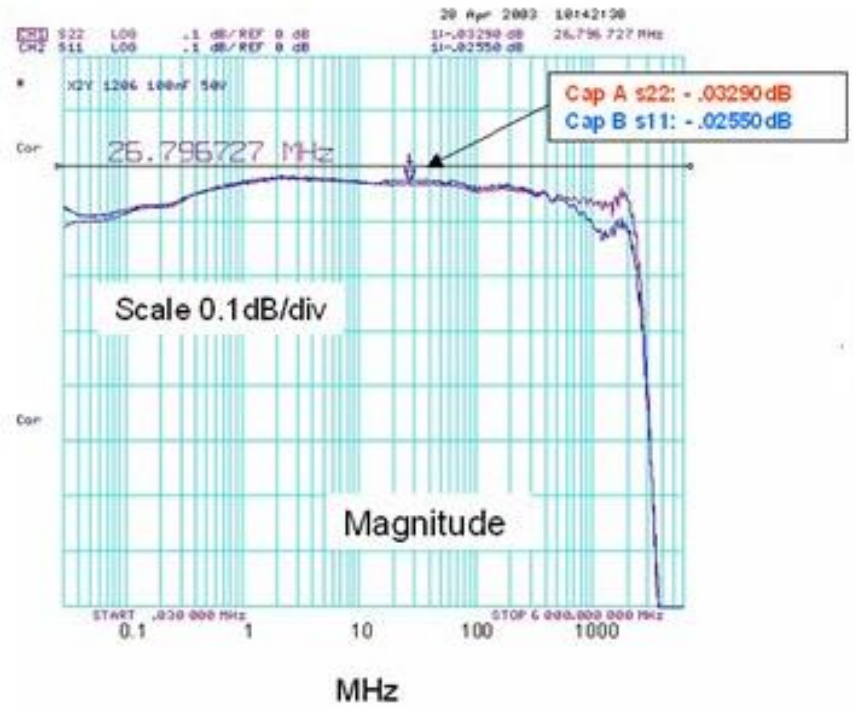


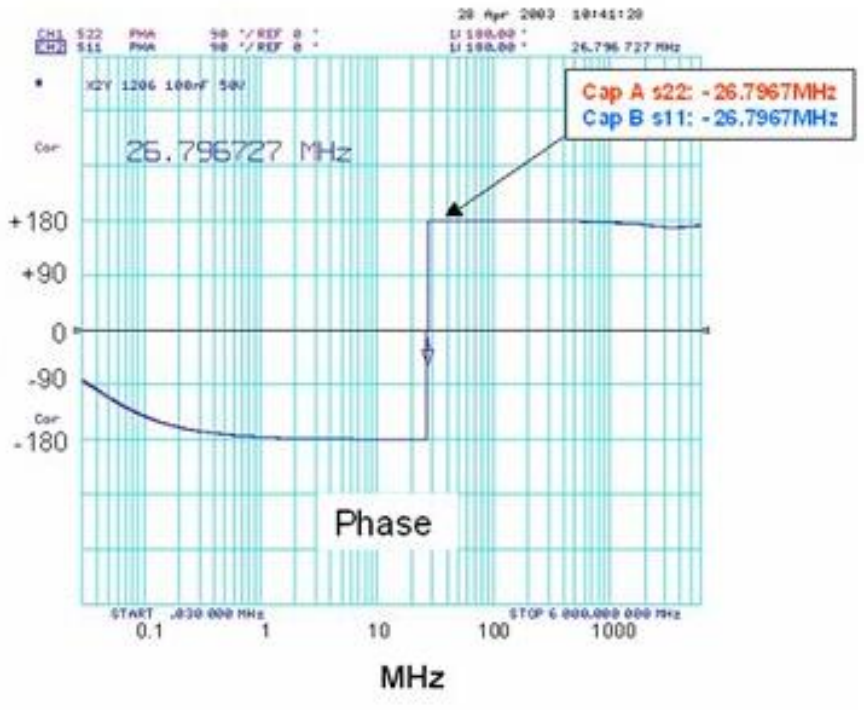
- Matched Y capacitors
- Y caps share same mounts
- PCB traces are uniform
- Temperature and voltage effects are equal on both Y caps at all times

There are many advantages to having both Y capacitors present in one device. In addition to the balanced internal electrode structure, the external effects of voltage, time, and aging are equal on both capacitors at all times. Also, the PCB layout for the device is inherently balanced compared to two discrete capacitors. These factors lead to exceptional common mode rejection for EMI filtering applications.

X2Y® Overview

Balance by Design

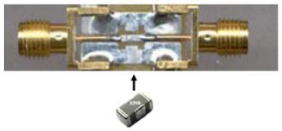


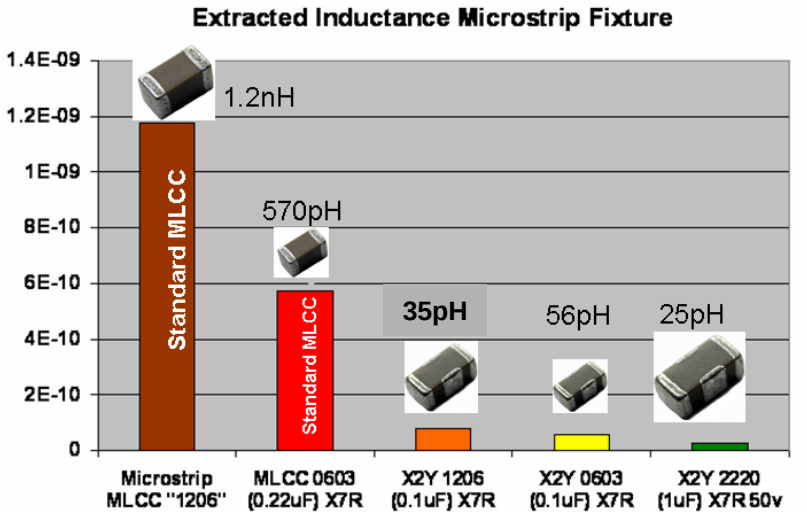


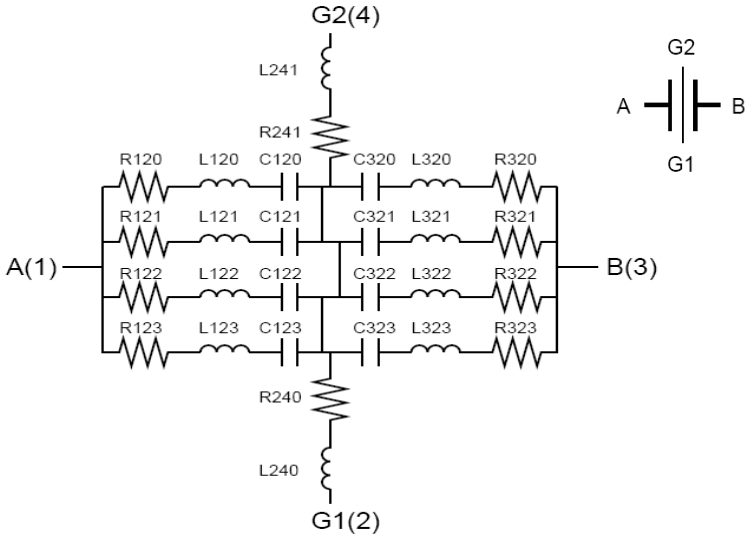
The magnitude and phase of the X2Y's A & B capacitors track almost identically from 1.0kHz up to 6GHz. This balanced performance translates to high common mode rejection in EMI filtering applications.

X2Y® Overview

- X2Y® caps are 1/10th the inductance of a like sized conventional MLCC
- Device-only SPICE models available for Circuit 2 configuration, bypass.
  - Four branch model to represent the field penetration effects at increasing frequency. At sufficiently high frequencies, the plate metalization confines the magnetic field to the plates closest to the PCB, decreasing the effective inductance.
  - R240, R241, L240, L241 (mounting) is effectively zeroe'd out.

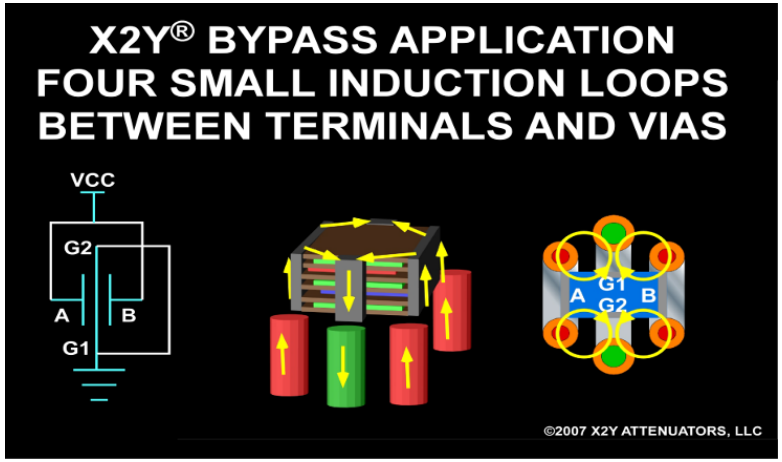




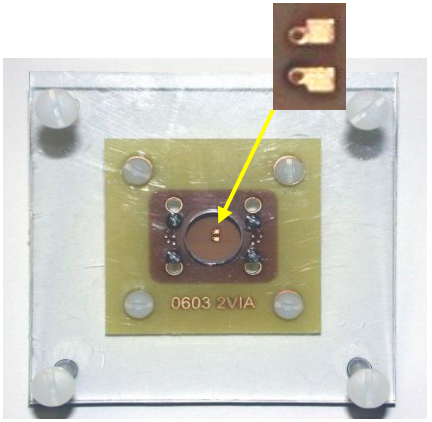


X2Y® Test Fixtures

- Mounted Capacitor Inductance
- Teraspeed/SigCon test cards

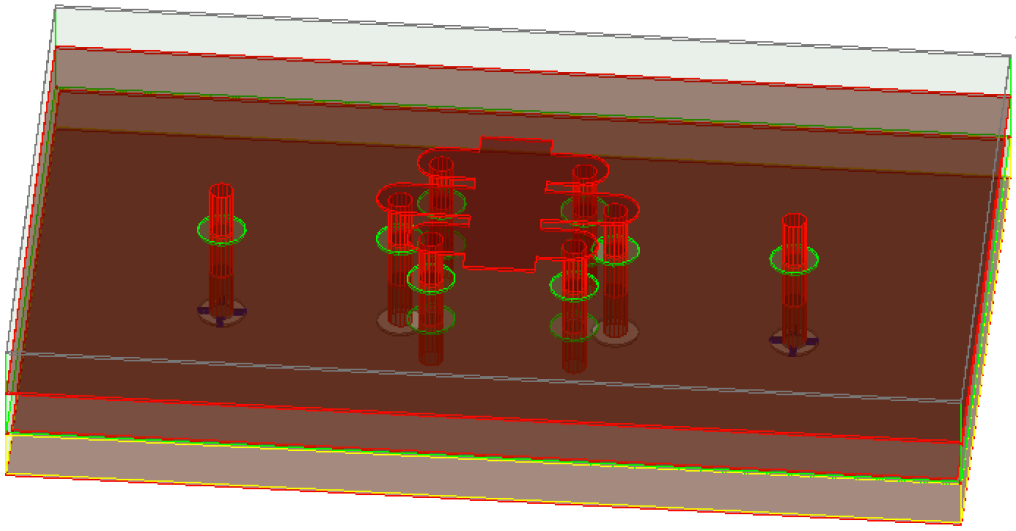


	X2Y	0402	Ratio
Surface	114pH	465pH	4.1:1
5 mils	137pH	575pH	4.1:1
14 mils	180pH	773pH	4.3:1
60 mils	396pH	1784pH	4.5:1



RF Cavity Modeling

RF CAVITY MODEL

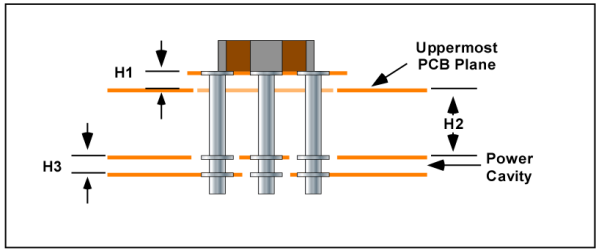


Top Layer Land Pattern w/Short

PCB Top RF Plane
No Capacitor Connections

Power Cavity Top Plane

Power Cavity Bottom Plane



Simberian
Electromagnetic Solutions

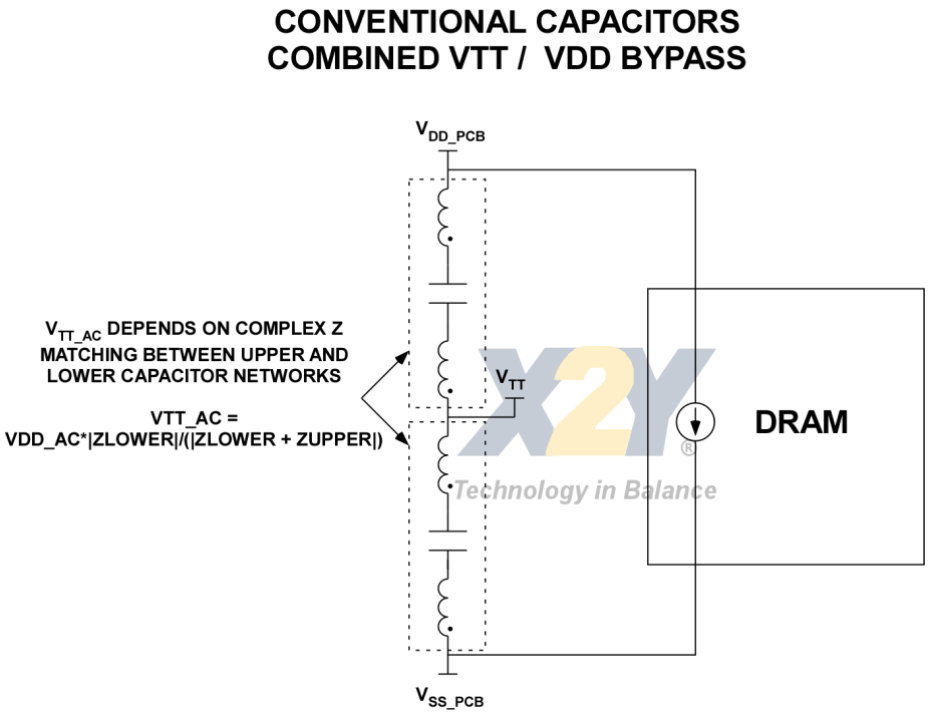
X2Y®
Technology in Balance

X2Y® In DRAM APPLICATIONS

- X2Y® Mounted inductance better than 4:1 conventional caps.
  - Total 25% fewer vias used w/ X2Y®.
- X2Y® Circuit 1 has unique advantages for V_{TT} bypass:
  - Balanced construction insures tight match of V_{TT_AC} to $V_{DD\_AC}/2$ at the PCB.
  - Through inductance in V_{DD} to V_{SS} loop of only one capacitor.
- X2Y® V_{TT} bypass also provides useful V_{DD} bypass.

X2Y® Combined V_{TT} / V_{DD} BALANCE

- AC voltage ratio at V_{TT} depends on the ratio of complex impedance magnitude between combined upper and lower bypass networks.
  - Conventional capacitors unit to unit and mounting variations disturb balance
  - X2Y® Circuit 1, balance is inherent



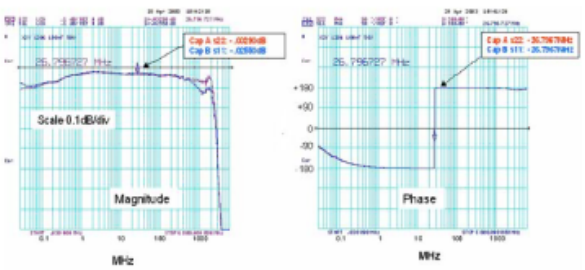
X2Y® Combined V_{TT} / V_{DD} BALANCE

- Inherent impedance balance of X2Y® A/B sides versus frequency insures better $V_{DD}/2$ tracking on V_{TT} than w/ conventional capacitors.

X2Y® CIRCUIT 1
COMBINED VTT / VDD BYPASS

Tightly Balanced Parasitics
< 0.1dB DIFFERENCE TO 1GHz+
Insure 50% Voltage Division
Across Frequency
$V_{TT\_AC} = V_{DD\_PCB\_AC} / 2$

Balance by Design



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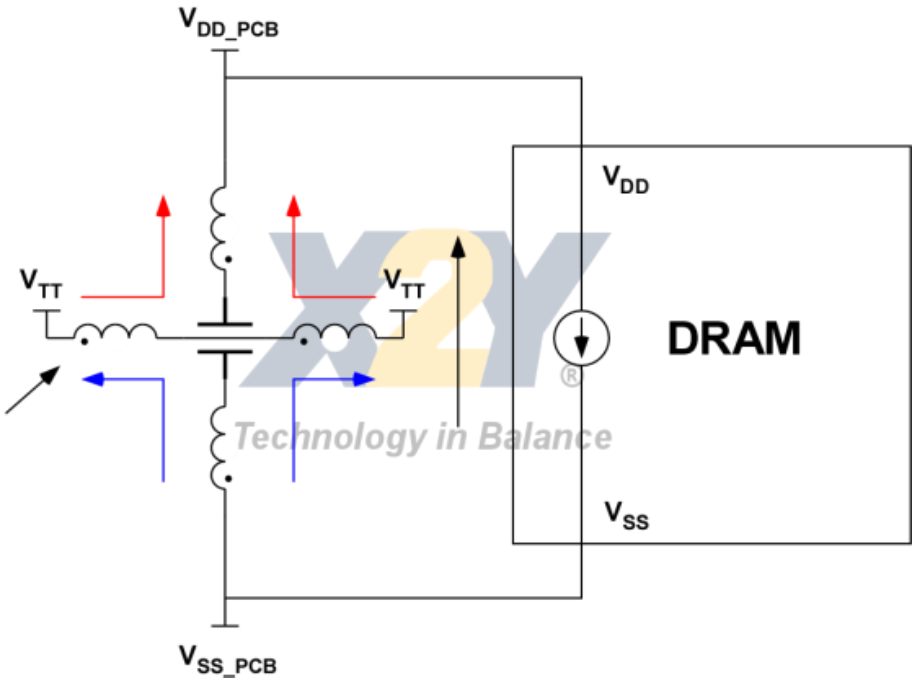
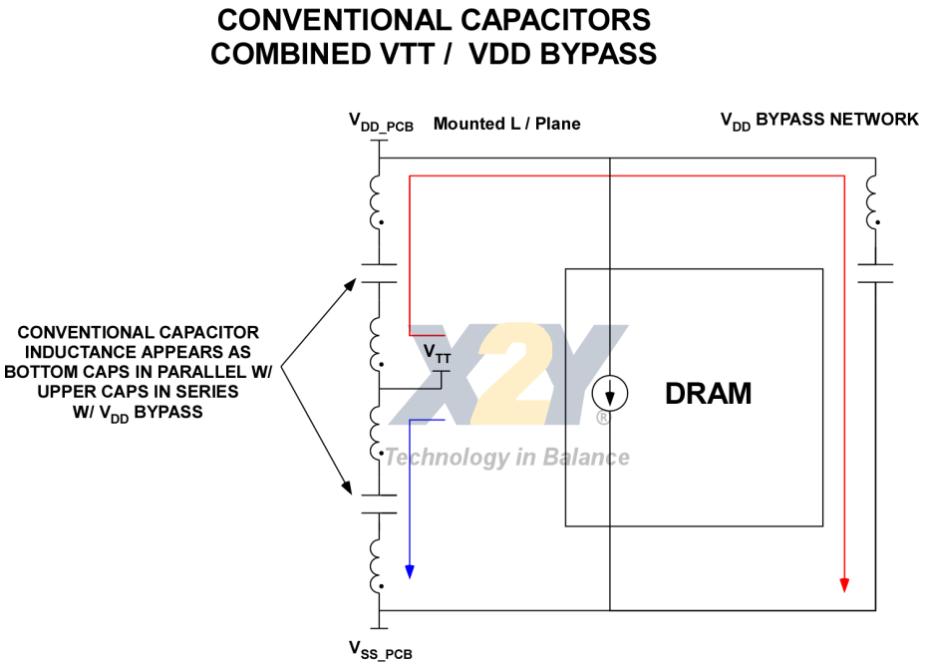


Inductance Presented to V_{TT} Loads

- Conventional presents combined mounted ESL of two capacitors in parallel.
- X2Y® presents effectively better than mounted ESL of four capacitors in parallel.

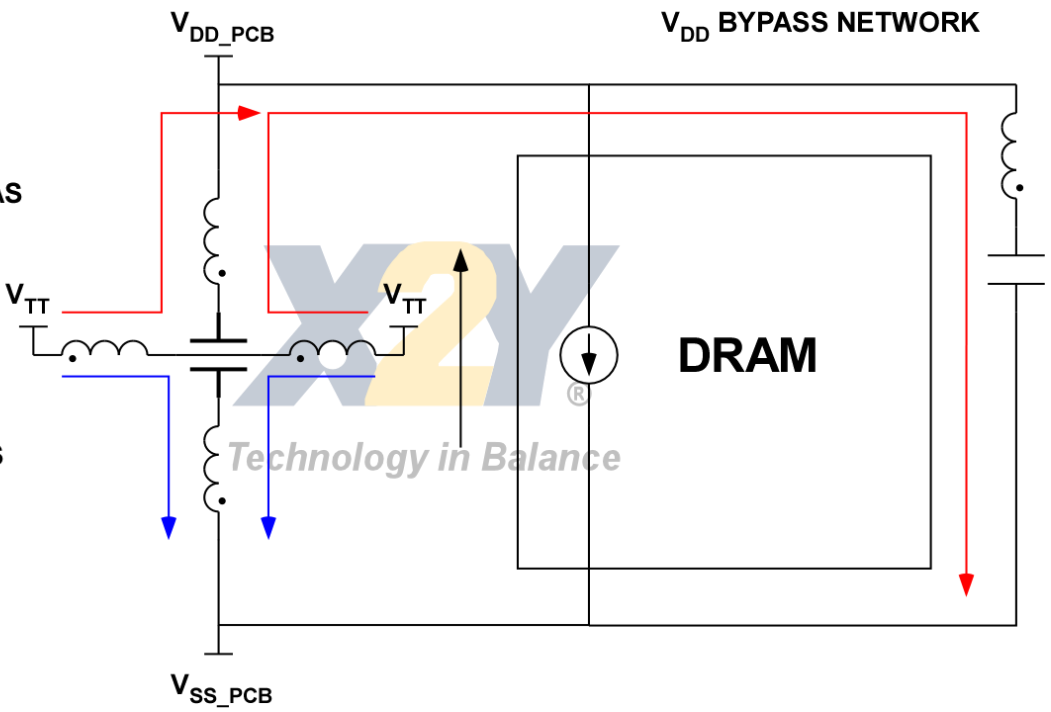


X2Y® Inductance Presented to V_{TT} Loads

X2Y® CIRCUIT 1
COMBINED VTT / VDD BYPASS

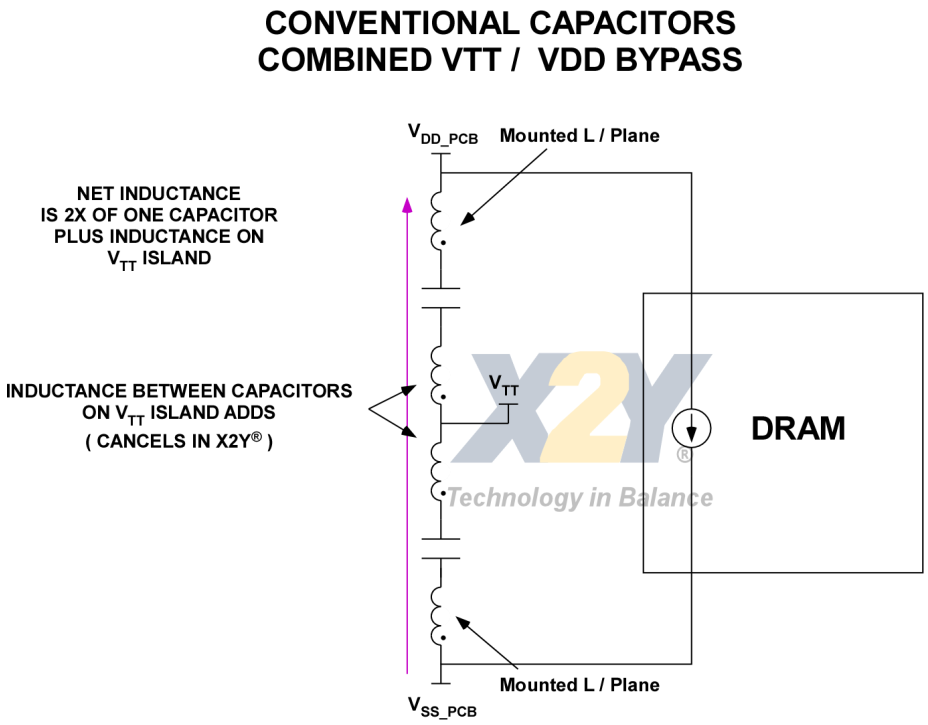
X2Y® INDUCTANCE APPEARS AS G1/G2 TO A IN PARALLEL W/ G1/G2 TO B IN SERIES W/ V_{DD} BYPASS NETWORK

ON A CAPACITOR BY CAPACITOR BASIS < 1/2 THE INDUCTANCE OF TWO CONVENTIONAL CAPACITORS IN PARALLEL.



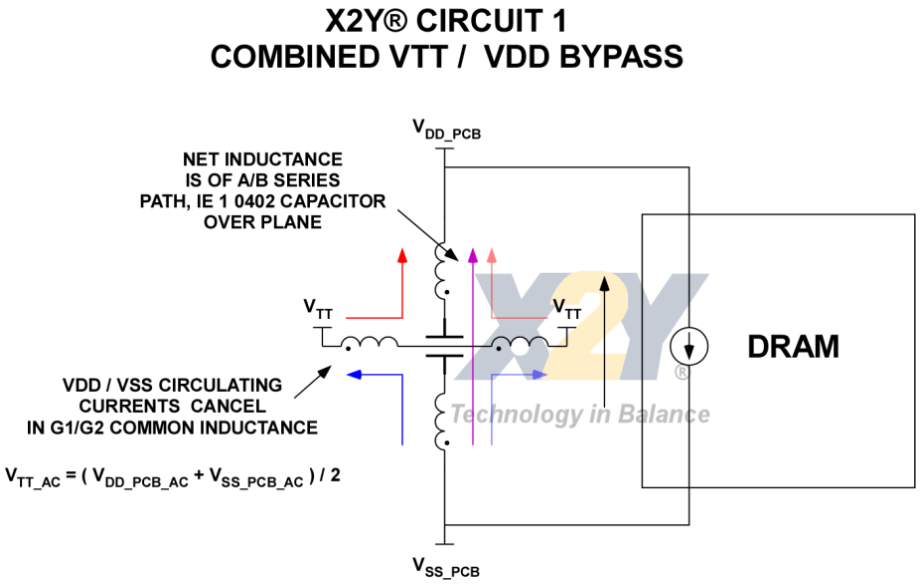
Conventional Combined V_{TT} / V_{DD} Loop Inductance

- Inductance presented to VDD / VSS loop is the series combination of the elements.
  - Conventional Caps:
    - 2X caps, + island between caps.
  - X2Y Circuit 1
    - 1X capacitor body



X2Y® Combined V_{TT} / V_{DD} Loop Inductance

- X2Y Circuit 1
  - Only one capacitor in series path from V_{DD} to V_{SS}
  - V_{DD} / V_{SS} loop currents cancel in G1 / G2 inductance.
    - G1/G2 and VTT effectively transparent.
  - No additional inductance due to interconnect island between capacitors.



Summary X2Y® In DRAM Bypass

- Straight inductance = impedance proposition:
  - X2Y® translates to 4:1 component, and 25% via reduction.
- X2Y® Circuit 1 improves V_{TT} AC tracking of $V_{DD}/2$.
  - Balance is inherent part by part.
- X2Y® improves V_{TT} bypass inductance typically more than 4:1 by component versus conventional.
- X2Y® used for V_{TT} bypass provides useful bypass to V_{DD} that conventional capacitors typically do not.