Low-power, high-intercept interface to the ADS5424 14-bit, 105-MSPS converter for undersampling applications

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With the advent of very highly linear ADC input stages, parts like the ADS5424 can deliver >75-dBc spurious-free dynamic range (SFDR) for two-tones at 170 MHz. The last-stage interface to this converter then needs to be better than 80-dBc two-tone SFDR to take full advantage of this exceptional performance in the converter itself. Until recently, the only amplifier solutions that have met this demanding performance level have been very high-power RF amplifiers, typically using >1.5 W to reach >80-dBc SFDR levels. A much lower-power alternative has recently emerged using the THS4509. This wideband fully differential amplifier, along with a number of external design tricks, can support this last-stage interface requirement using <200 mW of total power. This article steps through the design, measurement techniques, and resulting performance levels required to provide >80-dB SFDR at up to 170 MHz in support of the ADS5424.

Converter two-tone undersampling performance

Numerous applications are asking high-speed ADCs to deliver very high SFDR for narrowband applications at the various intermediate frequencies (IFs) used in communications. These include applications at 44 MHz, 70 MHz, 140 MHz, and 170 MHz. Recent converter introductions (such as the ADS5424) have done a very good job of meeting >80-dBc SFDR at the lower IFs and even >75-dBc SFDR at 170 MHz. Figure 1 shows a plot from the datasheet (Reference 1) of a two-tone SFDR for the ADS5424 at 170-MHz center frequency.

In this test, the converter is sampling at 92.16 MHz on a two-tone input at 169.6 MHz and 170.4 MHz. The input frequencies are falling in the fourth Nyquist zone and are folded to the difference between 4fs/2 and 170 MHz, giving the 14-MHz fast Fourier transform (FFT) output shown in Figure 1. Each tone here is at –7 dBFS so that the combined two-tone envelope sums to a –1-dBFS maximum. The full-scale input voltage for the ADS5424 is a 2.2-V_{PP} differential, giving a –1-dBFS level of 1.96 V_{PP} with each tone then at 0.98 V_{PP}. The converter plot report shows IMD3 = –82 dBFS, where this is the absolute level below 0 dB in Figure 1. The difference between each carrier level and the third-order intermodulation spurious signal level is more commonly used for amplifiers. To translate the converter specification to something that is comparable to amplifier specifications, subtract 7 dB from |IMD3|, just given, resulting in a 75-dBc third-order SFDR for the converter. This exceptional performance is the difference between the carrier level and

Figure 1. Two-tone SFDR for the ADS5424 at 170-MHz ±400-kHz input frequencies

f_S = 92.16 MSPS
$f_{IN}1$ = 169.6 MHz, –7 dBFS
$f_{IN}2$ = 170.4 MHz, –7 dBFS
IMD3 = –82 dBFS
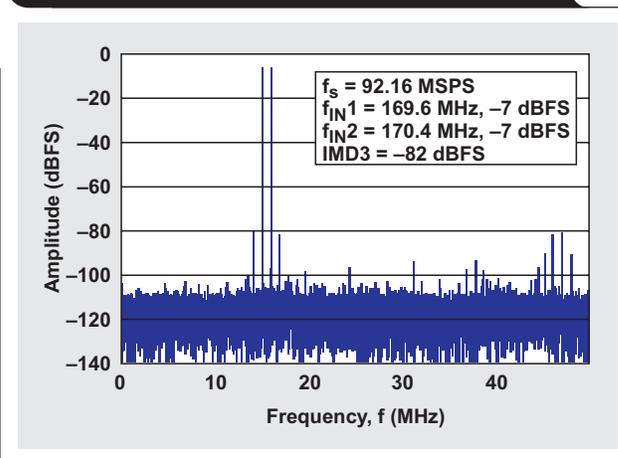
Figure 2. Simple characterization circuit for the ADS5424
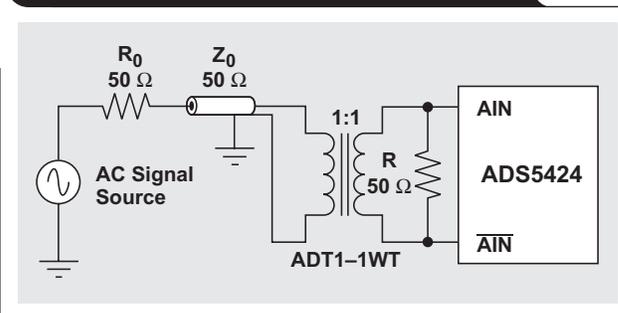
the average spurious signal level at a 170-MHz center frequency. The converter is also generating another cluster of spurs near 42 MHz, but it is the close-in third-order intermodulation terms that are of interest in developing an amplifier interface compatible with this level of ADC performance.

The test interface to get this plot for the converter is quite specific and depends on very high-quality sources (from a phase-noise standpoint) with moderate linearity. Each source is heavily filtered before the power combiner then drives the signal into a 1:1 transformer to get the differential converter input signal. This simple interface is shown in Figure 2 (from Reference 1), where the real magic is in getting the element called "AC Signal Source."

The input signal during the converter test is so heavily filtered that it is considered spurious-free.

One of the really nice features of the ADS5424 is that the differential input provides its own common-mode reference voltage and resistive termination, which then drive on-chip buffers prior to the sampling element. Figure 3 shows the analog input stage for the ADS5424. V_{REF} is sitting at 2.4 V when the power supply is +5 V on the analog portion of the ADS5424.

Figure 3. Differential analog input for the ADS5424
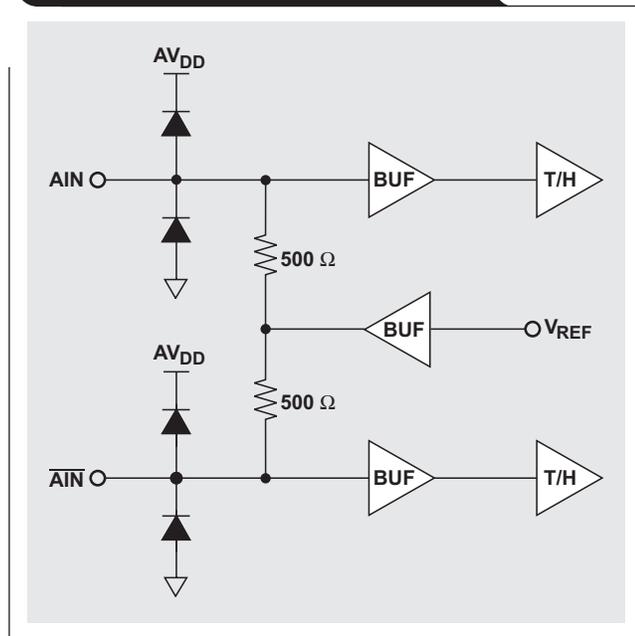
Target distortion levels for the last-stage interface to the ADS5424

Now we must estimate a target SFDR for the signal coming into the converter to hit some level of system performance. Imagine a two-tone input signal that has its own set of close-in spurious tones being presented to the converter input. The converter will process the fundamental tones to generate the converter spurious power levels shown in Figure 1. The spurious tones presented at the input are also processed by the converter as a signal and passed on to the FFT output combined with the converter-generated spurious signals at the same frequency. A worst-case

assumption, which actually has been shown to hold true at lower frequencies, is that these spurious tones add in phase. For instance, the –82-dBFS close-in spurs of Figure 1 imply a spurious signal of 2.2 V_{PP} × $10^{-82/20}$ = 175 µV_{PP}. If the input signal also has this same level of third-order spurious tones (which would be falling at 170 MHz ± 3 × 400 kHz), the final FFT output would have 2 × 175 µV_{PP} = 350 µV_{PP} in the FFT, or –76-dBFS worst-case. So, providing an input signal with the same two-tone SFDR as the converter results in a combined 6 dB worse than the converter alone. This is normally not acceptable, suggesting that the SFDR for the signal coming into the converter must be much higher than that of the converter itself to minimize degradation in system performance. While this may be a worst-case assumption, it will set a target for the amplifier performance. Equation 1 shows the combined SFDR calculation when the spurious signal levels are adding in phase.

$$ SFDR_{System} = -20 \log \left(10^{\frac{-SFDR_{ADC}}{20}} + 10^{\frac{-SFDR_{Amp}}{20}} \right) \qquad (1) $$

SFDR, a positive number, is the difference in dBc between the carrier and the close-in spurs.

In Equation 1 we must enter the SFDR defined in the same way. For instance, from Figure 1, the ADC has a 75-dBc SFDR. If the signal to the converter has an $SFDR_{Amp}$ of 82 dBc, then the combined $SFDR_{System}$ will be 71.8 dBc. This approximate 3-dB degradation requires an input signal with an SFDR at least 7 dB better than that of the converter. Equation 1 can also be solved for the required $SFDR_{Amp}$ to hit a target $SFDR_{System}$:

$$ SFDR_{Amp} = SFDR_{ADC} - 20 \log \left(10^{\frac{\Delta}{20}} - 1 \right), \qquad (2) $$

where Δ is the desired drop in SFDR. With Δ defined as a positive number, Equation 2 will add to the $SFDR_{ADC}$ to get the amplifier target. Note that this calculation is independent of the starting level for $SFDR_{ADC}$. For instance, a 1-dB drop requires the amplifier to be 18.3 dB better than the converter regardless of the starting point for the converter. An exact 3-dB drop would require the input signal to have an SFDR 7.7 dB better than that of the converter itself.

Typical amplifier solutions

Since most designs are converting to differential in the last stage, a typical design would use a very low-distortion RF amplifier driving a transformer. This has worked reasonably well in the past but typically requires in excess of 1.5 W in the amplifier to suppress its spurious signals to the levels

calculated earlier. A typical interface, shown in Figure 4, bears a marked resemblance to the converter test circuit.

This design is encumbered by two issues that require very high-power dissipation in the amplifier to achieve the desired linearity. The first issue is that the full-scale converter input is required at the amplifier output, since there is no further gain to the converter input. Some step-up in the transformer can be used to reduce this swing, but high turns ratios run into a band-limiting problem in the transformer. The second issue is that the single-ended output of the amplifier is not taking advantage of the even-order suppression available in a differential design. It is much tougher to get even-order suppression single-ended, again leading to very high-power dissipation in the amplifier. While the discussion thus far has focused on third-order intermodulation, the second-order and higher harmonics have to be dealt with at some point. Taking a single-ended signal path to differential at low-power level, then providing the final gain stage in a very balanced differential design, will go far towards removing the even-order terms as a limit to dynamic range. With the cost of one more transformer, all these problems go away and a much lower-power, very high-SFDR design can be delivered with the THS4509.

Low-power ADC interface with exceptional SFDR

Moving the transformer to the input of a balanced differential interface allows the final single-ended amplifier driving that transformer to operate at a much lower power level.

Figure 4. Single-ended amplifier driving a last-stage transformer
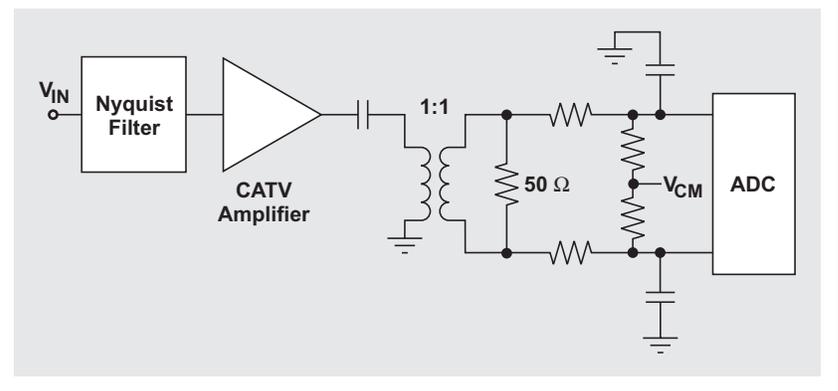
Normally, every dB of reduction in fundamental power level will reduce the even-order harmonics by 2× and the third-order harmonics by 3×. For instance, if an arbitrary single-ended amplifier is driving the full 2 V_{PP} at its output (10 dBm) and delivering –70-dBc second-order and –80-dBc third-order harmonics, dropping its output level by 20 dB to –10 dBm will drop the second-order harmonic down to –90 dBc and the third-order to –120 dBc. This is why moving the single-to-differential conversion upstream in the signal path can move the SFDR limit to the final stage, where running differentially has numerous advantages.

Figure 5 shows some earlier work in this topology where a very wideband current feedback amplifier, the OPA695, was used. This example was intended for the first Nyquist zone and included a second-order low-pass filter at the output to limit the noise-power bandwidth (see Reference 2).

Figure 5. Example input transformer-based circuit using the OPA695
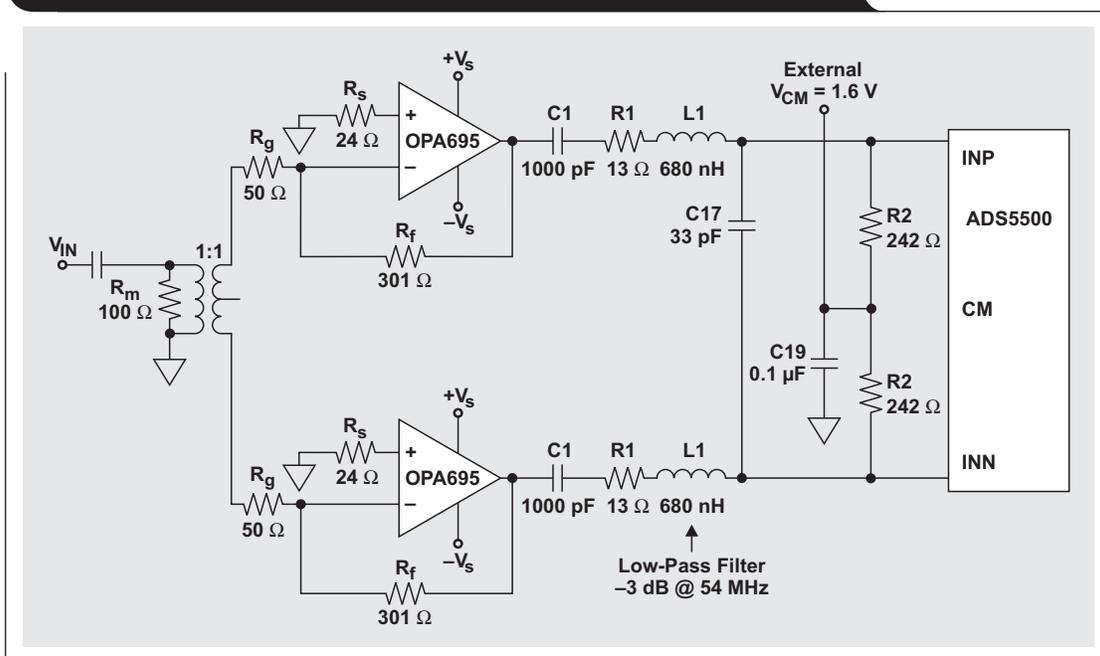
Adding a transformer to the input can improve dynamic range (reduce noise and distortion at the converter input) in at least three different ways.

1. The transformer provides a noiseless and distortionless signal conversion from single-ended to differential. This is very useful for ac-coupled signal requirements.

2. The signal gain from the transformer secondary is greater than the gain for the amplifier's voltage noise. This has the effect of reducing the contribution at the output for the amplifier's input voltage noise, or, equivalently, attenuating the amplifier input voltage noise contribution to the total noise when it is input-referred to the signal input at the transformer primary.

3. Similarly, if the amplifier is a voltage feedback device (like the THS4509, but not the OPA695), this reduced noise gain versus achieved signal gain also increases the loop gain for the amplifier. Increased loop gain will, all other things being equal, reduce harmonic distortion at the output.

The transformer interface of Figure 5 used a 1:1 transformer where a 50-Ω input match was desired. This was achieved with 100 Ω on the input side and two 50-Ω resistors on the secondary, where those reflect back to the input side as their sum—again, 100 Ω. A more general low-noise development (shown in Figure 6) would let the turns ratio be adjustable, eliminate the 100 Ω on the input side, and simply set $2R_g$ to get the required input impedance. The impedance looking out of the transformer secondary is the sum of the two R_g resistors, since the inverting amplifier inputs are assumed to be low-impedance points.

Then, with R_g set, R_f would be selected as needed to get the desired gain. Figure 6 shows the simplified circuit used to develop the noise figure (NF) equation (Equation 3) for this inverting-input, transformer-coupled design.

Figure 6. Noise figure analysis circuit
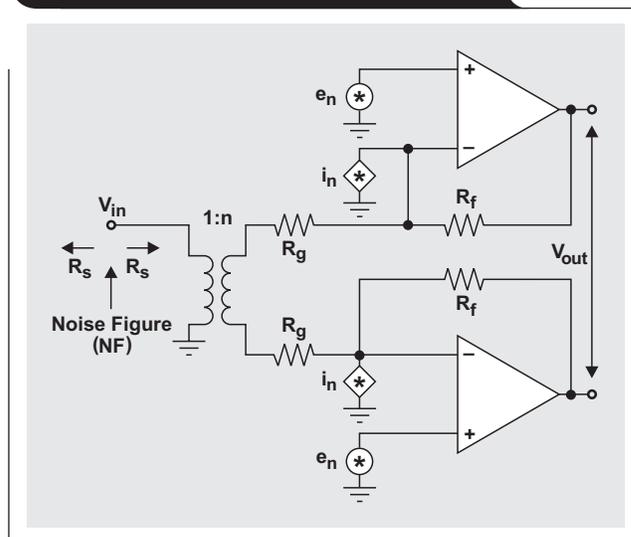
To get an input match, define $\alpha = R_f/R_g$ and set $R_g = \frac{1}{2}n^2R_s$, where n is the turns ratio and n^2 is the impedance ratio. Then $V_{out}/V_{in} = n\alpha \equiv A_v$, and R_f will be $(A_v/2)nR_s$.

While not shown in Figure 6, all the resistor noise terms are included in this analysis. Since R_g and R_f are so constrained by the input impedance and target gain requirements, they drop out explicitly from the total NF expression of Equation 3 but are effectively picked up by the $2+4/\alpha$ term:

$$NF = 10\log\left(2+\frac{4}{\alpha}+2\left\{\left[\frac{e_n\left(\frac{1}{2}+\frac{1}{\alpha}\right)}{n}\right]^2+\frac{1}{2}\left(i_b n R_s\right)^2\right\} \div kTR_s\right). \quad \textbf{(3)}$$

It is interesting to sweep the turns ratio and recompute the noise figure while holding a fixed target gain. Figure 7 does this for the OPA695, the THS4509, and the lowest-noise Texas Instruments op amp, the OPA847. While the THS4509 is a fully differential amplifier and not strictly an op amp, the analysis model in Figure 6 shows two equal voltage-noise sources (e_n) at the input that are equal to the THS4509 specified voltage noise divided by $\sqrt{2}$.

Figure 7. Input noise figure vs. turns ratio with fixed total gain for the circuit in Figure 6

All of these devices show a shallow minimum where going from a 1:1 turns ratio to some higher input turns ratio will improve NF. The OPA695 gets worse at higher turns ratios due to the dominant output noise term coming from its relatively large inverting current noise. That term becomes dominant at low amplifier gains—which is what happens in this analysis as the turns ratio increases for a fixed target total gain.

Table 1 summarizes the noise terms used in Equation 3 to generate Figure 7 (with $R_s = 50 \, \Omega$ and $kT = 4 \times 10^{-21}$ J). Recall that the THS4509 input noise used here is the actual specification divided by 1.41 to share that single input noise voltage in the two inputs used in the analysis model of Figure 6.

**Table 1. Noise terms used in Equation 3
to generate Figure 7***

DEVICE	e_n (nV)	i_n (pA)
OPA847	0.8	2.5
OPA695	1.8	22
THS4509	1.4	2.2

*$R_s = 50 \, \Omega$ and $kT = 4 \times 10^{-21}$ J

While this is an interesting mathematical exercise, it is important to consider other constraints that come into play over this turns ratio sweep. Specifically, as n>3 is used, the transformer will start to limit the bandwidth for high-IF applications. Also, letting R_f be completely driven from the target gain and required R_g value will quickly move it beyond its useful range. For the OPA695, letting R_f get too large will limit the bandwidth of the design. For the THS4509, letting R_f get too low will load the output, increasing distortion.

Tested design with the THS4509

Numerous efforts were made to find a working solution at 170 MHz that would not drop the ADS5424 two-tone performance of 75 dBc more than 3 dB. This gave an 82.7-dBc target for the amplifier SFDR with the analysis detailed earlier. Figure 8 shows the final configuration for just the amplifier portion of the circuit that has given the best results. A total gain of 10 V/V, or 20 dB, was targeted in these tests. Therefore, a –1-dBFS input to the converter requires a maximum input swing at V_{IN} of 200 mV_{PP}.

Early tests with just the input transformer did not meet the distortion targets. Reducing the amplifier gain by 1.4 and adding a 1:1.4 turns ratio output transformer helped both to improve the loop gain and to lighten the output swing requirement for the THS4509 so it can now meet the target.

The output transformer does not run doubly terminated, while the input transformer does provide a match to the source. It was assumed that the source needs to see a matched load for proper operation, while the output can (thus far) drive into the converter input impedance with no consideration of source matching. The output transformer provides 1.4-V/V gain that is removed from the THS4509 gain setting to still hit the target gain of 10 V/V.

We intended to test only the THS4509 with this test circuit to see if we could extend the performance to meet the SFDR target by using several design tricks:

1. This circuit runs completely differentially around ground. It does not use the internal common-mode loop (in an ac sense) in an effort to improve high-frequency linearity. The common-mode loop still controls the output common-mode voltage, but minimal dc, and hopefully no ac, current signal is required to do this for the implementation chosen.

Figure 8. Tested THS4509 circuit
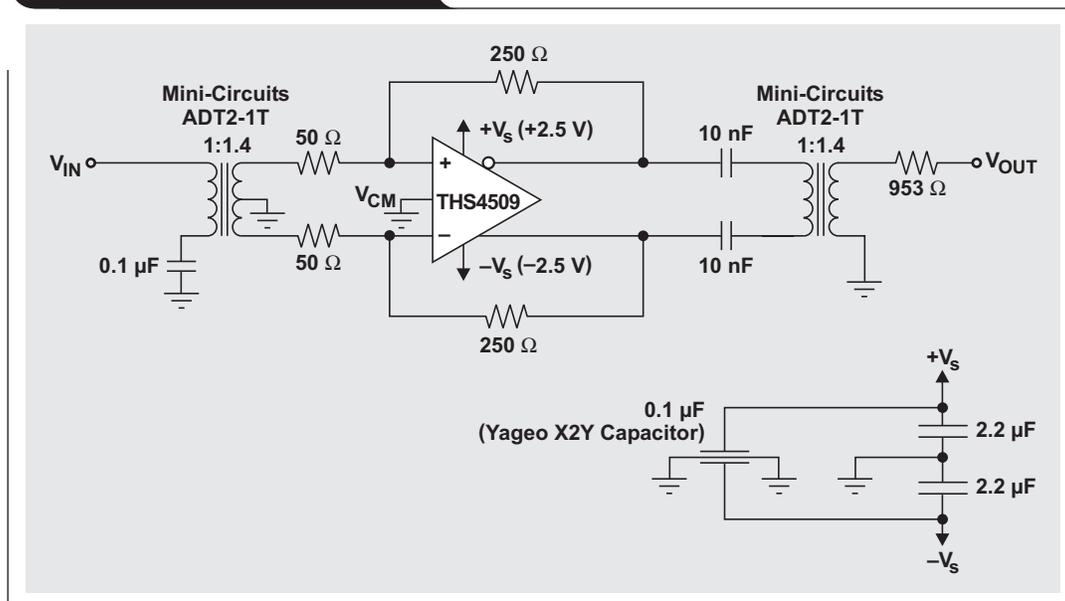
2. Testing and design are simplified with ±2.5-V supplies. Putting both the input transformer centertap and the V_{CM} pin at ground should eliminate common-mode currents and signals.

3. The signal path is ac-coupled at both the input primary and the outputs of the THS4509, eliminating dc currents.

4. While the THS4509 provides a gain of 5 for each side of the differential input signal, its noise gain is somewhat lower. Reflecting the 50-Ω source through to the secondary as 50 Ω on each side [$50 \times (\sqrt{2})^2$] and computing the equivalent noninverting gain, we get $1 + 250/100 = 3.5$ V/V. This is high enough to ensure stability in the THS4509 but lower than the signal gain delivered, which should improve loop gain and hence distortion by a factor of $20\log(5/3.5) = 3.1$ dB over a simple noninverting stage gain of 5.

5. The final output drives out through a 953-Ω resistor to a 50-Ω spectrum analyzer. This is intended to emulate the 1-kΩ input impedance of the ADS5424. Reflecting that load through to the THS4509 outputs, we see what looks like a 500-Ω load across the outputs. Each output

then sees half of this in parallel with the feedback element as a total load, or 125 Ω in Figure 8.

6. To get 2 V_{PP} at the transformer secondary (the required –1 dBFS for the ADS5424), $2/\sqrt{2}$ must be driven differentially at the THS4509 outputs. Dividing the result by 4 gives ±0.355 V on each output, which then drives 2.84 mA peak in each direction into the total equivalent load of 125 Ω.

The two-tone, third-order intermodulation test configuration is shown in Figure 9.

Two very low-phase-noise synthesized signal sources are used. One acts as the primary source and the other, along with the spectrum analyzer, is phase-locked to the primary. This allows very narrow frequency spans of where the spur should be. Notice that no filters are used here. The spectrum coming out of the mixer has numerous harmonics we don't care about—but nothing where the third-order intermodulation spurs should be. This test performed on a converter would always use filters for the signal sources, as the converter will fold the higher-order harmonics into the Nyquist zone—possibly falling on top of the spurious signal of interest.

Figure 9. Test configuration for two-tone, third-order intermodulation testing
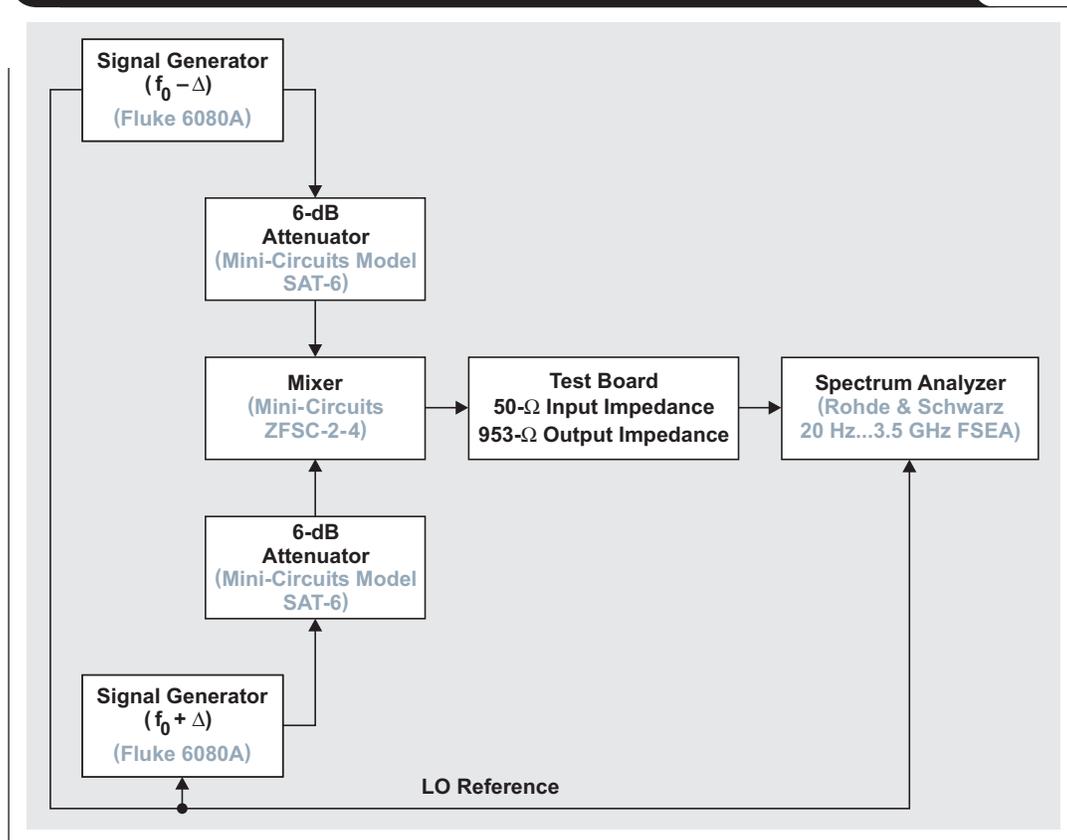
Figure 10. Measured third-order intermodulation spurious signal level
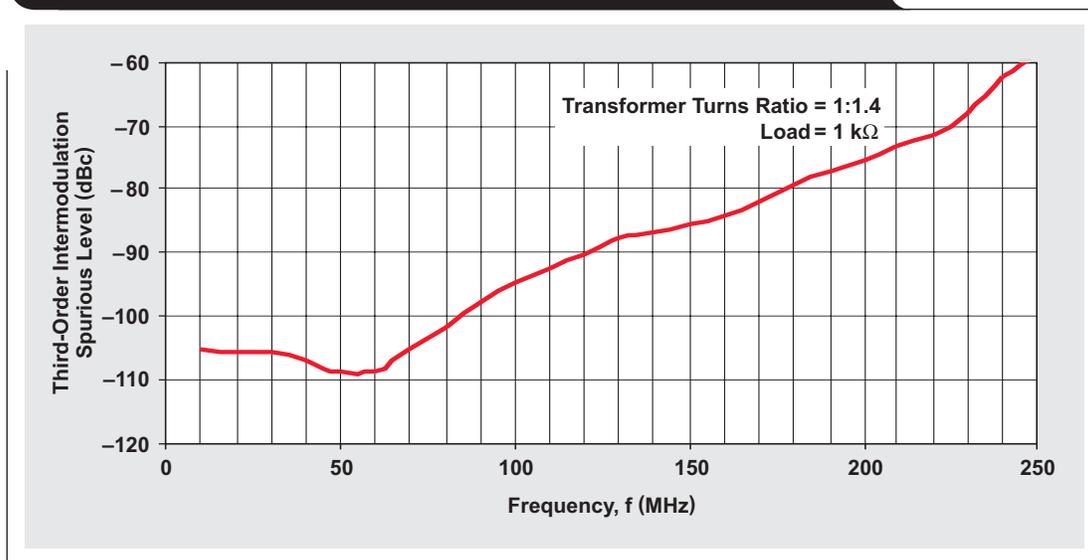
Figure 10 sweeps the center frequency (f_0) and reports the measured level of the close-in third-order intermodulation spurious signal. The SFDR is the negative of the numbers plotted.

This data not only shows the main target of –83 dBc at 170 MHz but also exceptional performance at lower frequencies. To make these lower-frequency measurements, a 4-V_{PP} output test was used, and the spurious level was projected at 2 V_{PP} with an intercept model. Figure 11 shows that at 70 MHz the ADS5424 has a two-tone SFDR of approximately 86 dBc. Again, to get SFDR in dBc, the reported –93 dBFS is adjusted as |SFDR| – 7 dB.

If the –105-dBc SFDR for the THS4509 interface (from Figure 10 at 70 MHz) were combined with the ADS5424 SFDR, the system performance would drop from 86-dBc to 85-dBc SFDR—extremely good performance, particularly when the low 190-mW total power dissipation in the THS4509 is considered (38 mA across a 5-V total supply).

Layout issues

To achieve this very low harmonic distortion, considerable attention to layout symmetry is required. Every effort is made to keep the signal current out of the ground plane and purely differential (see Reference 3). Figures 12 through 15 show the four layers for the test board we developed that resulted in the performance data reported here.

Figure 11. Two-tone SFDR of the ADS5424 at 70 MHz

16
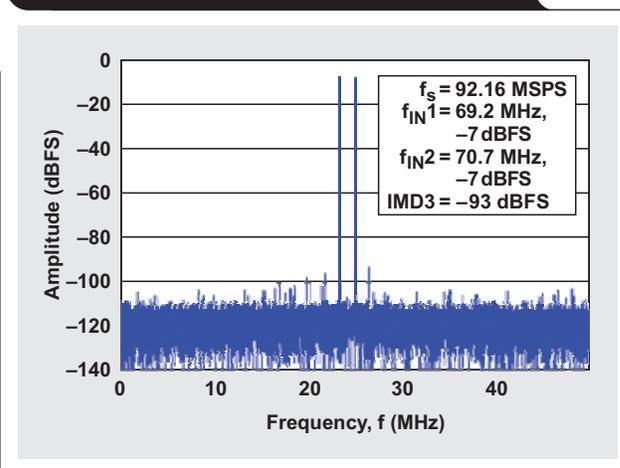
Top layer

To limit trace length around the THS4509 QFN-16 package, 0402-size resistors and capacitors were used (see Figure 12). R2A/B and R3A/B are the gain and feedback resistors. R4A/B are component placeholders that can be either resistors or capacitors. In this case, these placeholders have been populated with 10-nF capacitors as shown in Figure 8. T1 and T2 are transformers. To accommodate different transformer pinouts, pin 2 and pin 5 of T1 are connected together. Note that the transformers tested have a centertap on the secondary winding and no center-tap on the primary. The transformers this board can accommodate used either pin 2 as the centertap with pin 5 as a no-connect, or pin 5 as the centertap with pin 2 as a no-connect.

First inner layer (ground plane)

In the ground plane (Figure 13), note the window opening around the device pins as well as the signal trace to the transformers. This window minimizes parasitic capacitance effects that could push the THS4509 into instability.

Used immediately underneath the top layer, this ground plane can help shield traces from other layers. It can also be used to create controlled-impedance traces.

Second inner layer (power plane)

The power planes (Figure 14) were set to avoid crossing any top-layer signal trace and thus to limit parasitic capacitance. Each power plane is connected to the large bypass capacitors C1 and C2 from the top layer. C1 and C2 can

Figure 12. Top layer, where most components are loaded
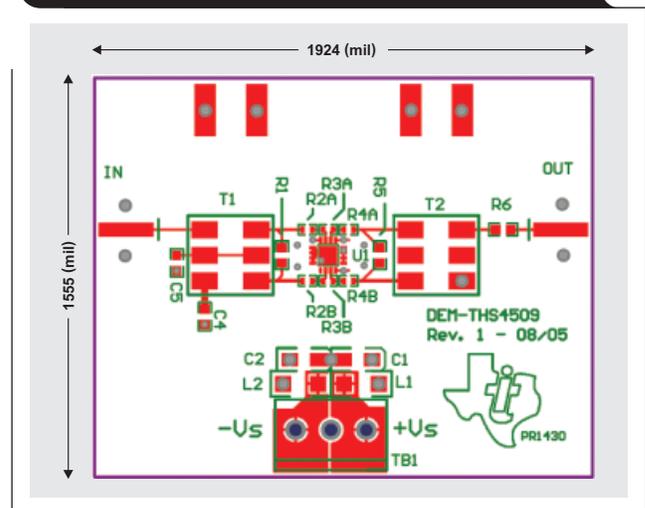
also be used as elements of a low-pass filter formed by the combinations L1-C1 and L2-C2. The L1 and L2 components are optional and intended to be lossy ferrite beads. They were not used for the tests taken here and were replaced with a short. Note in Figure 12 that C1 and C2 are connected together and then connected to the ground plane. This limits the return path traces and maximizes the self-resonant frequency of each capacitor.

Figure 13. First inner layer (ground plane)
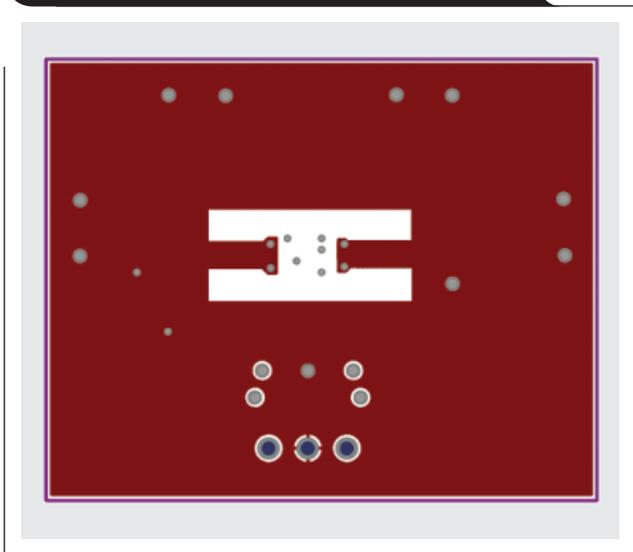
Figure 14. Second inner layer with power connections

17
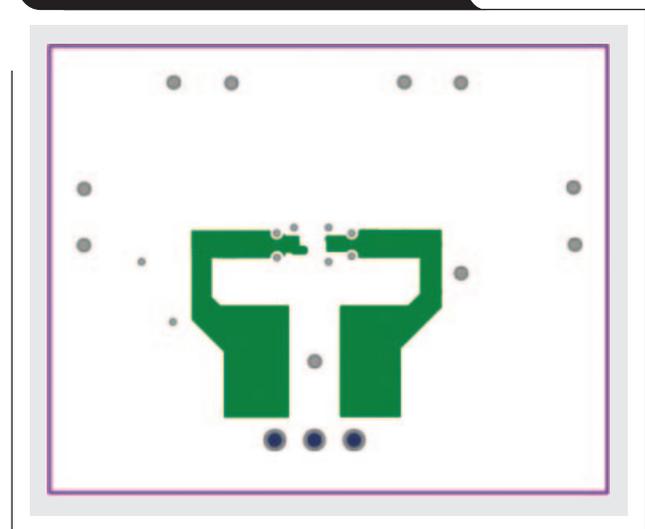
Bottom layer

The key element on this layer (Figure 15) is C3, a very high-quality, four-terminal capacitor from supply to supply. This capacitor replaces three regular capacitors in this circuit—two capacitors from each supply to ground and one capacitor across the supplies—simplifying layout and improving bypassing. For more information on this type of capacitor, go to www.x2y.com

Figure 15. Bottom layer
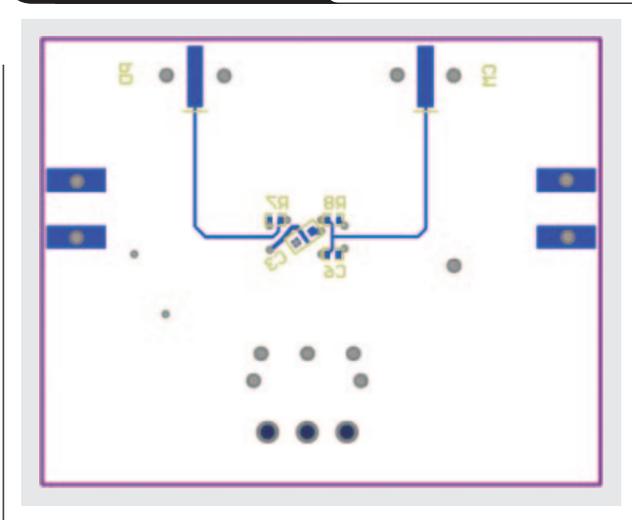
Adapting the THS4509 test circuit to an IF ADS5424 interface

The circuit and testing discussed here have shown that the THS4509 has the intrinsic capability to support the SFDR requirements of the ADS5424 over a wide range of IF frequencies. Actual implementations must also consider the out-of-band distortion terms, single-supply operation, and noise-power bandwidth issues. Most implementations will need to add at least a simple bandpass filter between the amplifier and the converter to limit the noise-power bandwidth and to attenuate the out-of-band distortion

terms generated by the THS4509. Figure 16 shows an example implementation.

This circuit ac couples in a few more places and adds a passive bandpass filter at the input of the converter. This will add some insertion loss to the channel that may require a slightly higher gain in the amplifier to achieve 20-dB total gain in the interface.

Summary

The THS4509 has been shown to provide adequate two-tone, third-order intermodulation levels to support the reported specifications for high-performance, 14-bit ADCs such as the ADS5424. While other approaches have also proven effective, the THS4509 is particularly attractive for its low 190-mW total power dissipation. For specific IF interface applications, an LC filter should be introduced prior to the converter to limit the signal-to-noise ratio and the SFDR degradation due to the broadband noise and distortion at the THS4509 output.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/ *litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "14-Bit, 105 MSPS Analog-to-Digital Converter," ADS5424 Datasheet	slws157
2. Michael Steffes, "RLC Filter Design for ADC Interface Applications," Application Report	sbaa108
3. Xavier Ramus, "PCB Layout for Low Distortion High-Speed ADC Drivers," Application Report	sbaa113

Related Web sites

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Figure 16. Single-supply implementation with bandpass filtering

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