

Photo courtesy Johanson Dielectrics Inc.

X2Y[®] FPGA SerDes Bypass

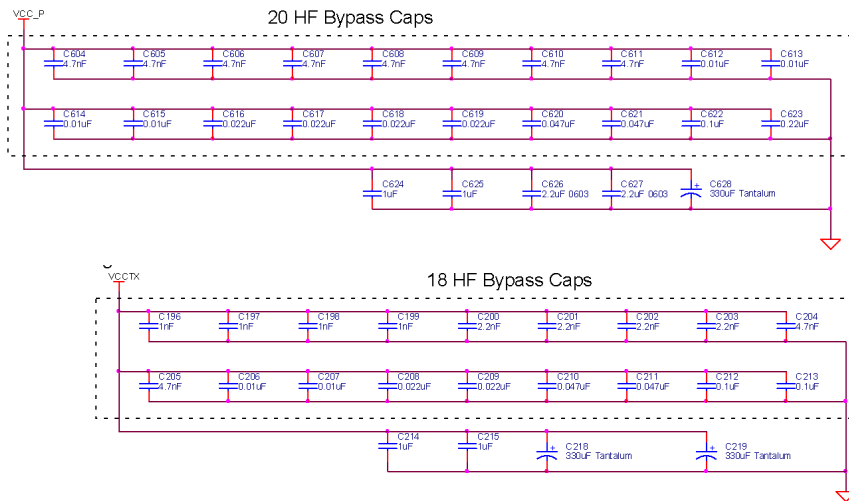
Simplified design and improved performance using X2Y[®] capacitors w/ Altera StratixII GX SerDes

Steve Weir, Consultant with Teraspeed[®] Consulting Group LLC and X2Y Attenuators, LLC, has more than 20 years of experience in the Electronics Industry, holds 17 U.S. patents and has architected a number of packet and TDM switching products. Steve has participated as a TecPanelist at several DesignCon Symposia and authored numerous technical papers on the subject of bypass capacitor application for PDN design. Steve is a frequent contributor to the Si-List message reflector, dedicated to signal and power integrity.

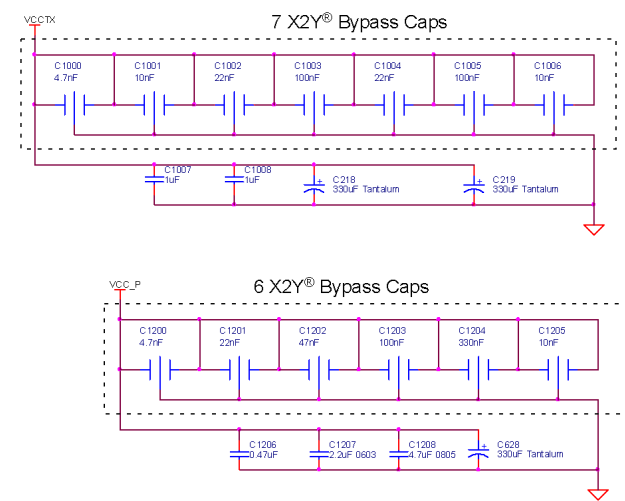
X2Y[®] vs. MLCC

- SERDES transmit power supplies: 13 X2Y[®] capacitors replace 38 0402 caps
 - X2Y bypass network engineered to match MLCC network impedance
- Plane inductance saturation for each supply is achieved w/ 2 X2Y[®] capacitors

MLCC Design

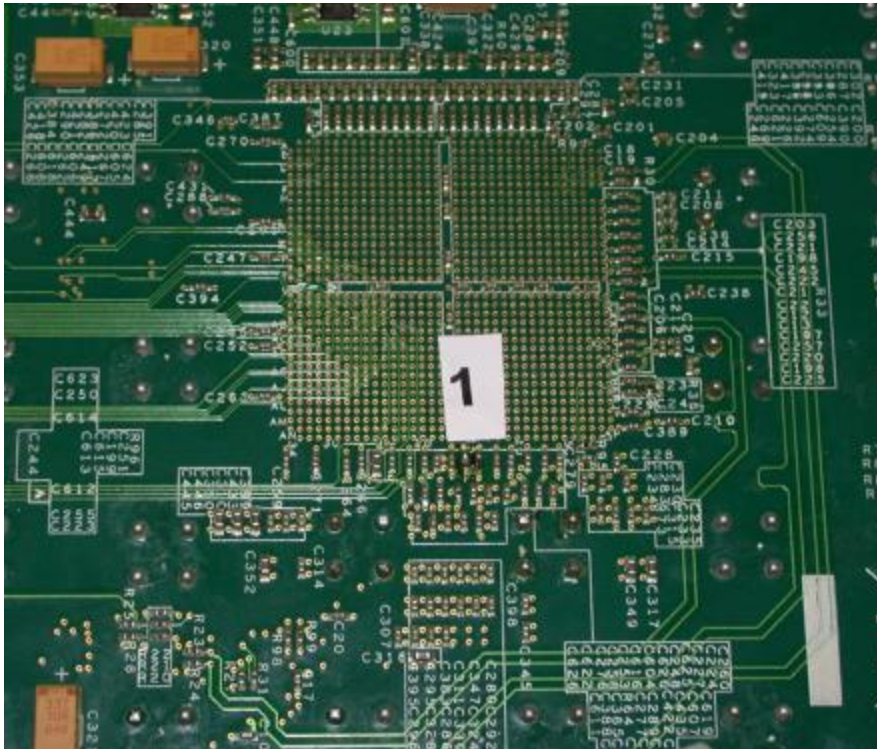


X2Y[®] Design

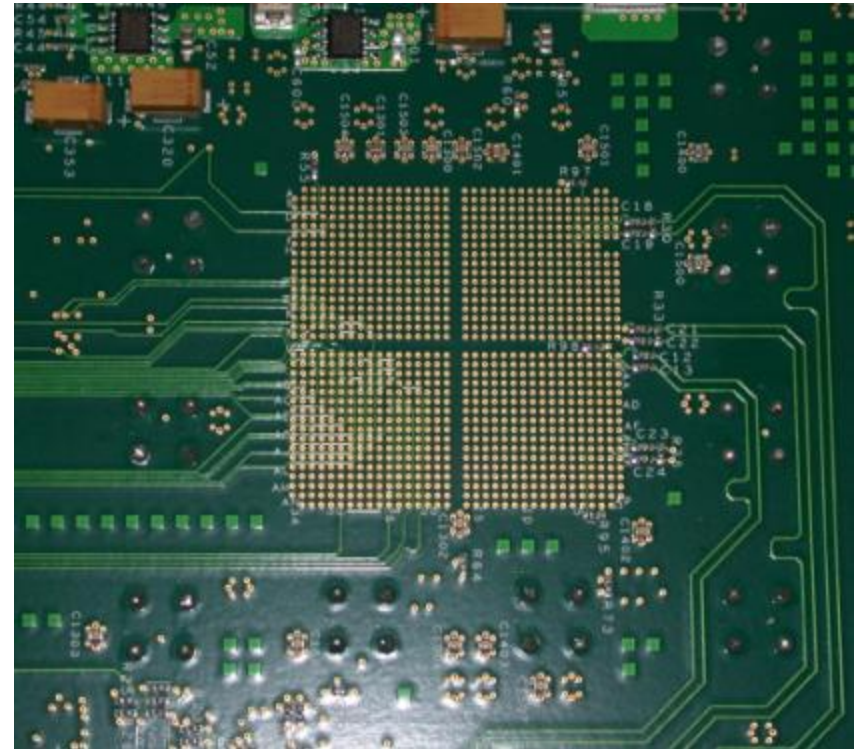


X2Y[®] vs. MLCC

MLCC Design



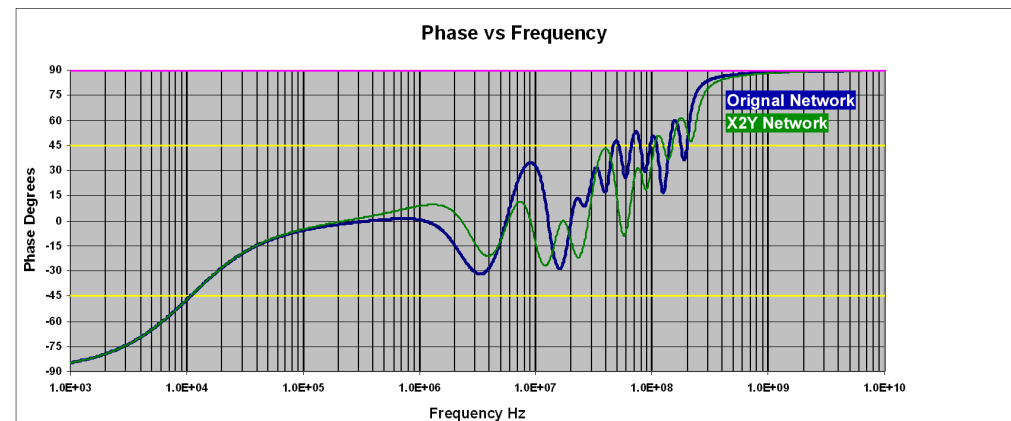
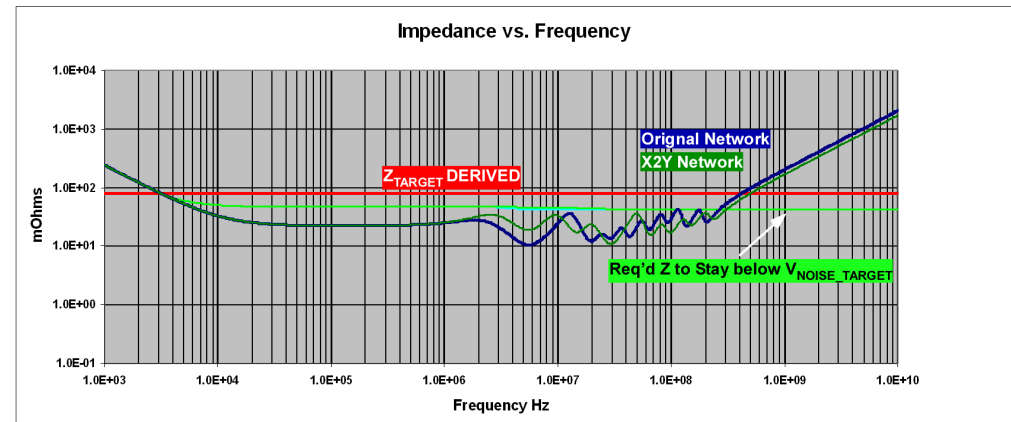
X2Y[®] Design



Transmit Analog: VCCH

■ X2Y[®] Design

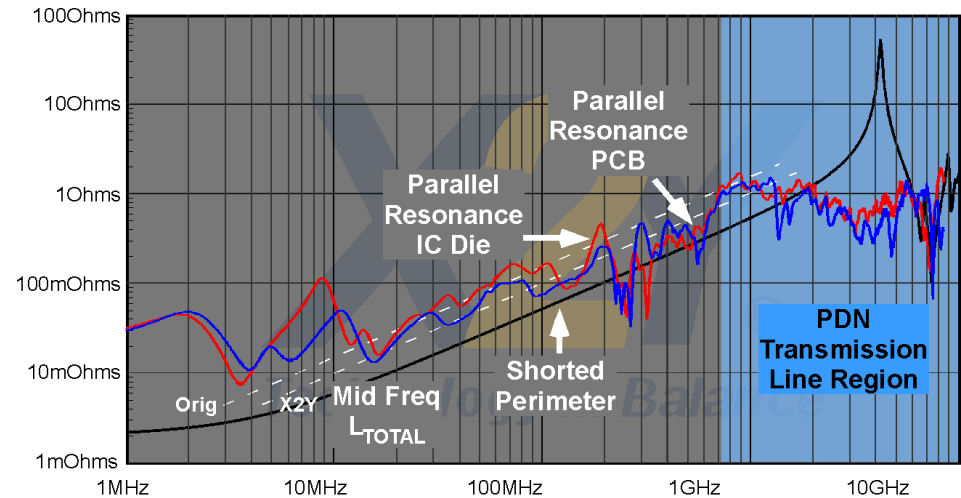
- 2 x 330uF tantalum caps + 2 MLCCs + 7 X2Y[®]
- 1D < 80mOhms equivalent resistive to 250MHz
 - ✓ Ignores spatial effects and IC parasitics
 - ✓ Spatial effects dominate above 10MHz



Original VCCTX and X2Y[®] Networks

- Original network, FDTIM
 - L_{BYPASS} decreases with increasing freq.
 - Near 20MHz about L_{TOTAL} about 220pH
 - Die / bypass PRF near 200MHz
 - Bypass / PCB PRF near
- X2Y[®] network selective zeroes
 - Lower L_{BYPASS} @ 20MHz up
 - Zero for Die / bypass PRF
 - Zero for PCB / bypass PRF

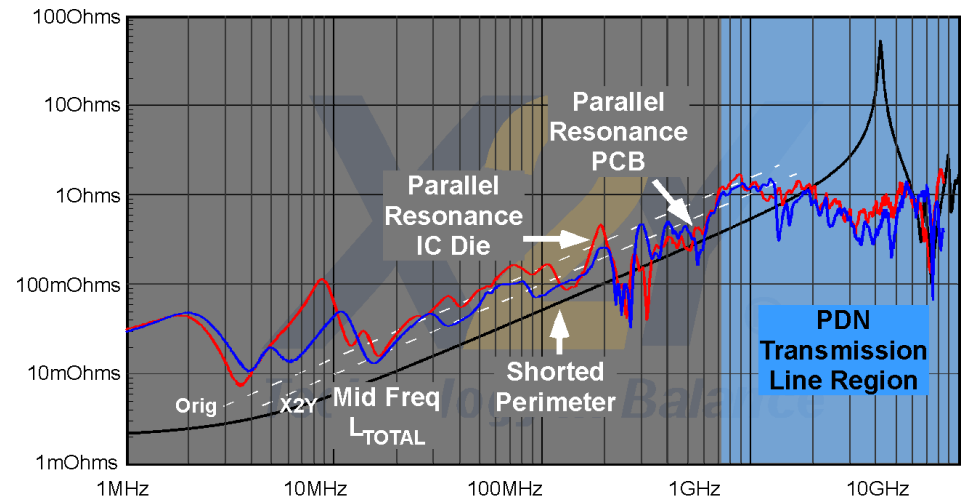
Measured VCCTX Networks vs Simulated Shorted Perimeter



VCCTX PCB / Bypass Resonance

- Original network
 - @ relatively low PRF
- X2Y[®] Network
 - Lower distributed L of 6/7 X2Y[®] caps raises to 580MHz
 - Suppressed w/ single 100pF rated X2Y[®]
 - ✓ Good suppression w/ conventional caps difficult due to high Q
 - Measured results, PRF completely suppressed

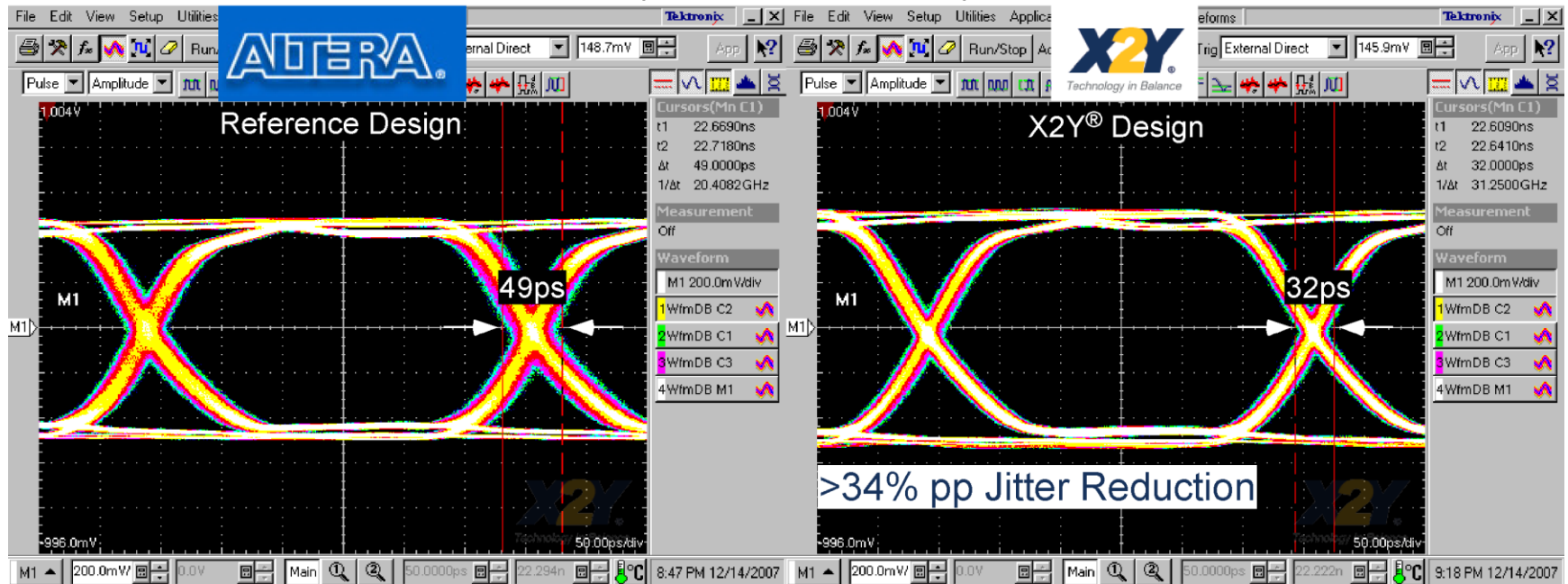
Measured VCCTX Networks vs Simulated Shorted Perimeter



3.125Gbps Performance PRBS7

- X2Y[®] Reduces jitter to 32ps p-p jitter
 - vs 49ps in reference design

3.125Gbps PRBS7, 1 Minute Captures

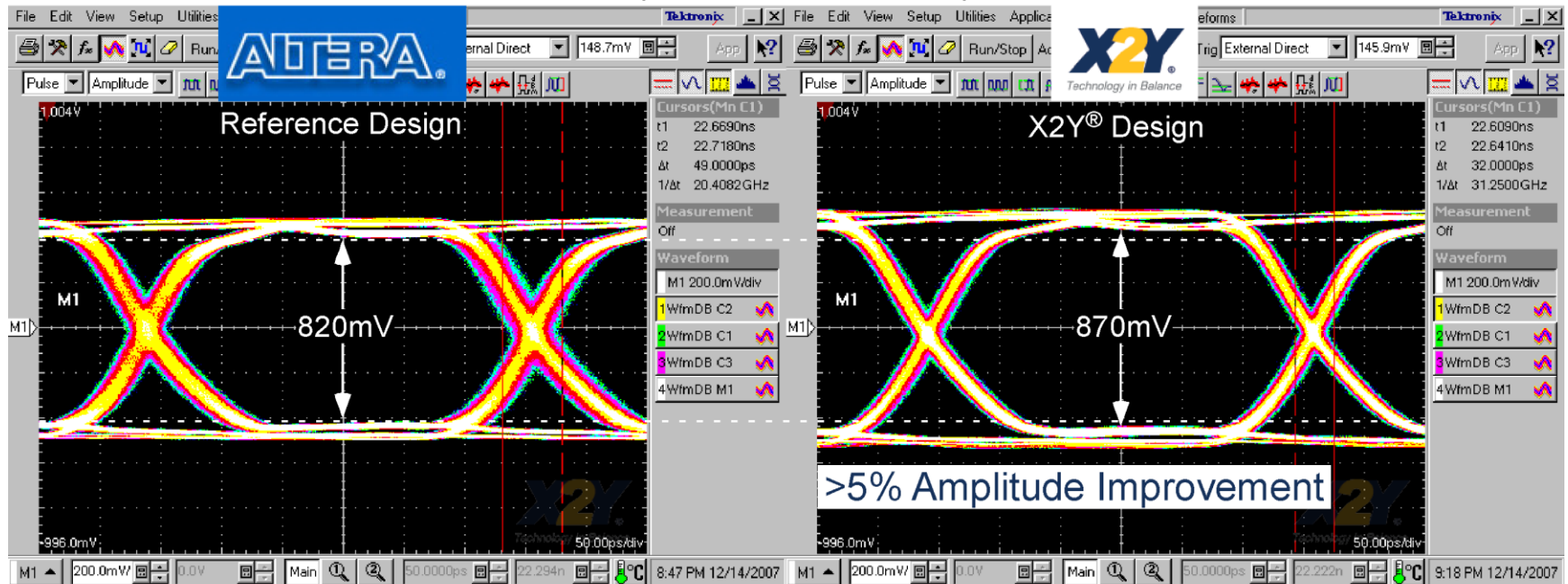


Trigger Source: 156.25MHz Reference Clock

3.125Gbps Performance PRBS7

- X2Y[®] improves better eye amplitude >5%
 - 870mV pp @ sample point vs 820mV pp reference

3.125Gbps PRBS7, 1 Minute Captures

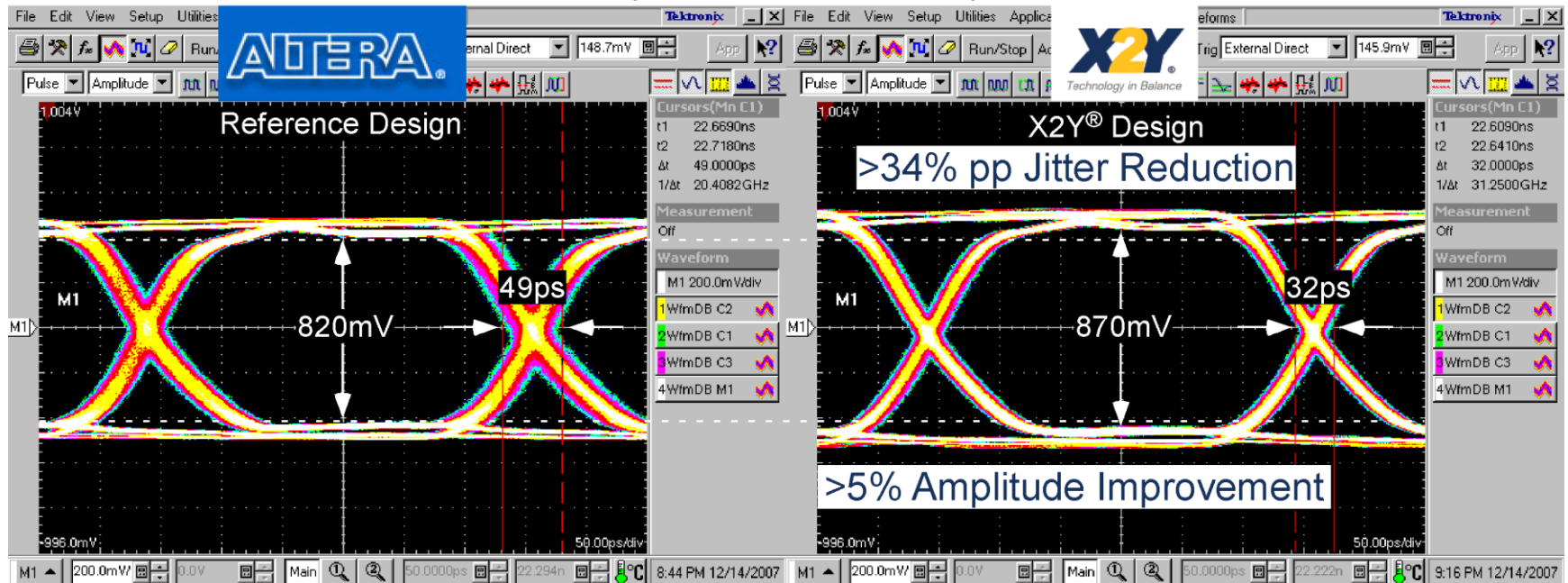


Trigger Source: 156.25MHz Reference Clock

3.125Gbps Performance PRBS23

- Shows same improvements in jitter and eye amplitude:
 - X2Y[®] 32ps p-p jitter vs 49ps in reference design
 - X2Y[®] 870mV pp vs 820mV pp in reference design

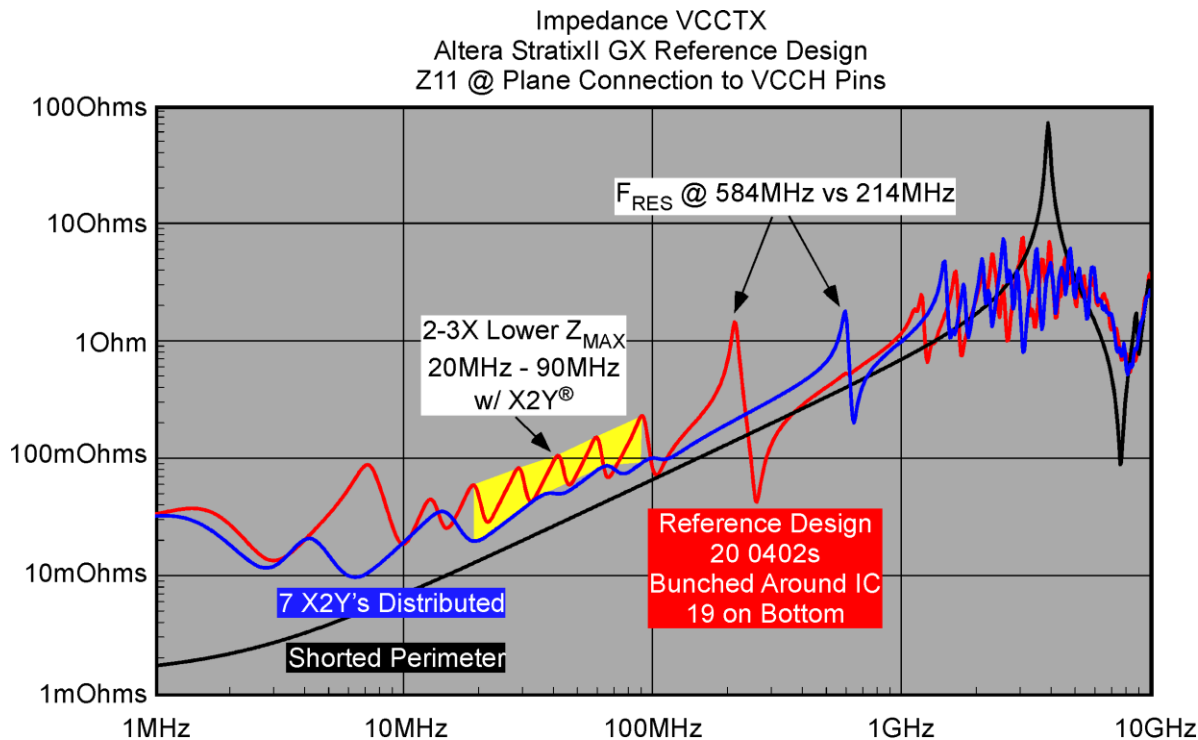
3.125Gbps PRBS23, 1 Minute Captures



Trigger Source: 156.25MHz Reference Clock

Impedance Comparisons w/o IC

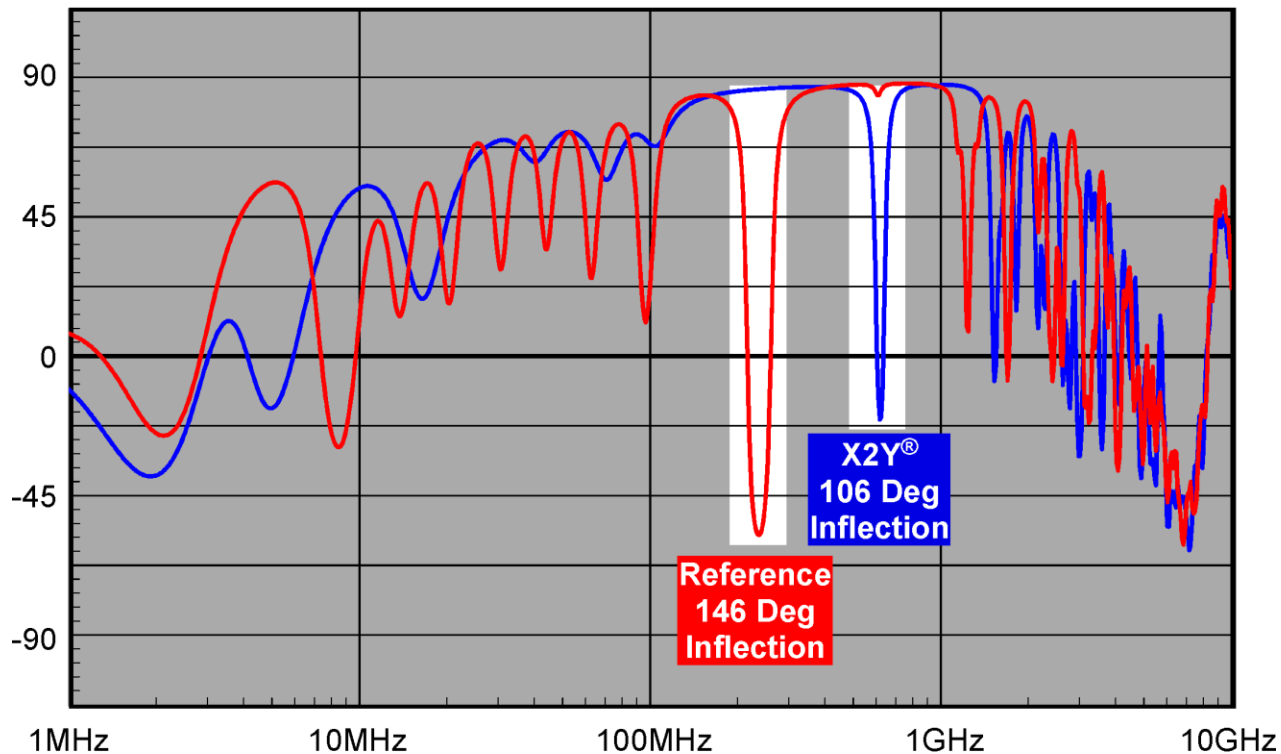
- X2Y provides the following benefits:
 - 2-3X lower impedance 20MHz-100MHz w/ 7 X2Y[®] capacitors instead of 20 ordinary capacitors
 - >2.5:1 Higher F_{RES}
 - 2.5:1 reduction in Q



Impedance Comparisons w/o IC

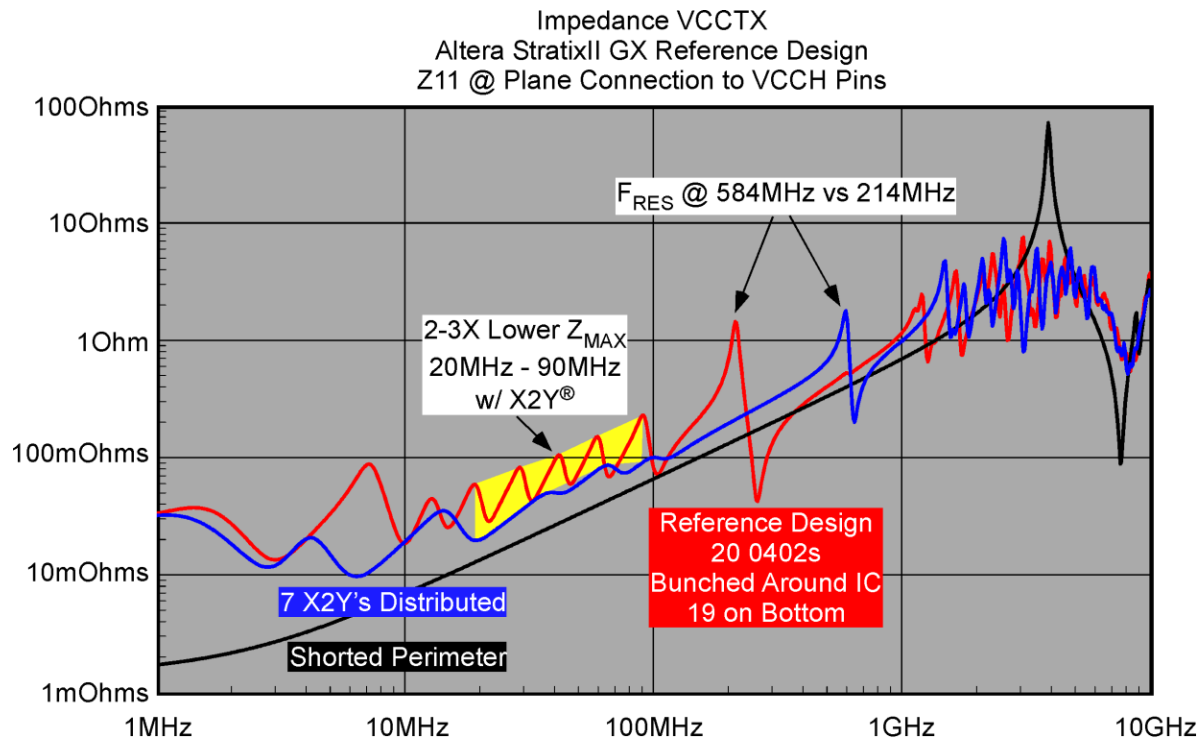
- Phase inflection @ resonance much smaller, and narrower w/ X2Y[®] solution.

Z11 Phase Comparison
Altera StratixII GX Reference Design
Reference vs. X2Y[®]



Impedance Comparisons w/o IC

- Radically lower mounted L / cap w/ X2Y[®] top-side solution flattens impedance modulation.
 - Remains much closer to limit of shorted planes
- Higher F_{RES} w/lower Q stabilizes power system much faster after each transient.



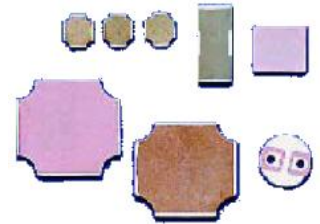
Summary

- Using 13-X2Y capacitors to replace 38 ordinary MLCCs in the SERDES transmit power supplies resulted in:
 - Significant improvements in jitter and eye amplitude
 - ✓ Component reduction
 - ✓ Less board space used
 - ✓ Placement cost reduction
 - ✓ More room for trace routes
 - ✓ Improved reliability through fewer components

MLCC Manufacturers



Through-hole and Planar Manufacturers



Distribution

