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PCB Power Delivery Optimizations for the Cost Driven Era

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Abstract

PCB level power delivery involves choices in: PCB laminates, construction, bypass capacitor selection, and placement. We examine currently available choices as they apply to realizing high performance power delivery while optimizing manufactured cost. We demonstrate results using test vehicles built with current generation ICs.

Author(s) Biography

Steve Weir, Member Technical Staff, Teraspeed Consulting Group LLC - Steve is an independent consultant with over 20 years plus industry experience with a broad range of expertise. Steve holds numerous patents, has authored more than a dozen papers on power integrity, and contributes regularly to the SI-LIST signal intgrity reflector.

Tom Dagostino, VP Device Modeling Group of Teraspeed Consulting Group LLC - Tom has over 30 years of design, management, modeling, and market research experience. Mr. Dagostino was a key contributor to the early digital storage oscilloscope design at Tektronix and acquired 10 patents on DSO related technologies at that time. Besides program management and design responsibilities on DSO products, Mr. Dagostino worked with customers and marketing to understand the market's needs and define the products. Mr. Dagostino managed the Mentor Graphics Modeling Group before joining Teraspeed Consulting Group in 2002.

Summary
PCB level power delivery involves choices in: PCB laminates, construction, bypass capacitor selection, and placement. As industry growth occurs more and more in consumer oriented products, effective power distribution must not only perform to ever higher levels, it must do so in the most cost effective manner possible. A clear understanding of the roles and limitations each design choice impacts enables realization of optimal performance at the lowest possible manufactured cost.

The Power Delivery Task
We can break PCB power delivery down into five goals:

- Support DC current requirements of each IC
- Support AC current requirements of each IC
- Sufficiently suppress AC noise between separate IC power nodes and ICs
- Support I/O return path impedance requirements
- Meet emissions and susceptibility requirements

DC current distribution is generally a relatively straightforward task that requires providing sufficient interconnect metal between the VRM and any load to limit DC drop within acceptable limits. Judicious choice of voltage sense location, and/or use of techniques such as adaptive voltage positioning can afford maximum margin to DC and low frequency AC requirements. In this paper we are primarily concerned with distribution issues as they relate to the physical interconnect and medium to high frequency bypass.

The remaining four goals involve trade-offs in PCB construction and layout, as well as bypass network implementation. The primary detractors from PDN performance are:

- PDN series inductances
- PDN circuit resonances
- PDN modal resonances

PDN series inductance as seen by any given IC depends on:

- IC power / ground pin assignments
- PCB power / ground layer assignments
- PCB laminate choices
- Bypass capacitor type, quantity, and location

PDN circuit resonances result from interaction of low-loss inductances with low-loss capacitances. The most troublesome are usually the bypass network inductance to IC die capacitance, and bypass network inductance to PCB cavity resonances.

PDN modal resonances vary depending on:

- Power cavity laminate materials

- Power cavity physical layout
- IC location

The PDN design engineer usually has little control over either IC pin-out or general location on a PCB, as these are usually dictated in advance by the IC manufacturer, and packaging demands of the end product. What the PDN engineer is left with is:

- PCB stack-up
- PCB laminate selection
- Bypass capacitor selection
- Bypass network design

Where changing market focus towards consumer oriented product exerts ever increasing pressure on cost, it is critical to understand the cost and performance trade-offs available PCB laminate and bypass network design choices make on actual manufactured cost. Properly applied, alternate choices in capacitors and laminates afford designs with substantially fewer components. Our emphasis is to illustrate effective estimation techniques to compare optimal near optimal design alternatives early in the design process.

Defining the Metrics

In many ways PDN design remains an ad-hoc process. Several tools have recently entered the market to enable more systematic, numerically based approaches. These include tools from Sigrity, Ansoft, and Mentor Graphics. Other vendors are expected to enter the market shortly. With the exception of Sigrity's Optimize PI product, the current generation tools evaluate a design after the fact. While this is useful for validation, it is not that helpful when developing design strategy.

In order to address this gap we present reliable estimating for the PDN circuit network and power cavity performance. These methods complement any of the tool sets in current use.

Understanding Power Plane / Cavity Behavior

Power cavities exhibit two distinct behaviors:

- Distributed
- Localized

Each behaves differently with respect to bypass capacitor networks and IC loads.

At frequencies well below transmission line modes, a power cavity acts like a very low resistance, low inductance interconnect with some parasitic capacitance. As far as an individual IC is concerned this view breaks down at relatively low frequencies.

For any load looking out into a power cavity, the power cavity interconnect out to a fixed perimeter may be reduced to an equivalent series R-L circuit. Planar inductance and resistance exhibit identical geometric dependencies.

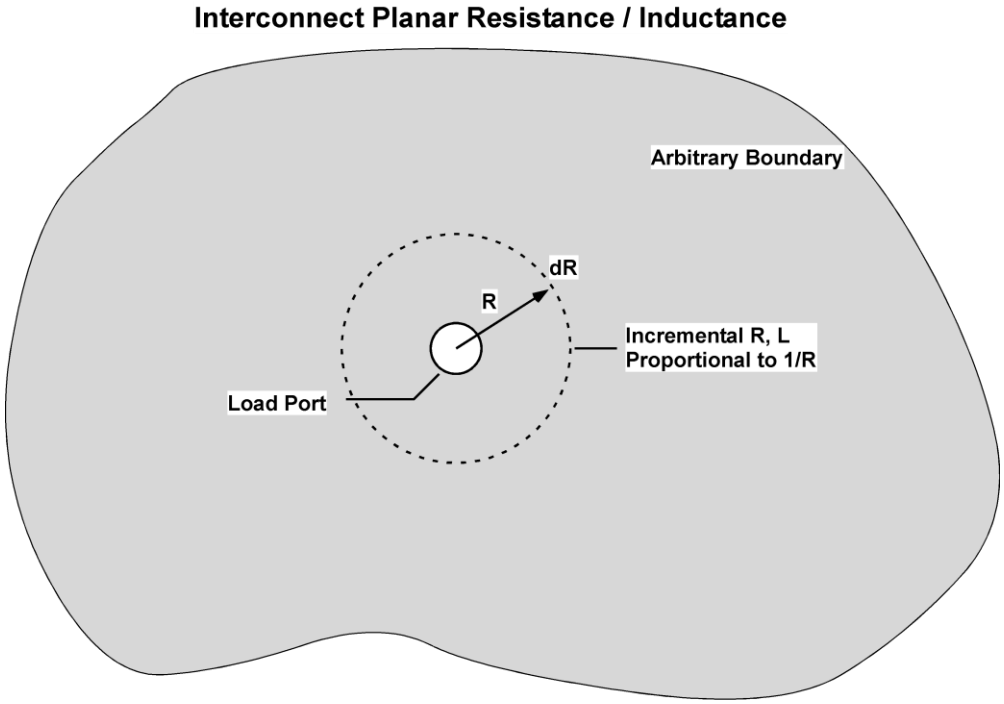

Figure 1

Resistance and inductance from a planar load power port to a surrounding boundary each integrate over the incremental path length outward from the load. The resistance and inductance through each incremental radius, dR is inversely proportional to the conducting perimeter length at each point along the path. As such the L/R ratio, and therefore for any planar interconnect phase versus frequency between a load and an arbitrary perimeter is independent of the planar etch pattern. The L/R ratio instead varies by:

- Conductor bulk resistance,
- Skin effect,
- Conductor relative permeability, 1.0 for copper
- Cavity dielectric height

Figure 2 shows comparative plane impedance for a square power pin pattern out to a perimeter twice the pin pattern width. The figure shows impedance for 48, 4, and 1 mil cavities in both 1oz and 2oz copper clad. Figure 2 also illustrates phase. Altering the planar geometry scales the interconnect impedance magnitude but has no impact on interconnect phase.

Heavier copper weights reduce bulk resistance and shifts the interconnect L/R corner frequency down commensurately. What may be surprising is the weak influence of skin effect on cavity series impedance. Where skin effect is dominant, series impedance for different copper weights converges. Figure 2 illustrates that in thick cavities such as 48mils, cavity inductance strongly dominates over skin effect. The L/R corner for a 48 mil cavity interconnect in 2oz copper is 73kHz, versus 138kHz in 1oz copper, a 1.89:1 frequency ratio. This amounts to 95% of the ratio that would result with no skin effect at all.

Planar interconnects with dielectric heights of 2mils or more all appear inductive above 6MHz. Table 1 summarizes planar interconnect L/R transition frequencies for common dielectric heights using 2oz and 1oz copper. This for most frequencies where the bypass capacitor network operates, planar interconnect appears inductive to a given load, even though the plane overall appears capacitive to the bypass capacitor network.

Cavity Impedance
Square Perimeter / Source 2:1
Zero Perforation, 1oz / 2oz Cu

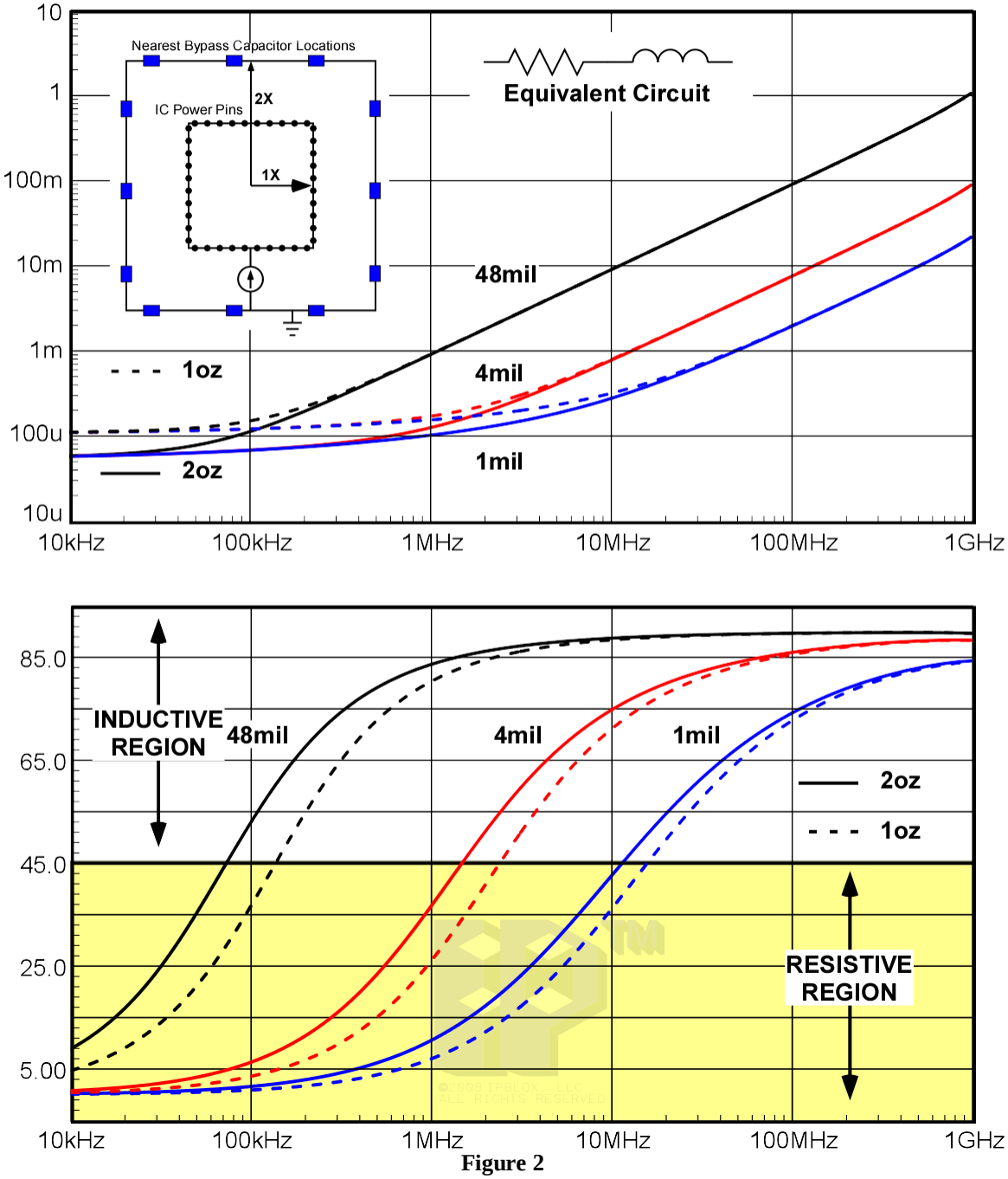

Figure 2

Cavity Height	L/R Transition Frequency 2oz Cu	1oz Cu	Ratio
1200um	73kHz	138kHz	1.89:1
100um	1.5MHz	2.4MHz	1.61:1
50um	4.0 MHz	5.9MHz	1.48:1
25um	11.4MHz	15.8MHz	1.39:1
8um	76.0MHz	91.4MHz	1.20:1

Table 1, L/R Transition Frequencies

Interconnect impedance provides the basis for solving the PDN for each major IC separately. A simplified model of the PDN including spatial effects:

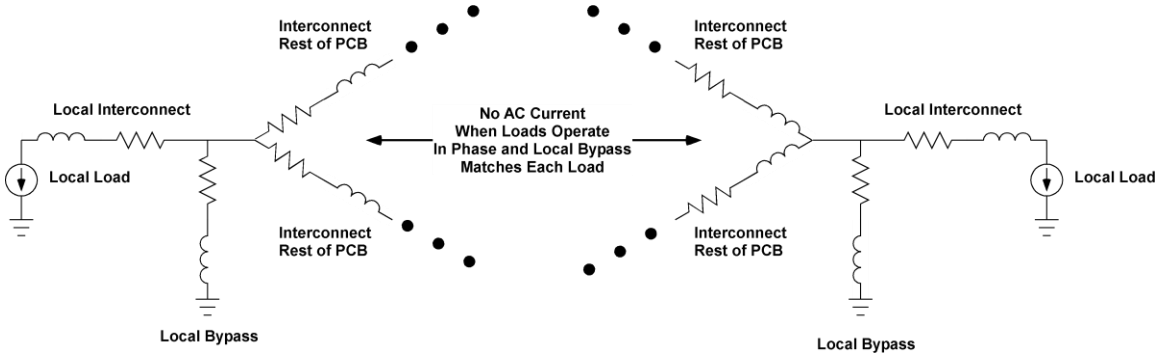

Figure 3

Where each load is allowed to disturb the PDN by a like voltage, and where the worst case load currents are presumed to all operate in phase, PDN HF current circulates only through the local bypass network.

Estimating PDN Bypass Capacitor Requirements

The PDN functions to isolate the noise disturbance of each load from the others on the same rail. A PDN may isolate individual loads with series decoupling, or by sufficiently low shunt bypass. At frequencies above the high audio range, practical PDNs do a mixture of both.

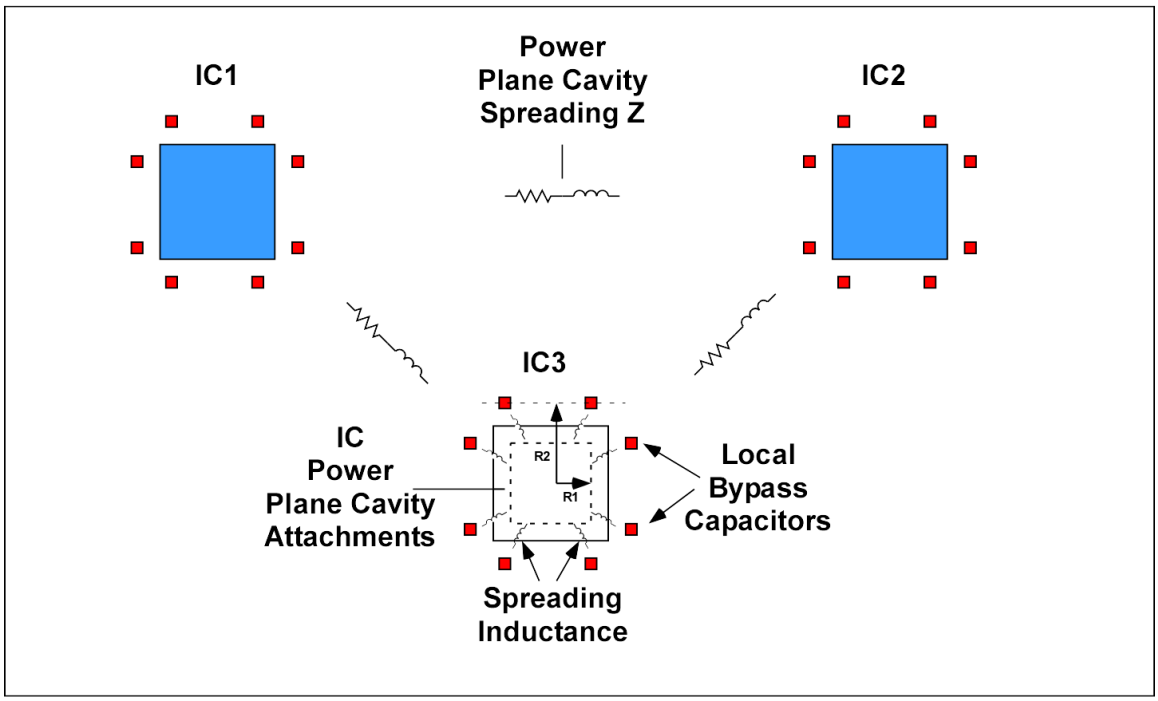

Figure 4, PDN as a Collection of Isolated Distribution Islands

A conservative estimate of bypass requirements considers each IC in total isolation. Power cavity spreading Z between ICs as shown in Figure 4 becomes infinite. Premised on this model, intial bypass requirements are established for each IC giving due consideration to:

1. PDN impedance versus frequency requirements at the IC die.
2. On die bypass
3. Package interconnect parasitics
4. Any package substrate bypass
5. Z axis parasitics from the IC attachment plane to the power cavity
6. Interconnect impedance from the IC plane cavity attachment to the nearest bypass capacitors
7. Attached impedance of each value of bypass capacitor anticipated

For purposes of evaluating alternate PCB stack-ups and bypass networks, we first reduce items 1-4 to a required impedance profile looking the IC sees looking out from power attachments at the IC mounting surface on the PCB. Given that for all but very thin dielectrics, the interconntect is inductively limited, we translate the impedance requirement at the highest frequency, noise current product to an equivalent inductance.

Equation 1

$$L_{MAX\_IC\_SURFACE\_THRU\_CAPS} = \Delta V_{PP}/(2*\Delta I*jw_{MAX})$$

This inductance consists of three pieces:

- Z axis inductance from IC mounting surface to the power cavity attachments
- Spreading inductance from the IC power cavity attachments to the nearest bypass capacitors
- Attached inductance of the nearest bypass capacitors.

Two and Four Routing Layer Construction Options

Low cost / low layer count PCBs make for difficult trade-offs between signal and power integrity optimization. In order to achieve trace impedances near 50 Ohms, the outer dielectric height must be close to the trace widths used. For a 0.062" thick four layer PCB the power cavity is often 50 mils thick or more. Spreading inductance looking out from an IC pin array is:

Equation 2

$$L_{SPREAD} \approx 5.1pH * H_{CAVITY} * \ln(R2 / R1) * A_{CONTIGUOUS}/A_{PERFORATED}$$

For a rectangular package Equation 2 holds for R2 >> R1. For R2 < 4 R1 the value decreases somewhat:

Equation 3

$$L_{SPREAD} \approx 4pH * H_{CAVITY} * \ln(R2 / R1) * A_{CONTIGUOUS}/A_{PERFORATED}$$

Z axis inductance for each attached via pairs is approximately:

Equation 4

$$10.2pH * H_{VIA} * \ln(2*S/D)$$

In an 0.062" thick PCB using 10mil drills and vias on 1mm centers, this translates to 21pH / mil, 1300pH / via pair.

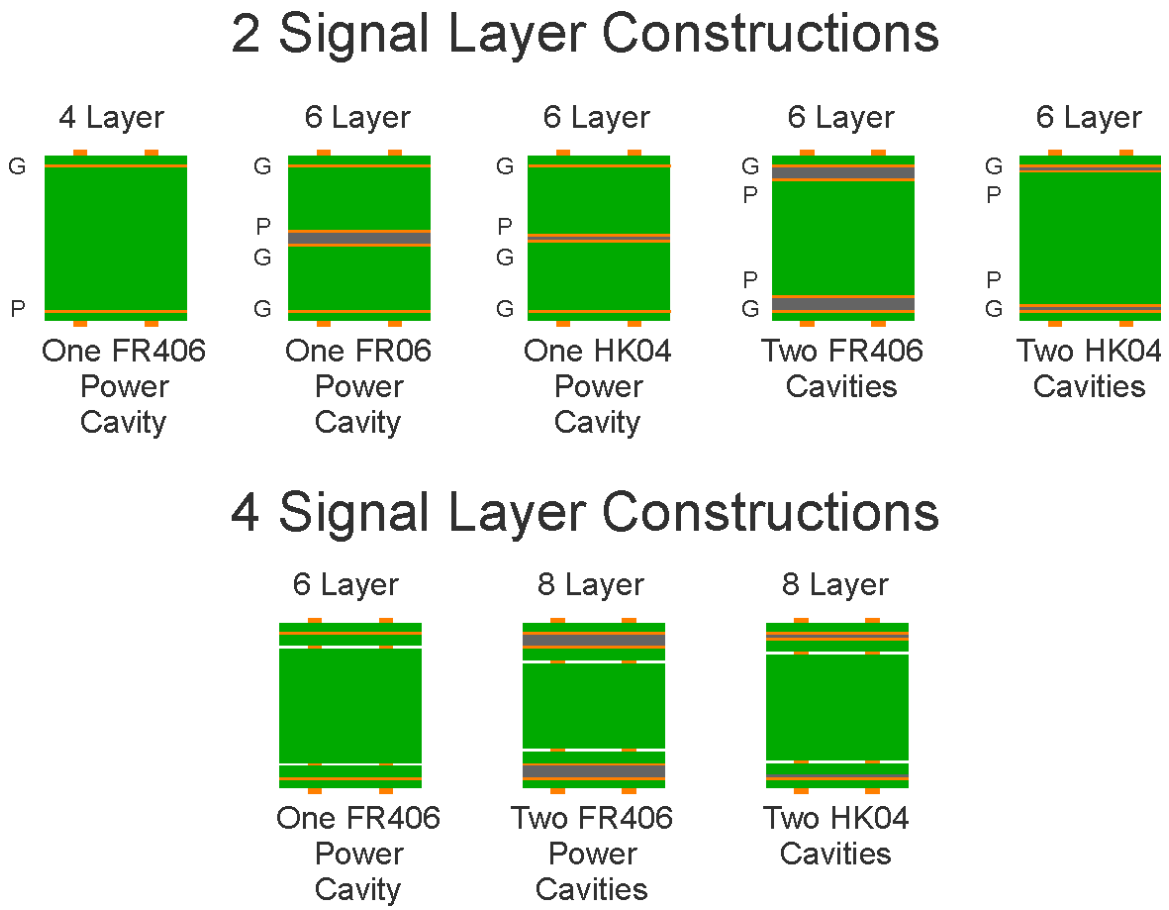

Figure 5, 2 / 4 Signal Routing Layer Stack-ups

At 50mil H_{CAVITY}, 35% perforation, and R2 = 2*R1spreading inductances approaches 300pH, 100mOhms at 50MHz. An arbitrary bypass network cannot reduce the impedance profile below this point. The only alternative that remains in four layers is where the IC power / ground pin pattern lends itself to back side mounting of bypass capacitors. Because the power cavity is so thick, relatively few well mounted backside capacitors outperform an arbitrary number of top side capacitors. The performance limit for this construction is determined by the number of backside capacitors the IC power / ground pattern supports, and whether additional capacitors are located around the IC periphery.

Equation 5

$$L_{LOCAL\_PDN} \approx (21pH/mil*T_{PCB}/N_{IC\_VIAPAIRS} + L_{CMOUNT\_UNDER}/N_{UNDER}) \parallel (H_{CAVITY}* \ln(R2 / R1)*A_{CONTIGUOUS}/A_{PERFORATED} + L_{CMOUNT\_PERIPHERAL}/N_{PERIPHERAL})$$

Where:

L_{LOCAL_PDN}	Inductance from IC attach point at the top of the PCB
T_{PCB}	PCB thickness in mils
$N_{IC\_VIAPAIRS}$	# of IC power / ground pairs on 1mm centers
L_{CMOUNT_UNDER}	Mounted inductance of each capacitor under the part
N_{UNDER}	# of capacitors mounted under the part

$L_{CMOUNT\_PERIPHERAL}$ Mounted inductance of each capacitor mounted peripheral to IC
$N_{PERIPHERAL}$ # of capacitors mounted peripheral to the IC

Where the PCB board thickness is fixed, the bypass capacitors and their mounting standardized, and the peripheral bypass capacitor mounted inductance set to match the cavity spreading inductance, Equation 5 can be approximated as:

$$L_{LOCAL\_PDN} \approx K3*(K1*/ N_{IC\_VIAPAIRS} + K2/ N_{UNDER}) / (K1*/ N_{IC\_VIAPAIRS} + K2/ N_{UNDER} + K3)$$

For the 4 layer case $N_{IC\_VIAPAIRS} >> 6$

$$L_{LOCAL\_PDN} \approx (K1*/ N_{IC\_VIAPAIRS} + K2/ N_{UNDER})$$

The situation can be greatly improved by increasing layer count from four to six layers. Three construction alternatives all retain two routing layers:

- Center cavity 3, or 4 mils glass / resin.
- Center cavity 24um, epoxy fill, or polyimide.
- Two outer cavities, 3 or 4 mils glass / resin
- Two outer cavities 24um, epoxy fill, or polyimide

The center cavity constructions yield one power cavity as before, while the outer cavity constructions yield two power cavities each. All four constructions are readily arranged such that signals all reference ground. This eliminates I/O return current injection in the PDN, a particular point of concern for passing EMC compliance without extensive enclosure shielding.

The center cavity constructions with 4mil or 1 mil dielectric greatly reduce spreading inductance making it possible to add more capacitors for lower total PDN impedance than is possible with capacitors only on the bottom side. However, the two outer cavity 4 mil construction has the same cost without the Z axis inductance penalty.

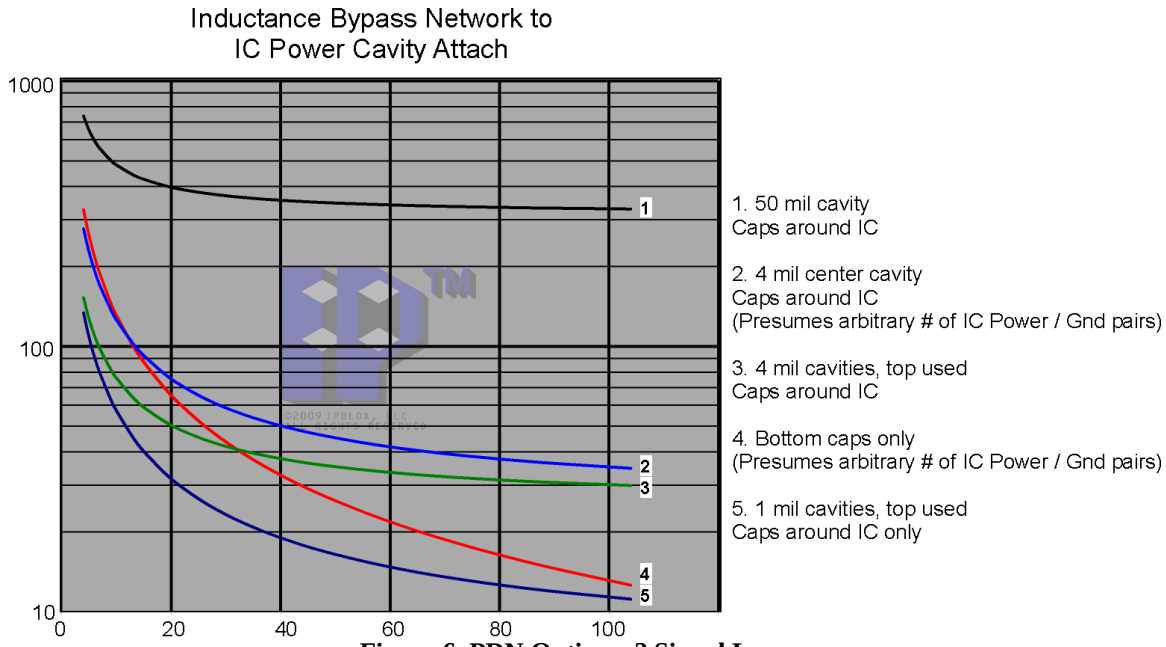

Figure 6, PDN Options, 2 Signal Layers

For bypass capacitors mounted around the IC and any given cavity thickness, the combined interconnect and bypass capacitor inductance quickly saturates for capacitor counts beyond:

$$COUNT_{CAPACITOR\_SATURATE} = L_{INTERCONNECT} / L_{CAP\_MOUNTED}$$

	0402	X2Y	L_{SAT}
4 layer, 50 mil center	6	2	625pH
6 layer, 4 mil center	41	11	50pH
6 layer, 4 mil top	21	6	50pH
6 layer, 1 mil top	81	24	13pH

Figure 7, Inductance Saturation Capacitor Counts , Typical

A given cavity exhibits the best relative capacitor count advantage over a thicker cavity between saturation of the respective cavities. Bottom mount capacitor configurations do not saturate per-se. The bottom mount configuration requires the same or fewer capacitors from about 1.5X the saturation count for a given cavity configuration. For an 0.062" thick PCB, at saturation, a top cavity configuration saves 33% capacitor count versus bottom mount.

For example: On an 0.062" thick PCB to hit a 100pH target inductance, requires 7 capacitors attached to a top mount 4 mil cavity, 5 capacitors attached to a 1 mil top cavity or 13 capacitors attached to the PCB bottom. The 4mil cavity removes 46% capacitor count, while the 1 mil removes 62%.

The required capacitor counts for common board constructions are readily tabulated:

Target Inductance	0402				X2Y	
	4/6 lyr	6/8 lyr			6/8 lyr	
	Bottom	4 mil top	1 mil top		4 mil top	1 mil top
30pH	61	102	21		30	6
40pH	46	34	15		10	4
50pH	37	20	12		6	3
60pH	31	15	9		4	3
70pH	26	11	8		3	2
80pH	23	9	7		3	2
90pH	21	8	6		2	2
100pH	19	7	5		2	2
120pH	16	5	4		2	1
140pH	13	4	4		1	1
160pH	12	4	3		1	1
180pH	11	3	3		1	1
200pH	10	3	3		1	1
220pH	9	3	2		1	1
240pH	8	2	2		1	1
260pH	7	2	2		1	1

Table 2, Bypass Capacitor Counts vs Inductance to IC Attach 0.062 Thick PCB

The PCB construction cost difference depends primarily on PCB area and materials used. Evaluating break-even on materials can be procedurealized as:

1. For each significant IC in the design, determine the target inductance at the IC plane cavity attachment.
2. Look-up the number of capacitors required from Table 2 for each construction option.
3. Add to the running total capacitor count.
4. Determine PCB incremental cost:
    a. 4/6 layer
    b. 6 layer 4 mil dielectric-
    c. 6 layer 1 mil dielectric-
5. For each column in Table 2 determine the assembled bypass network cost
    a. Multiply the capacitor count by the sum of purchase, and assembly costs.
6. Add values from steps 4 and 5.
7. Select the lowest resulting cost.

Over a wide range of common inductances, the combination of 1mil dielectric and X2Y™ capacitors results in a 10:1 component reduction.
Example: 4” x 8” PCB, two routing layers, $2.00/sq ft FR406 / layer pair, $5.00 / sq ft HK04, $0.001 / cap 0402, $0.03 / cap X2Y™, $0.015 assembly cost / cap all. 10 ICs 70pH each.

Costs	0402				X2Y	
	4 lyr	6 lyr			6 lyr	
	Bottom	4 mil top	1 mil top		4 mil top	1 mil top
PCB	$0.89	$1.33	$2.66		$1.33	$2.66
Capacitors req'd	260	110	80		30	20
Cap. mat'l	$0.26	$1.10	$0.08		$0.90	$0.60
Cap. assy	$3.45	$1.65	$1.20		$0.45	$0.30
Total	$4.57	$4.07	$3.94		$2.68	$3.56

Table 3, Example Two Signal Routing Layer Costs

The more than 2:1 reduction in bypass capacitors afforded by switching to 6 layers from 4 layers more than pays for the additional material. For the assembly costs shown, the difference favors use of 1mil dielectric despite the material premium. Opting for X2Y™ capacitors with 4 mil 6 layer construction drops costs nearly in half and models as the most cost effective solution by far for this scenario. Accurate, raw material and assembly cost numbers are critical to the decision process.

Example: 4" x 8" PCB, four routing layers, $2.00/sq ft FR406 / layer pair, $5.00 / sq ft HK04, $0.001 / cap 0402, $0.03 / cap X2Y™, $0.015 assembly cost / cap all. 12 ICs 50pH each.

Costs	0402				X2Y	
	6 lyr	8 lyr			8 lyr	
	Bottom	4 mil top	1 mil top		4 mil top	1 mil top
PCB	$1.33	$1.78	$3.11		$1.78	$3.11
Capacitors req'd	444	240	144		72	36
Cap. mat'l	$0.45	$0.24	$0.15		$2.16	$1.08
Cap. assy	$6.66	$3.60	$2.16		$1.08	$0.54
Total	$8.44	$5.62	$5.42		$5.02	$4.73

Table 4, Example Four Signal Routing Layer Costs

Transition Between the Bypass Network and Cavity

At the frequency where the impedance magnitude of the parallel inductance of the bypass network matches the distributed capacitance of the power cavity, a resonance forms. When this resonance is within the signal frequency band, as it usually is for current applications, action is required to dampen the resonance. Several methods are available, including often the simplest: mapping one or more mounted capacitor zeros to the resonant frequency. This involves selecting a few capacitor instances to suppress the pole at resonance and has little impact on cost. Any of the commercially available tools such as Sigrity's Optimize PI™ can model and shape the transition.

Transition Between the Bypass Network and ICs

Where ICs include substantial on die, and/or on substrate capacitance, resonances readily form. Where (rarely) the IC manufacturer provides detailed information on the IC power distribution, these resonances can be suppressed early in the PCB design process. Alternatively, a laboratory service such as our Teraspeed Labs may be used to measure the ICs prior to PCB layout. A final alternative is to simply allocate a few capacitor locations distributed around each PDN. These positions will be populated once the PDN is characterized after first board build. Teraspeed can perform this evaluation and supply the compensation capacitor values.

Conclusions

Competitive cost pressure is more severe than ever. A clear understanding of PDN design options is critical towards achieving lowest production costs. In low-cost 4, and 6 layer constructions the PDN appears inductive to any given IC from 70kHz and higher. Reducing dielectric thickness reduces this inductance and affords sometimes massive reductions in bypass capacitor counts.

In many situations, total manufactured cost can be minimized through use of:

- More material – taking a 4 layer PCB to 6 layers with 4 mil upper and lower power cavities
- More expensive raw materials – using 1 mil polyimide (DuPont Interra® HK04), or epoxy (Oak/Mitsui BC24) dielectric in place of 4 mil glass / resin
- Lower inductance capacitors such as X2Y™

On four layer boards, the most likely savings are realized by switching to a six layer construction with conventional dielectric. Depending on the number of ICs and impedance targets, often X2Y™ capacitors will further improve product margins.

On six layer boards with four routing layers, the advantage tends to fall to 1 mil materials near 20mOhm individual IC power targets. The actual transition points depend heavily on delivered component, and assembly costs. In some instances of very low assembly costs, it is possible that assembly cost savings will not be sufficient to justify changing stack-up, dielectric or capacitor types.