X2Y Capacitors for FPGA Decoupling

Summary

X2Y capacitors provide advantages to FPGA decoupling applications unmatched by any other devices in the market.

Introduction

High performance, low-voltage FPGAs demand low impedance power bypass for both core and I/O voltage rails. Mounted inductance of conventional capacitors makes it increasingly difficult to adequately bypass FPGA power, much less do so economically in terms of total space and cost. Due to their super low, raw and mounted inductance, X2Y capacitors are uniquely suited to economical realization of high performance FPGA bypass networks. As we will see, X2Y capacitors enable bypass networks with the fewest parts and fewest vias.

FPGA Decoupling

Today's FPGAs are remarkably powerful and flexible devices. Both aspects place stringent demands on the power delivery system. Modern devices often require power bypassed to well under 50 milliohms as measured at the FPGA.

FPGA high frequency power path:

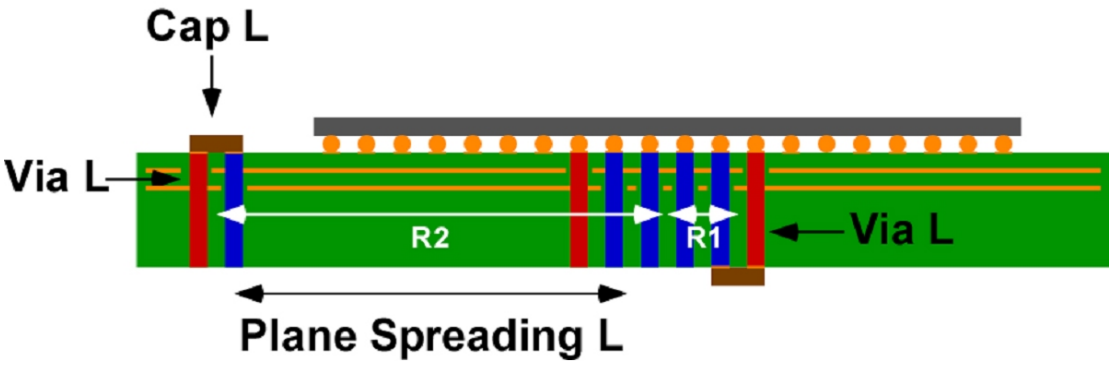


Figure 1. FPGA Power Distribution Components

Modern voltage regulator modules provide sufficiently low impedance at frequencies as high as one or two MHz. The bypass capacitors through their attachment vias, the power/ground planes, and the FPGA power/ground attachment vias provide current from the low MHz up to the cut-off frequency of the FPGA package itself. Above the FPGA package cut-off, capacitance provided within the FPGA package must support device currents.

Figure 2, illustrates a schematic view of the circuit elements:

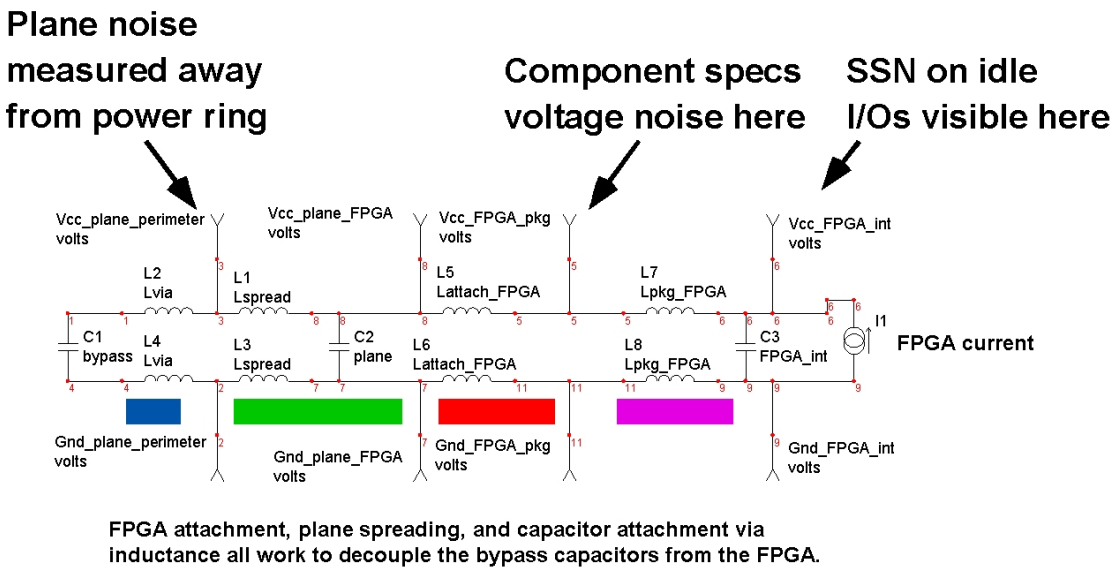


Figure 2. Schematic, FPGA Bypass Path

In the past, bypass emphasis has tended to focus on the bypass capacitors and their attachment vias, (blue section in Figure 2). For relatively high impedance systems where the spreading inductance of the planes (green section), and attachment inductance of the FPGA power ground vias to the PCB power/ground planes (red section) were low compared to the mounted capacitor inductance, this emphasis was well-placed. Further, common wisdom asserted that because via inductance is often significantly greater than inductance of even conventional MLCC capacitors such as 0603, that use of low inductance capacitors provides little benefit. The running practice has been to just add ever-increasing numbers of conventional device. Along these lines, one popular FPGA application note recommends one capacitor per FPGA power pin.

In reality these generalizations only hold for special cases that are becoming increasingly uncommon. As we will see that X2Y capacitors not only dramatically reduce component count in all cases, but in most cases they also reduce via count and corresponding routing congestion as well.

The Importance of Inductance

Inductance is the critical measure of bypass impedance. At frequencies above the bypass capacitor SRF, the impedance of the network in Figure 2, may be approximated as:

Equation 1

$$|Z| = jw((Lesl\_caps + Lattach\_caps) / N + Lspread + Lattach\_FPGA)$$

If we substitute: Lcaps_mounted = (Lesl_caps + Lattach_caps) / N, this reduces to:

Equation 2

|Z| = jw(Lcaps_mounted+ Lspread + Lattach_FPGA)

For example, assuming an FPGA package cut-off frequency of 50MHz, and a pedestrian |Z| of 50mohms we get:

Lcaps_mounted+ Lspread + Lattach_FPGA <= 50E-3 /(50E6 * 2pi)

or 160pH.

We then need to budget this 160pH among the three elements.

FPGA attachment via inductance has two components: A portion for the via segment that is inside the power / ground plane cavity, and the portion that is between the top of the cavity and the FPGA. The closed form equations derived by Dr. Howard Johnson in “High Speed Signal Propagation”, pp 259:

Equation 3

$Lvia = u_0 / 2pi * ((H_1^2 * (2 – K_1) / (S * K_1)) + 2 * H_2 * ln(2 / K_1))$ where

u0 is the permeability of free space, 31.9nH/square (English)

H1 is the via height above the uppermost plane.

H2 is the via height from the furthest plane to the top of the board.

S is the separation between the power and ground vias, 0.04” for VirtexII™ Vccint

D is the via hole drill diameter.

K_1 is the ratio D/S.

Assuming a stack-up with logic ground on layer 2 0.005” below the surface, and Vccint on layer 5 0.02” from the board surface, we get:

Lvia = 590pH

Xilinx Virtex2™/Pro™ FPGAs have 44 Vccint pads. The total inductance will be twice the inductance for a single via (1X for each Vccint via and ground via) divided by the total number of Vccint vias:

Lattach_FPGA = Lvia * 2/44 = 590/22 = 27pH. For 50mohms @ 50Mhz 27pH is a small fraction of a 160pH budget. However, for a high performance system, requiring 10mohms, or only 32pH total, 27pH would constitute 84% of our entire inductance budget.

Assuming that we have mounted our decoupling capacitors on the surface as depicted in Figure 1, for FPGAs such as Virtex2™/Pro™ where the power connections are almost all concentrated in a central ring, we can then find the inductance by integration across the annular ring from the power/grounds to the decoupling capacitors, and then integrate again across the height of the plane cavity using the Biot-Savart Law. The resulting equation is:

Equation 4

Lspread = u0 / 2pi * H * ln(R2 / R1) where

u0 is the permeability of free space, 31.9nH/square (English)

H is the plane separation height.

R2 is the mean radius from the FPGA center to the decoupling capacitors.

R1 is the mean radius from the FPGA center to the power ground ring at the center of the FPGA.

Plane perforation caused by antipads raises the inductance by the approximate unperforated area divided by the perforated area. For 0.02" diameter antipads on a 0.0393" grid, perforation results in an adjustment factor 1.25.

Assuming a capacitor radius of 1.2", then for the FF896 / FF1152 packages, and plane spacing of 14mils, for a dual offset stripline configuration we get:

Lspread = 5.08E-9 * 14E-3 * ln(1.2"/0.35") * 1.25 = 110pH.

Spreading inductance consumes almost three quarters of even our pedestrian 50mohm @ 50MHz / 160pH budget.

In this example case Lcaps_mounted is left with 160pH – 27pH – 110pH = 23pH, barely 1/8th total inductance budget.

Lcaps_mounted is self inductance of each capacitor, plus its attachment vias divided by the number of capacitors in the bypass array:

For conventional capacitors attached with a single via per pad:

Equation 5

Lcaps_mounted_conv = (2 * Lvia + Lesl_conv) / N

For an X2Y capacitor attached as in Figure 3, we have six vias per capacitor. The relative current through the A and B vias is 1/4th that of each via for the conventional capacitor, while the current through each the G1 and G2 vias is ½ that of the conventional capacitor vias. The resulting inductance is:

Equation 6

Lcaps_mounted_x2y = ((Lvia / 2 + Lvia / 4) + Lesl_x2y) / N

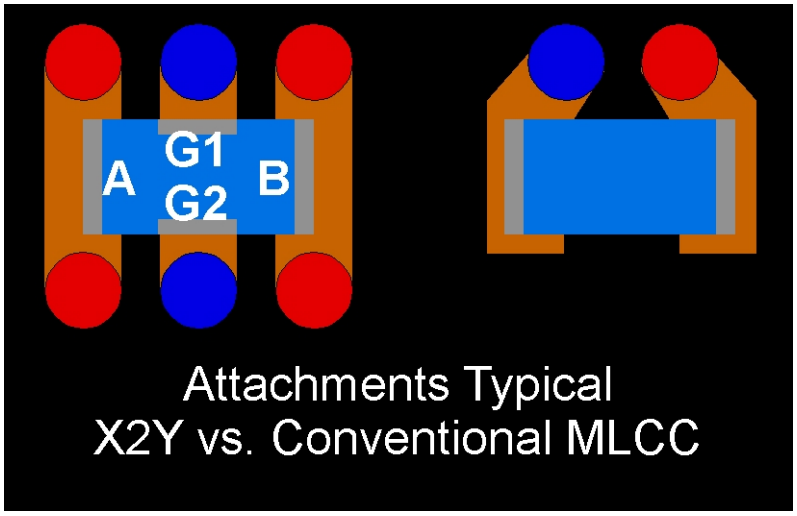


Figure 3. Bypass Capacitor Typical attachments

Given via geometries, the self-inductance of each raw capacitor, and our budget of 23pH we can solve for N in each case. X2Y 0603 capacitors exhibit extremely low self-inductances of just 60pH, (see Measurement and Comparative S21 Performance of Raw and Mounted Decoupling Capacitors).

Example Capacitor Networks

The first row demonstrates performance with a commonly used configuration with 0603 capacitors where the vias are placed on 0.05" centers to facilitate routing grid. The inductance of each via is 374pH, leading to 748pH for two vias and 1248pH for the combined vias and capacitor. 54 such capacitors are required to reach 23pH total. The second example improves matters by pushing the vias closer together, but this will also add offsetting surface trace inductance. The third example both pushes the vias closer together, as well as doubles up on the vias. This example makes the artificially optimistic assumption that mutual coupling does not erode via performance, when in reality, it does. Even with these artificially optimistic assumptions, no arrangement of the 0603 capacitor is even remotely competitive with the X2Y 0603 solution.

	Via								
Cap type	D	S	H_1	H_2	Lsingle	LTot	Lcap	N	Vias
0603 2 via	.01	.05	.005	.015	374	748	500	54	108
0603 2 via	.01	.03	.005	.015	294	588	500	47	94[1]
0603 4 via	.01	.03	.005	.015	294	294	500	35	140[2]
X2Y 0603	**.01**	**.03**	**.005**	**.015**	**294**	**221**	**60**	**12**	**72**

Table 1. Example Networks, 23pH Target

For this pedestrian example, the X2Y solution replaces ordinary 0603s at ratios varying from 3:1 to 4.5:1, and via counts by 23% to more than 48%. As system impedances drop, it becomes necessary to reduce both Lattach_FPGA, as well as Lspread. This means thinner dielectrics located closer to the FPGA mounting plane. It also means that the inductance of the capacitor attachment vias drops, and by extension that the comparative advantage of X2Y capacitors grows.

As a second example, we determine the lowest impedance that we can meet with currently available materials to a Xilinx Virtex2™ / Pro FF1152 package. For this extreme case, we use 0.63 mil C-ply, and incorporate the ground plane into the upper surface.

From Equation 4:

Lspread = u0 / 2pi * H * ln(R2 / R1) where

And with R2 = 1.2”, R1 = 0.35” we get

Lspread = u0 / 2pi * 0.63E-3 * ln(1.2” / 0.35”) = 3.9pH.

Since we have the ground plane in the upper surface, the height above the planes is only the thickness of the upper plane itself. We assume plate up to 1oz, ie 1.4mils. Lattach_FPGA then becomes from Equation 3:

$$Lvia = u_0 / 2pi * ((H_1^2 * (2 - K_1) / (S * K_1)) + 2 * H_2 * \ln(2 / K_1))$$

K1 = 0.01 / .04 = 0.25

[1] Actual performance will be somewhat worse due to inductance of the additional surface traces.
[2] Actual performance will be somewhat worse due to inductance of the additional surface traces.

Lvia = u_0 / 2pi * ((1.4E-3[2] * (2 – .25) / (.04 * .25)) + 2 * 0.63E-3 * ln(2 / 0.25)) = 15pH.

We target 20pH total, (6mohms @ 50MHz) for an attached capacitor array inductance of 5pH:

	Via								
Cap type	D	S	H_1	H_2	Lsingle	LTot	Lcap	N	Vias
0603 2 via	.01	.05	.0014	.63E-3	17	34	500	107	214
0603 2 via	.01	.03	.0014	.63E-3	13	26	500	105	210[3]
0603 4 via	.01	.03	.0014	.63E-3	13	13	500	103	412[4]
X2Y 0603	**.01**	**.03**	**.0014**	**.63E-3**	**13**	**10**	**60**	**14**	**84**

Table 2. Example, FPGA Bypass Array, 5pH

Table 2 is not a misprint. For this board configuration, only 14 capacitors are needed. This stems from the inherently low self-inductance of the parts. X2Y's component count is approximately 1/8th that of conventional 0603's while using 40% or fewer the vias needed by conventional parts.

- As PDS impedance requirements drop, X2Y advantages increase.

Measurement Results w/ Test Boards

For demonstration, we constructed a series of test boards. Each board is four-layer 0.062" construction with ground plane at 0.012", and power plane at 0.050". Each board has population patterns for two FPGAs and surrounding decoupling capacitors in either an array of 104 conventional 0402 devices, or 32 X2Y 0603 devices. We positioned a series of two pin connectors around the board to simulate FGPA power consumption. We tied all Vcco, and Vccint pads to the power plane.

[3] Actual performance will be somewhat worse due to inductance of the additional surface traces.
[4] Actual performance will be somewhat worse due to inductance of the additional surface traces.

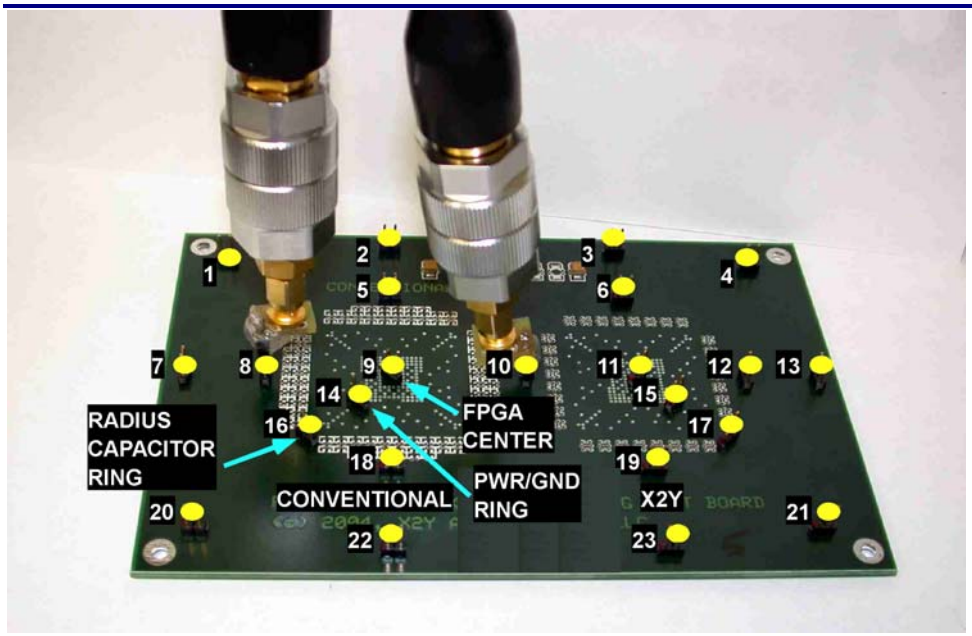


Figure 4. Bypass Capacitor Test Board

Measurements confirm insertion loss and apparent transfer impedance reflects spreading inductance from the power / ground ring to the bypass capacitor radial:

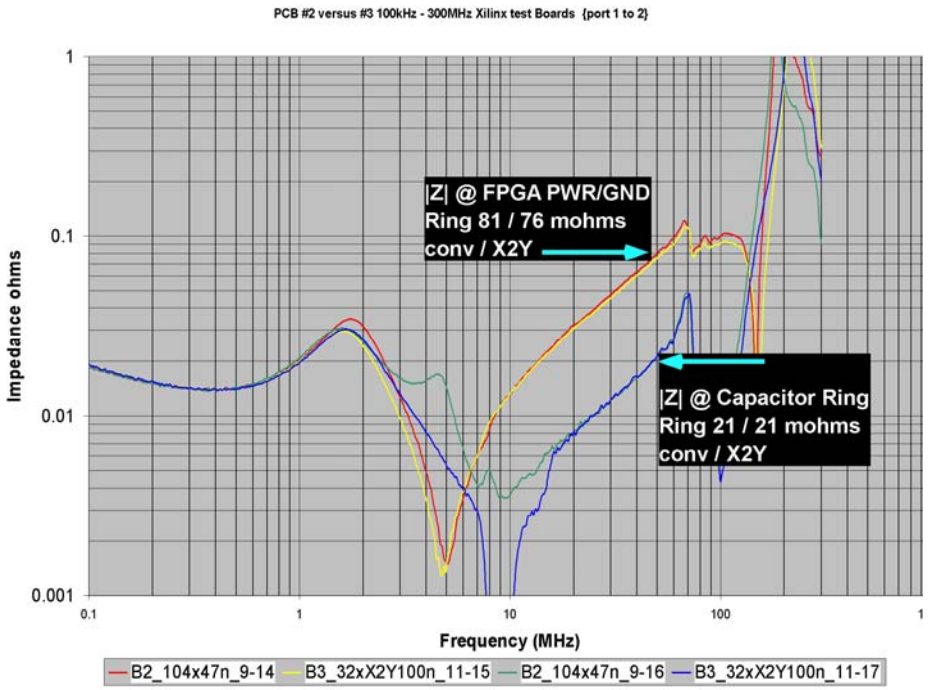


Figure 5. Comparison, X2Y vs. Conv. Widely Separated Planes

The expected results:

Lspread = 5.08E-9 * 38E-3 * ln(1.0”/0.33”) = 212pH

Lvia = u_0 / 2pi * ((12E-3^2 * (2 – .44) / (.02)) + 2 * 0.038 * ln(2 / 0.44)) = 642pH.

Lcaps_mounted_conv = (2 * 642pH + 400pH) / 104 = 16pH

Lcaps_mounted_x2y = (0.75 * 642pH + 60pH) / 32 = 17pH

The SPICE model:

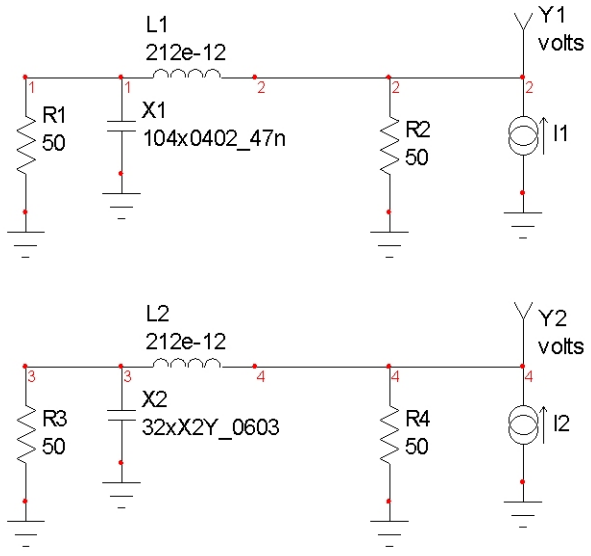
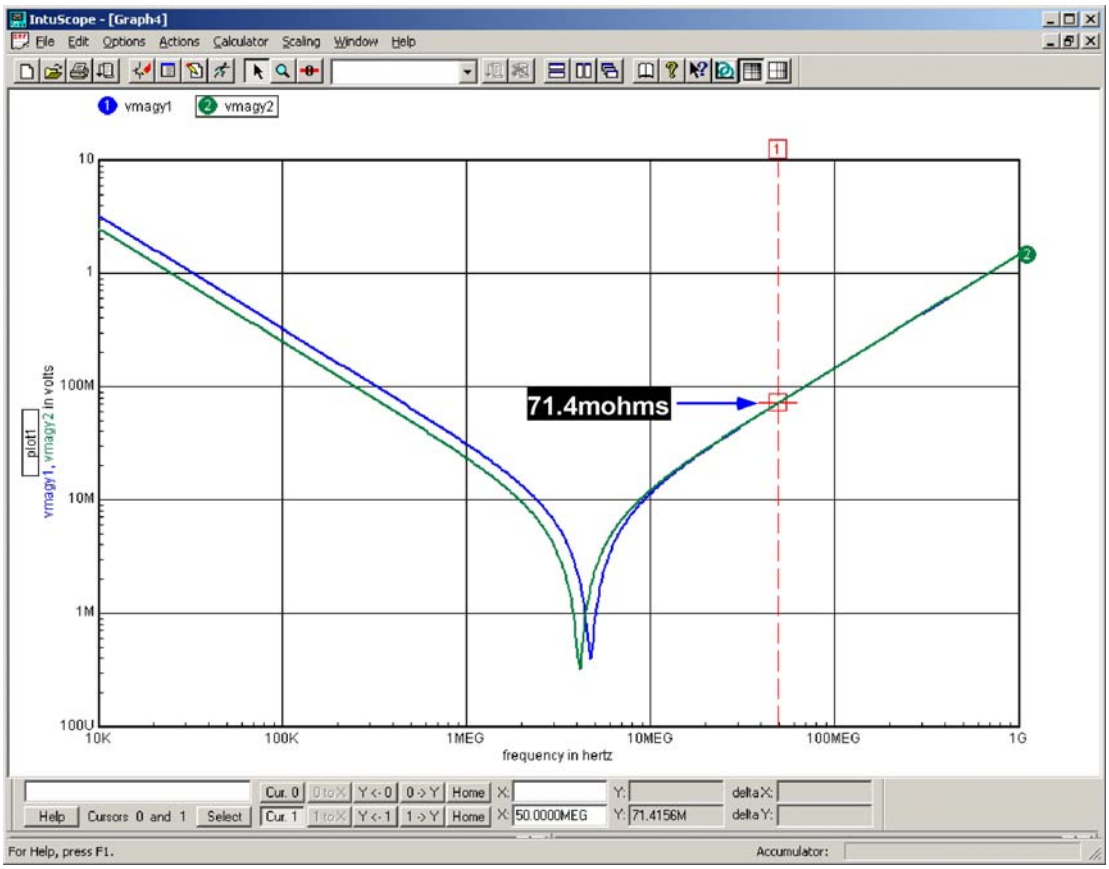


Figure 6. Test Fixture SPICE Model, Simple

And the simulations results:



Correlation between the measurement and simulation is reasonable, with actual results for the X2Y array 6% higher than the simulated value, while the conventional capacitor results are some 13% higher. The additional error with conventional capacitors is likely attributable to mutual coupling between the many capacitors in close proximity. The common error is likely due to deviation of the fabricated board stack-up from the model.

Conclusion

The extraordinarily low inductance of patented X2Y capacitors uniquely suits them to high performance bypass applications of today's modern FPGAs. Because X2Y capacitors can gainfully utilize six vias per capacitor, even in moderate performance systems with very long vias, X2Y capacitors outperform conventional devices 3:1. Test results and decoupling design methodology showing performance ratios of 5:1 will be published in; *High Performance FPGA Bypass Filter Networks*, DesignCon 2005, Jan 31- Feb 3, Santa Clara, CA.

Due to their very low inductance, as FPGA power system demands increase, the X2Y advantage over conventional capacitors climbs dramatically. Compared to conventional capacitors, X2Y capacitors enable extremely low impedance systems with low component counts resulting in major gains in all: raw component, PWB real-estate and in many cases- Total via count.

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